A two-channel 8 Gbps 16:1 serializer ASIC for the ATLAS liquid argon calorimeter upgrade

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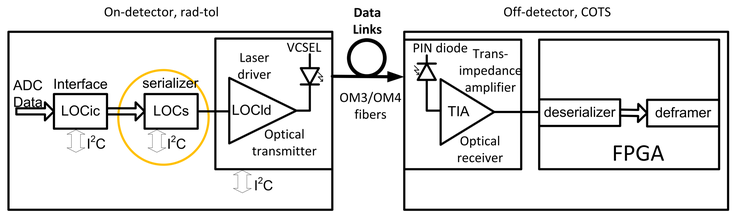
Introduction

LOCs2, a 2-channel, 8 Gbps 16:1 serializer is a prototype ASIC for ATLAS liquid argon (LAr) calorimeter readout upgrade. In the proposed LAr calorimeter readout upgrade, the large volume of data from ADC, about 100Gbps each board, will be continuously transferred to back-end through optical data link[1]. A serial ASICs are demanded for optical link because of its high bandwidth, low power and radiation-tolerant requirements. Serializer is the key component to convert parallel data from ADC to high speed serial data to laser driver. LOCs2 is the second version of serializer we developed based on Silicon-on-Sapphire (SoS) CMOS process.

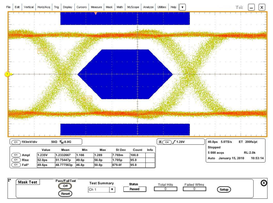


The upgrading ATLAS LAr calorimeter readout optical data link

SoS process and LOCs1 test

The SoS CMOS process, with a thin layer of silicon deposited on highly insulating sapphire substrate, reduces parasitic capacitance and Single Event Upset (SEU) cross section, making it a good technology candidate for ASIC design in detector front-end electronics in particle physics experiments.

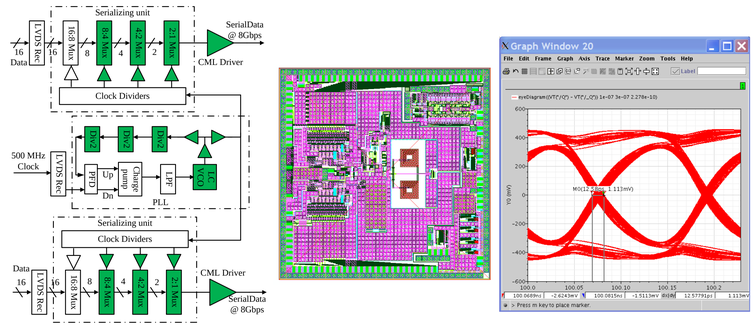
Based on the 0.25 um SoS CMOS technology, we had developed a single channel 5 Gbps 16:1 serializer in 2010, LOCs1. LOCs1 is implemented with CMOS logical and its high-speed clock generator is a 2.5 GHz ring oscillator phase-locked loop. The prototype chip has been successfully tested in lab and proven to be radiation-tolerant in radiation test[2].



The previous version LOCs1: Left) Eye diagram; Right) Radiation test

Current design overview

The current design inherits the structure of previous design. To improve the serializer speed, the clock generator is replaced with a 4 GHz LC-tank phase-locked loop and part of the high-speed circuits are re-designed with current mode logic (green block below). Two serializers share one PLL to save power consumption.

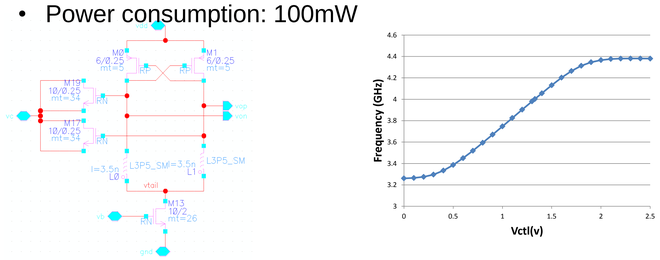


LOCs2: Left) Block diagram; Middle) Layout of the die; Right) Eye diagram of post-layout simulation

LC-tank PLL

LC-tank PLL has low power and low-jitter characters, comparing to ring oscillator based PLL. The core of the LOCs2 clock generator is a LC-tank PLL inherited from previous design in 2010[3].

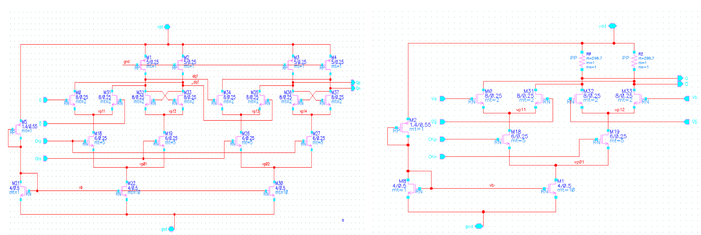
- Frequency center at 4GHz with 20% tuning range
- LC VCO phase noise -110 dBC/Hz at 4GHz
- Power consumption: 100mW



LC-tank VCO: Left) Schematic; Right) V-F curve of VCO

High-speed differential 2:1 multiplexer stage

The serializer comprises 4 multiplexer stages in serial and only last stage is driven by the highest clock signal at 4GHz This stage is composed of two D-flip-flop, a latch and a 2:1 MUX. To achieve high speed and reduce jitter, all circuits are implemented with CML logic.

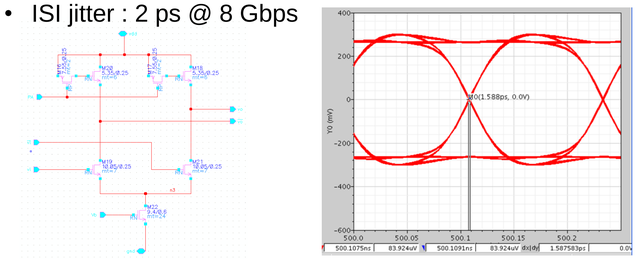


Schematic of CML circuits in last stage: Left) D-flip-flop; Right) 2:1 MUX

CML Driver

The serial data is driven to output by a CML driver.

- Output impedance 50 ohm
- Power supply : 3.3 V
- 5 differential stage structure
- Active shunt-peaking on first 4 stages.
- ISI jitter : 2 ps @ 8 Gbps



CML Driver: Left) Active shunt-peaking circuit; Right) Eye diagram Post-layout simulation

Summary

We designed a two channel, 8Gbps radiation-tolerant serializer for ATLAS liquid argon calorimeter readout optical link system upgrade. The ASIC consumes about 1.2 Watt and its total jitter is estimated to be about 39 ps.

The design has been submitted in June 2012 and will be test in October 2012.

Acknowledgements

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