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A two-channel, 8-Gbps serializer ASIC for the ATLAS liquid argon calorimeter upgrade

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We present a high-speed, low power serializer ASIC, LOCs2, for the ATLAS liquid argon calorimeter upgrade. The ASIC consists of two 8 Gbps serializer channels, each of which has a 16-bit parallel data input in LVDS and a serial data output in CML logic. The ASIC is designed and fabricated in a 0.25-um commercial silicon-on-sapphire CMOS technology which is suitable for the high energy physics front-end electronics applications.

Summary

The optical data link system is extensively used in high energy physics experiments because of its high-speed and low power features. In the proposed upgrade plan of the ATLAS liquid argon calorimeter, the level-1 trigger is generated by processing the digitized detector signals in the back-end to achieve higher efficiency. Without the on-board trigger signal, the bandwidth requirement of the optical link from the super-cell digitizer board (SCD) mounted in the detector is about 300 Gbps, 120 times of the one in the current front-end board. A serializer ASIC is one of the key components demanded for this high-speed, low power, radiation-tolerant optical link system. A single channel 5 Gbps prototype serializer based on a commercial 0.25-μm silicon-on-sapphire CMOS technology had been developed and tested successful in radiation environment in 2010. Based on the same technology, a two-channel, 8-Gbps serializer ASIC, LOCs2, has been designed and will be submitted on June 1, 2012. The fabricated chip is expected to be delivered in August, 2012. The design and the preliminary test results of LOCs2 will be presented.

The LOCs2 consists of two 16:1 serializer channels. Each channel has a 16-bit parallel data input in LVDS logic and a serial data output in CML logic. Same as the previous prototype chip, each serializer channel consists of 4 stage 2:1 multiplex and has a binary tree structure in which only the last stage of 2:1 multiplex operates at 4 GHz. All 2:1 multiplexers are based on static D-flip-flops for better single-event effect (SEE) immunity. To achieve a higher speed than the previous version, CML circuits are used in the last three stages.

The two serializer channels share an LC-tank-based phase locked loop (PLL). The PLL provides each serializer channel with clock signals locked to a reference clock. We choose the same LCPLL prototyped and tested in the previous version. The tuning range has been slightly modified to match the speed of the serializer. The PLL loop bandwidth is programmable from 1.3 to 7.0 MHz, allowing for system jitter optimization.

Each serializer channel has a differential CML driver with 50 ohm output impedance. The driver is composed of five-stage CML differential amplifiers with 3.3V power supply. In the first four stages, an active shunt peaking technique is applied to improve its bandwidth.

In the post-layout simulation, the deterministic jitter is estimated to be about 15 ps (peak-to-peak) operating at 8 Gbps at the nominal conditions and room temperature in the post layout simulation. The random jitter is mainly from LC PLL which has been verified to be about 1.4 ps in previous prototype chip. The power consumption of the LOCs2 is estimated to be 1.2 W.

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