CMS Trigger Drift-Tube Track Finder electronics upgrade
Hardware Simulation

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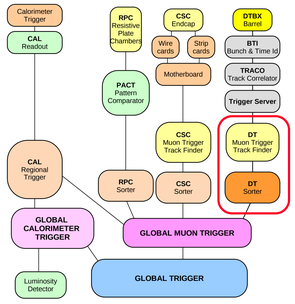


The Drift-Tube Track Finder in the CMS Trigger Chain

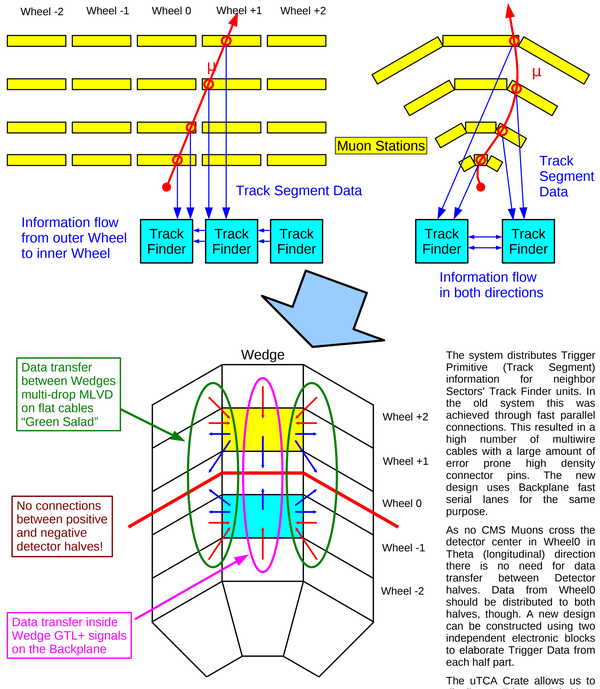
The Bunch and Track Identifier (BTI) units of the Local Muon Trigger identify muon track segments in the detector and assign a local position (azimuth Phi in the plane transverse to the beams, pseudorapidity Eta in the direction along the beams) to them. The Track Correlator (TRACO) units assign a Bending Angle value to the muon hit. The Trigger Server collects information from one 30-degree sector of CMS and forwards it to the Regional Trigger.

The Track Finder System is part of of the Regional Muon Trigger. It receives data from the Trigger Server and performs the Track Finding with them.

The Track Finder calculates which of the muon hits belong to the same track. It selects the highest quality tracks, which are those that are the longest ones, and calculates their physical parameters. The Sorters select the best four muons of all candidates in the barrel area and send them to the Global Muon Trigger.

The Track Finder System consists of two different units. The Phi Track Finder (PHTF) finds muons from the data of the Phi planes of the muon chambers, the Eta Track Finder (ETTF) from the Eta planes.

The Sector based Track Finder units exchange Trigger Primitive information with neighbors both in Phi and Eta direction

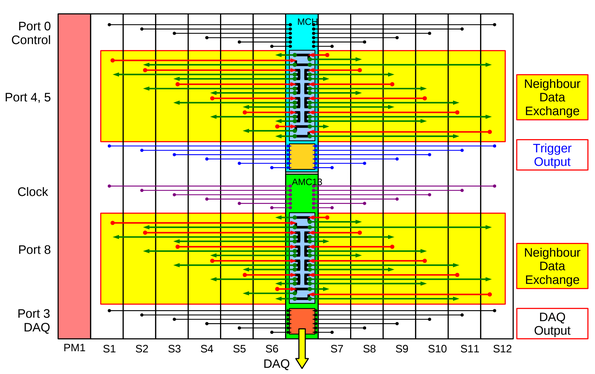


The system distributes Trigger Primitive (Track Segment) information for neighbor Sectors' Track Finder units. In the old system this was achieved through fast parallel connections. This resulted in a high number of multiwire cables with a large amount of error prone high density connector pins. The new design uses Backplane fast serial lanes for the same purpose.

As no CMS Muons cross the detector center in Wheel0 in Theta (longitudinal) direction there is no need for data transfer between Detector halves. Data from Wheel0 should be distributed to both halves, though. A new design can be constructed using two independent electronic blocks to elaborate Trigger Data from each half part.

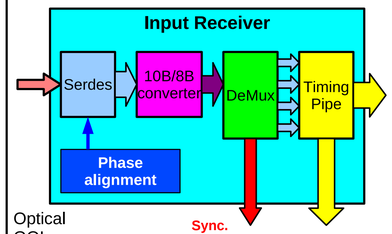
The uTCA Crate allows us to distribute Trigger Primitives through Backplane Fast Lanes.

New system designed using uTCA Crate



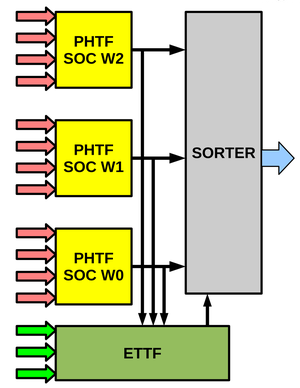
Simulation Blocks for development

Input Deserializer Block



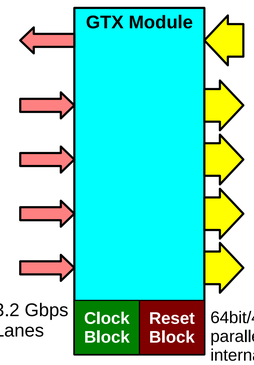
Design features:
- 18 Input Receivers total
  - 3x4 Input Receivers for Phi Sectors
  - 6 Input Receivers for Eta Half Wedge
- Serdes in 10-bit mode
  - Using CMT Block
    - Internal Clock with PLL Clock multiplier
  - Connected 10B/8B converter
  - Intenal bus runing with 160MHz
- Demultiplexer to arrange 32-bit words
  - Dimensioned for present 110 bits + spare
- Real time synchronization error message
- Simulation to test Serdes latency
  - Input latency must not be more than in present Optical Receiver + Inrec Chip
- Timing pipe – as present design
  - Max. 16BX programmable delay
  - Separate delay pipe for CSC TF
- Simulation results
  - Clocking as main issue
    - Common clock not possible
    - Keep separate clock domains

Main Logic Block



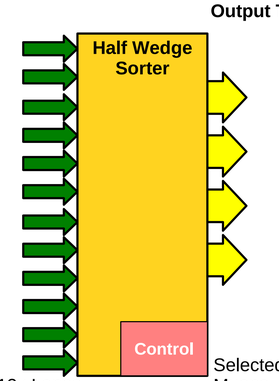
Design features:
- Merge VHDL Codebase
  - 3xPHTFs + ½ ETTF + ½ WS
  - Without Input Receivers and Output Ports of the present design
    - These are separate Blocks under development
- New Blocks added to follow technology change
  - Xilinx Clock (CMT)
  - Use internal Dynamic Reconfiguration Port
    - For Clocks and Interfaces
    - Limited extent, keeping design simple
- Perform feasibility study
  - FPGA with Optimal fitting
  - Latency requirements
    - Decrease latency to cover Link latency increase
  - Test LUT features in new design platform (Xilinx)
- Testbench rebuilt from present PHTF TB
  - Use existing physical simulation result files
  - Feed into 3 TF blocks instead of one PHTF

Neighbor Data Exchange Transcievers

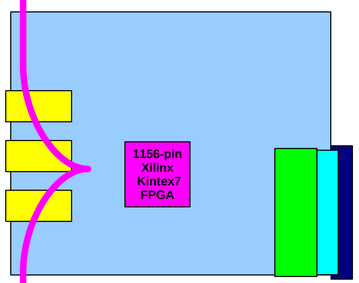


Design features:
- Use Kintex built-in GTX Units
  - Simulation: 1xOutput, 4xInput
  - Final design: 2xOutput, 4xInput
  - Common clocking for all modules
    - Clock derived from LHC Clock
- Design with Xilinx Core Generator
  - 10B/8B conversion for balancing and signaling
    - Standard Xilinx converter block
    - Synchronization sequences only for startup
  - Standard reset sequence generation
  - Automatically creates correct CMT block
    - Best fit Clock parameters
  - Bypass Transmit and Receive buffers
    - Latency decrease
- Testbench with loopback and data link fanout
  - Simulates fanout crosspoint switch
  - Data integrity is checked inside the FPGA
    - Comparing output and input data stream
    - Practice recommended by Xilinx design tools

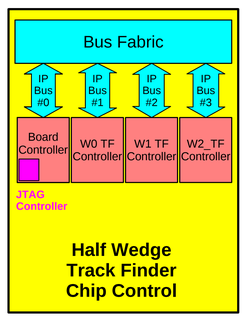
Output Trigger Object Sorter



Design features:
- Based on present Wedge Sorter
  - Taking over existing VHDL codebase
  - Ghost cancellation schemes integrated
  - Flexible ranking
- Simulation of timing
  - TF design foresees Track Category 2 BX before Track Parameters
- Output feeds GTX Link to Global Sorter
- Testbench requires integration with TF functions
  - No separate Trigger Output simulation possible
- Testability
  - Include spy block in Sorter

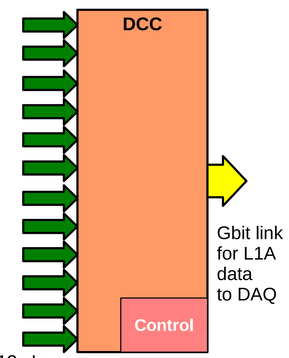


IPBus Control Unit



Design features:
- IPBus HDL Blocks taken from CERN IPBus community
  - Reserve separate IPBus instances for each sub-unit
    - Merging scheme remains simple
  - Interface existing Control Scheme with IPBus
    - Registers are already compatible
    - Memory structures follow
  - Add control for new design items
    - GTX Links
    - Input Circuits
    - Dynamic Reconfiguration Port
  - Limited address range – separate sub-unit ranges
    - Increases transparency
    - Easier maintenability
  - JTAG controller block to include
    - Timing differs from other, on-chip memory or internal register based targets
- Compatibility on Control Software level
  - Merge CERN IPBus access and addressing programs with present control schemes
  - Database issues with future CMS-wide solution
- Simulation Testbench
  - Copy of CERN IPBus testbench

DAQ Block



Design features:
- Redesign present DCC according new requirements
  - Separate blocks for detector halves
  - Inputs
    - Fast Lanes replace Channel Links
    - Rigid synchronization scheme not applicable
    - New synchronization based on data block header
    - New zero suppression scheme
  - Internal data handling
    - Consider and test new format
    - Simulate Buffer management
  - Outputs
    - New output links replace SLINK
    - Change output data format
    - Refinement in MMC system
- New DCC on a separate ouput card
  - Build as mezzanine for AMC13
- Testbench with new algorithms
  - Deliver new data format
  - Analyze MMC reaction

Conclusions

- Blocks synthesable in Xilinx Kintex7
  - Optimizing for built-in chip features
    - Serdes
    - GTX Blocks
    - Memories
    - Clocking system
  - Synthesis results ready for prototying
- New FPGA features allow enhanced physics performance
  - More inputs
    - Finer parameters for CSC data exchange
    - Possible RPC hits around detector gaps
  - More output bits
    - Increase Phi, Pt resolution
    - 8 instead of 4 Muons found in every BX
    - More efficient charge assignment
- Resource requirements differ from earlier designs
  - Determined by FPGA dependent building blocks
  - Extensive efforts needed to port present design
- Control scheme common with other CMS Upgrade projects
  - Possible to develop system wide software solutions
- Clocking will be a main concern
  - Not all units' clocks can be derived from LHC Clock
  - Independent clock domains foreseen
    - Sophisticated interfacing between them necessary
  - Chip design requires global clocking scheme