Contribution ID: **116** Type: **Poster**

CMS Trigger Drift Tube Track Finder electronics upgrade Hardware Simulations

Tuesday 18 September 2012 17:43 (1 minute)

The upgrade of the Drift Tube Track Finder (DTTF) electronics will be designed using VHDL synthesis. The construction of the HDL structure merges improved blocks of the Track Finding algorithms and the results of the CMS wide detector control, monitoring and DAQ output common development. This merged design is subject of extended simulations both on behavioral level and concerning the timing constraints. The simulation results help in generating the complete
design documentation.

Summary

The latency requirements of the CMS Trigger System, together with the semiconductor technology available at the time of the DTTF design required to construct a fully parallel high speed data network to distribute the Trigger Objects prior to their elaboration. This network is, however, the most unreliable component of the DTTF system, whose maintenance is time consuming and error prone. The other weak point of the present DTTF is its control. Implemented in seven VME crates, the control and monitoring access is slow and complex, its software components are custom-built. In addition, the present system is optimally tailored for the physics requirements of the present CMS trigger system. Physical constraints, like board and FPGA size and connector placement do not allow to increase its capabilities to accept more detailed, higher resolution or different Trigger Objects for the case of a future detector upgrade.

The upgrade design allows us to exploit the results of the recent and near future developments in the electronics. A more compact design using reliable high speed backplane serial links for data distribution and control could be constructed as a low cost DTTF system. The design framework will be a uTCA chassis which contains by design all fast serial links necessary for the DTTF internal data distribution. The new design, similarly to the present one, would use Field Programmable Gate Arrays to implement all required logic functions and processes. The new, highly integrated FPGAs also make it possible to merge the functionality of several electronics cards of the present DTTF together with the control, monitoring logic and the necessary I/O blocks into one FPGA.

The upgrade activity of the DTTF electronics is planned to be synchronized with upgrade plans of other members of the CMS electronics community. We want to use common design platforms, compatible developments of common services all based on CERN electronics R/D activity results. This baseline uses a fast lane besides the uTCA standard IPMI connection that will only be responsible for the slow control and firmware bootstrapping. Data traffic will use fast connections to all uTCA AMC boards. The foreseen solution IPBus maps a register-based control system into the externally accessible Ethernet network.

The DTTF development seizes the opportunity to map the present system control structure into the future one. In addition, this framework gives the possibility to add further control objects. The development has started by preparing the new control structures and establish a connection to the DTTF VHDL Blocks. The new development is also programmed using VHDL language. It reuses the existing VHDL blocks of both the present DTTF system and the CMS supported IPbus. The merged system is subject of extended simulation activity. The results of the simulation will give the basis to develop the control software framework, too. They also provide information for the FPGA and link feasibility. The simulation blocks are constructed to be fully synthesisable. The simulation and synthesis steps are maintained in parallel. The results will be shown in this presentation.

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Session Classification: POSTERS