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An 8-channel Programmable 80/160/320 Mbit/s Radiation-Hard Phase-Aligner Circuit in 130 nm CMOS

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The design of an 8-channel phase aligner is presented that is to be used in the GBTX chip for the LHC upgrade program. The circuit is able to align the phases of up to 8 parallel data streams to the GBTX transmitter clock so that the data can be serialized. The bit rate is programmable between 80, 160 or 320 Mbit/s. Data jitter up to ± 3•Tbit/8 can be tolerated without compromising the errorless operation. The phase-aligner has been designed as a radiation-hard circuit in a 130 nm CMOS technology.

Summary

The proposed circuit is part of the GBTX (GigaBit Transceiver) chip which monolithically encompasses data readout, trigger and control for the LHC upgrade program. As an on-detector chip, the GBTX is a radiation-hard design that is connected to the counting room by means of two optical fibers, one for transmitting data and another for receiving data, and to the experiments'front-end modules with electrical links. These links have a programmable bit rate of 80, 160 or 320 Mbit/s. The physical length of the links is determined by the front-end position with respect to the GBTX and is therefore different for each of them. Consequently, the data from the electrical links arrives at the GBTX with different phases. Eventually, all the data is serialized by the GBTX so that it can be transmitted to the counting room. Therefore, a circuit taking care of phase alignment is required to equalize the phases of all incoming electrical links to the transmitting clock.

The operation principle of the phase-aligner is based on the generation of 14 versions of the data stream, each delayed by Tbit/8. The delay line generating these has thus a total delay of 7•Tbit/4. The phase selection algorithm determines which version is best aligned with the transmitter clock. Although one might think that having a total delay line delay of Tbit is sufficient, having the extra delayed versions extending in the previous bit results in a jitter tolerance up to ± 3•Tbit/8 instead of only ± Tbit/8. The bit rate of an electrical link being programmable, the total delay of the delay line has to change accordingly. Instead of changing the delay of a single delay line cell, this has been implemented by changing the number of delay line cells from 14 for 320 Mbit/s to 56 for 80 Mbit/s. Consequently, the delay cells always operate in the same region with the same control voltage which is advantageous for the control loop.

The control voltage for the delay cells is generated by means of a DLL (Delay-Locked Loop) that equalizes the delay of a separate delay line to Tbit. In contrast to the data delay lines, this DLL delay line consists therefore of 8, 16 or 32 cells for 320, 160 or 80 Mbit/s respectively. The control voltage is distributed between 8 identical data delay lines working at the same bit rate. Because of the bang-bang nature of the DLL, jitter is generated in the data delay lines. By a considerate design, the jitter at the delay line output has been kept below 11 psRMS for a bit rate of 80 Mbit/s (56 delay cells) which is excellent for the application.

Three operation modes are provided:

- Fixed tap selection, given by configuration
- Automatic lock at startup only
- Continuous lock tracking during operation

Every bank of registers in the phase selection logic has an individual clock gating to save power in the first two operation modes.

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