Cold electronics for the LBNE LAr TPC

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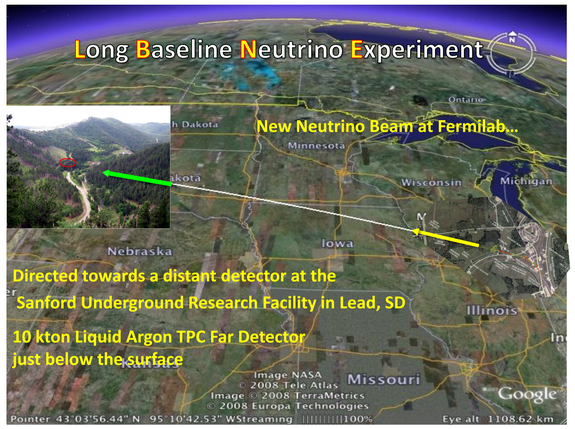
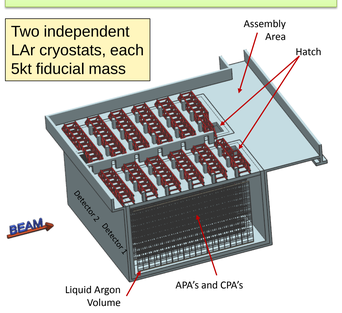


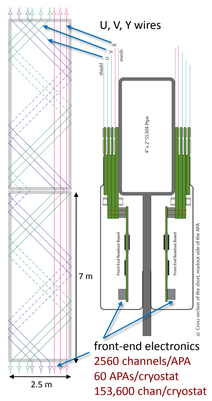
Why put the signal processing chain in LAr?

1. The proximity of the charge sensitive amplifier to the sense wires reduces cabling capacitance, and therefore noise.
2. Digitizing, zero-suppression, and multiplexing in LAr minimize the cable plant, decreasing contamination of LAr and decreasing dead volume
3. Fewer feed-throughs are required in the cryostat decreasing contamination risk and increasing cryostat design flexibility
4. Electronics are incorporated into anode assemblies, manufactured, tested, and installed as a unit, with minimal cabling, increasing reliability

LBNE Far Detector - LArTPC

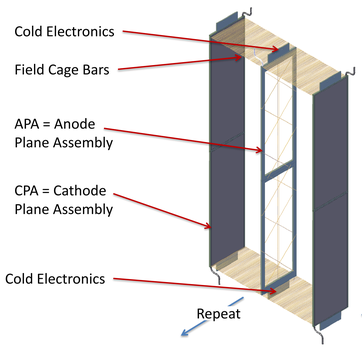
Two independent LAr cryostats, each 5kt fiducial mass





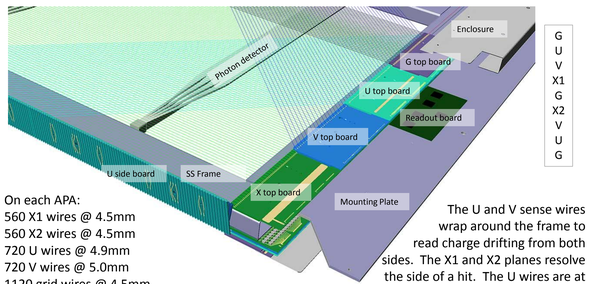
APAs are structural & electrical units, containing all sense wires and readout electronics. They are standardized manufactured assemblies, can be tested in LN2, stored and transported in shipping containers.

APA + CPA Assemblies form TPC Modules in a Large Cryostat



Unit Cell
TPM = TPC Module = 1 APA + 1 CPA (+1 "terminal" CPA)

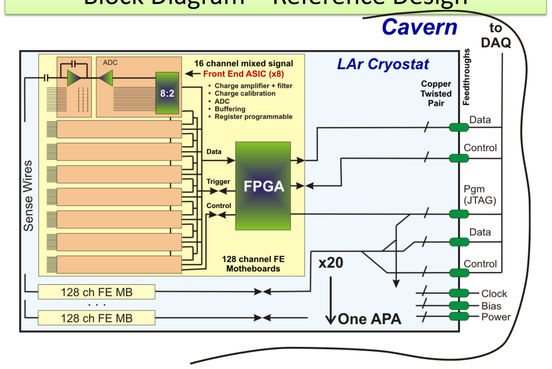
Active volume/APA
2 x 2.5m H x 7m W x 2.5m drift = 87.5 m³ = 122 t =7.33 kt active/cryostat

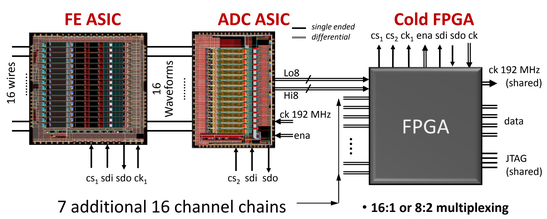


On each APA:
560 X1 wires @ 4.5mm
560 X2 wires @ 4.5mm
720 U wires @ 4.9mm
720 V wires @ 5.0mm
1120 grid wires @ 4.5mm
20 front end mother boards (128ch) mounted on one end of the frame.

The U and V sense wires wrap around the frame to read charge drifting from both sides. The X1 and X2 planes resolve the side of a hit. The U wires are at 45.7° and V wires are at 44.3° to the long axis to resolve ambiguities in hits on the two sides

LAr TPC - Cold CMOS Electronics Block Diagram – Reference Design





7 additional 16 channel chains

- low-noise analog amplification
- programmable

- ADC 12-bit 2MS/s
- small buffer
- 2 x **8:1 multiplexing**

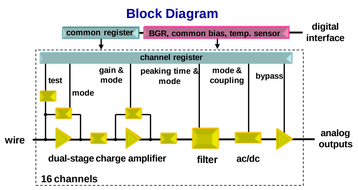
- **16:1 or 8:2 multiplexing** (total 128:1 or 64:2)
- timestamp
- compression
- zero suppression
- neighbor triggering

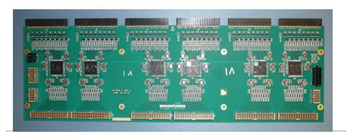
- **ASIC development complete**

- **ASIC development in progress**
- **Final prototype by mid 2013**

- **Cold FPGA tests in progress (power, lifetime, driving)**
- **Selection by early 2013**
- **Full chain test by late 2013**

Analog Front-End (FE) ASIC for Operation in LAr

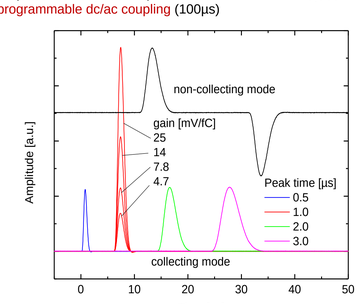




Prototype Vertical Cold Mother Board populated with 4th version of prototype ASICs

- 16 channels
- charge amplifier, high-order anti-aliasing filter
- programmable gain: 4.7, 7.8, 14, 25 mV/fC (charge 55, 100, 180, 300 fC)
- programmable filter (peaking time 0.5, 1, 2, 3 μs)
- programmable collection/non-collection mode (baseline 200, 800 mV)
- programmable dc/ac coupling (100μs)

- technology CMOS 0.18 μm, 1.8 V
- **designed for room and cryogenic operation, >20 yr lifetime at 88K**
- 136 programming registers with digital interface
- 5.5 mW/channel (input MOSFET 3.9 mW)
- single MOSFET test structures
- ~ 15,000 MOSFETs



Bandgap Reference:

$$V_{BGR} \approx \begin{cases} 1.185\ V & at\ 300\ ^{o}K \\ 1.164\ V & at\ 77\ ^{o}K \end{cases}$$

variation ≈ 1.8 %

Calibration Capacitor:

$$C_{INJ} \approx \begin{cases} 184\ fF & at\ 300\ ^{o}K \\ 183\ fF & at\ 77\ ^{o}K \end{cases}$$

variation ≈ 0.5 %

Temperature Sensor:

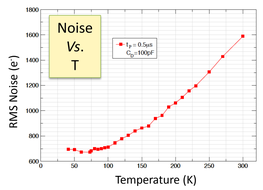
$$V_{TMP} \approx \begin{cases} 867.0\ mV & at\ 300\ ^{o}K \\ 259.3\ mV & at\ 77\ ^{o}K \end{cases}$$

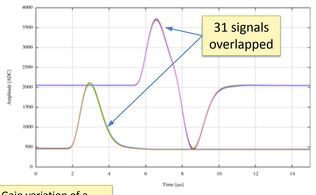
variation ~ 2.86 mV / °K

Maximum charge of 55, 100, 180, or 300 fC

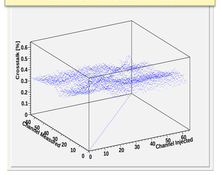
Measurements for FE ASICs on MicroBooNE Motherboard

Performed with the entire MicroBooNE signal chain: Analog ASIC + cold cable + intermediate amplifier + ADC

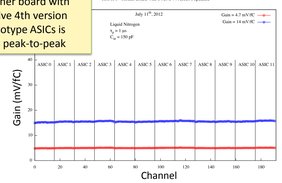




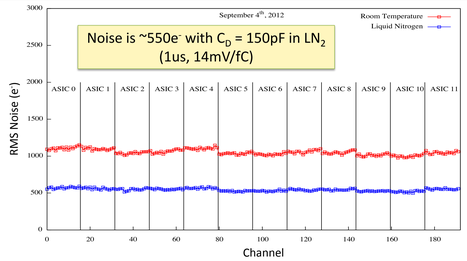
Measured Crosstalk < 0.3%

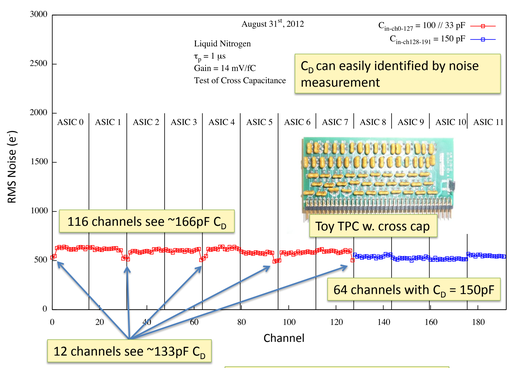


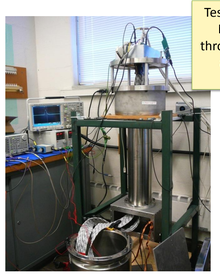
Gain variation of a mother board with twelve 4th version prototype ASICs is ~7% peak-to-peak



Test of 12th Mother Board with 12 ASICs Populated (192 channels)







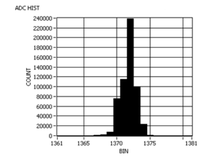
Test setup for assembled FE boards Models the MicroBooNE feed-through, cabling, ASIC motherboard, and cryostat for testing of the electronics chain

The FE ASICs have been extensively tested both warm and in LN2. The chip yield for both is >90%.

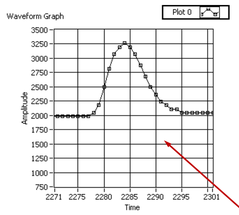
The ASICs and the motherboard have experienced >1000 chip immersions in LN_2, without a single failure

Low Power CMOS ADC Designed for Operation in LAr

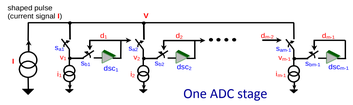
Performance at 77K



ADC Output Histogram DC



Clockless Low Power Current Mode ADC



Dual stage: 6-MSBs in 150ns, then 6-LSBs in 250ns

- Single conversion trigger per stage
- 12-bit resolution
- 2 MS/s conversion rate
- Power dissipation 3.6 mW/ch at 2 MS/s

Measured linearity

- DNL < 1.5 LSB for majority of codes
- INL ~1% of Range

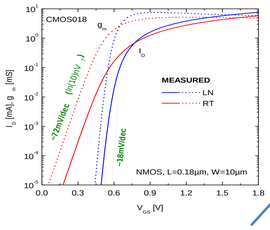
Equivalent input noise measurement

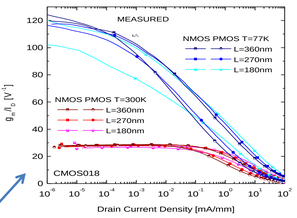
- 1.27 LSB
- Effective resolution: 11.6 bits

Fabricated for normal temperature operation for SNS, see De Geronimo, et al., *IEEE Trans NSS*, **54** (2007) 541.

The ADC has been tested with an FPGA, both immersed in LN_2

CMOS Characteristics in LAr





Transconductance/drain current $\Rightarrow \frac{g_m}{I_D} \rightarrow \frac{q}{nk_BT} = \begin{cases} \sim 30 & at\ T = 300K \\ \sim 116 & at\ T = 77K \end{cases}$

At 77-89K, charge carrier ***mobility*** in silicon *increases* and ***thermal fluctuations*** *decrease* with ***kT/e***, resulting in a ***higher gain***, ***higher*** g_m/I_D, ***higher speed*** and ***lower noise***.

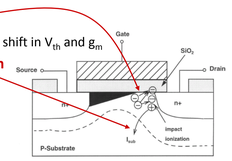
Lifetime of 180nm CMOS for use in LArTPCs

Degradation is due to **impact ionization**

- charge trap in oxide, interface generation → shift in V_{th} and g_m

Substrate current monitors impact ionization

- increases with drain voltage
- is higher in short channel devices
- has a maximum at $V_{GS} \approx V_{DS}/2$



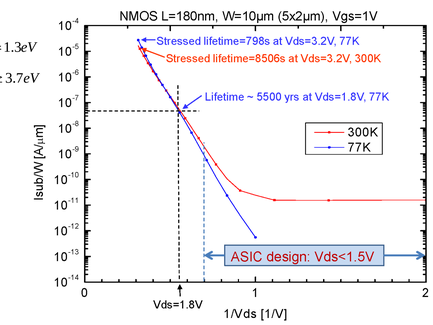
$$I_{sub} = c_1 I_{ds} e^{-\varphi_i/qλE} \qquad \varphi_i \simeq 1.3eV$$

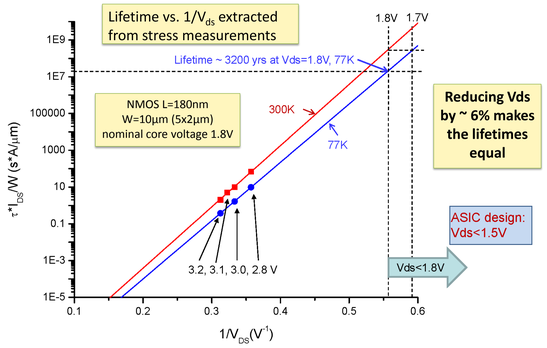
$$\tau = c_2 \frac{W}{I_{ds}} e^{-\varphi_{it}/qλE} \qquad \varphi_{it} \geq 3.7eV$$

so

$$\tau = \frac{c_3}{I_{ds}/W} \left(\frac{I_{sub}}{I_{ds}}\right)^{-\varphi_{it}/\varphi_i}$$

with $\varphi_{it}/\varphi_i \simeq 3$





Reducing Vds by ~ 6% makes the lifetimes equal