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Cold electronics for the LBNE LAr TPC

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The LBNE Project is developing modular multi-kiloton liquid argon time projection chambers for the Long Baseline Neutrino Experiment. A complete electronic readout system operating in LAr for 20 years is essential to this design. We are developing 180 nm commercial technology CMOS ASICs, with low-noise readout of the TPC wires, digitization, zero-suppression, buffering and output multiplexing. An analog frontend is complete, and will be used in the MicroBooNE LArTPC. Prototypes of the digital section have been fabricated. Results demonstrate that CMOS transistors have lower noise and improved DC characteristics in LAr. We describe results and planned development.

Summary

The LBNE Project is developing designs for scalable, modular multi-kiloton liquid argon (LAr) time projection chambers to be used as the far detector for the Long Baseline Neutrino Experiment. An essential component of this design is a complete electronic readout system designed to operate in LAr (at 87 K). This system is being implemented in mainstream commercial CMOS technology that will provide low-noise readout of the signals induced on the TPC wires, digitization of those signals at an appropriate sampling frequency (1-2 MS/s), zero-suppression, buffering and output multiplexing to a small number of cryostat feedthroughs. A resolution better than 1000 rms electrons at 200 pF input capacitance for an input range of 300 fC is required, along with low power (<15mW/channel) and operation in LAr with a lifetime greater than 20 years. An analog-only frontend ASIC in has been successfully completed and fully evaluated. The charge amplification is obtained in two stages, each with adaptive reset and nonlinear pole-zero cancellation, and it provides a charge gain up to 320, adjustable to 4.7, 7.8, 14, and 25 mV/fC. The charge amplifier is followed by a high-order semi-Gaussian anti-aliasing filter with adjustable time constant (0.5, 1, 2, and 3 microseconds) and an ac/dc coupling stage which, when enabled, introduces an ac time constant on the order of 100 microsecond. Each channel also implements a high-performance analog buffer, which in the final version will be replaced with a sample-and-hold stage preceding the ADC. In its current version, this analog ASIC is being used as the front end for the MicroBooNE LAr TPC detector scheduled for operation in early 2014. The dissipated power is about 5mW/channel, plus an additional 5mW in each output buffer. A prototype of a low power 12-bit current mode ADC has been fabricated as a separate ASIC and is being evaluated. All circuits are designed using rules that have been developed to ensure a long lifetime at cryogenic temperatures. The results demonstrate that CMOS transistors have lower noise and much improved DC characteristics at LAr temperature. The ASICs have comparable signal response at room and cryogenic temperatures, while the noise at low temperature is significantly reduced.

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