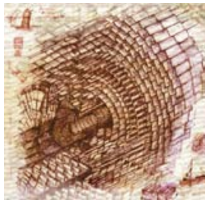


A DC-DC Conversion Powering Scheme for the CMS Phase-1 Pixel Upgrade

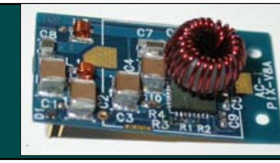
Lutz Feld, Martin Fleck, Marcel Friedrichs, Richard Hensch, Waclaw Karpinski, Katja Klein, Jan Sammet, Michael Wlochal

1. Physikalisches Institut B, RWTH Aachen University

Topical Workshop on Electronics for Particle Physics

Oxford, September 20th, 2012

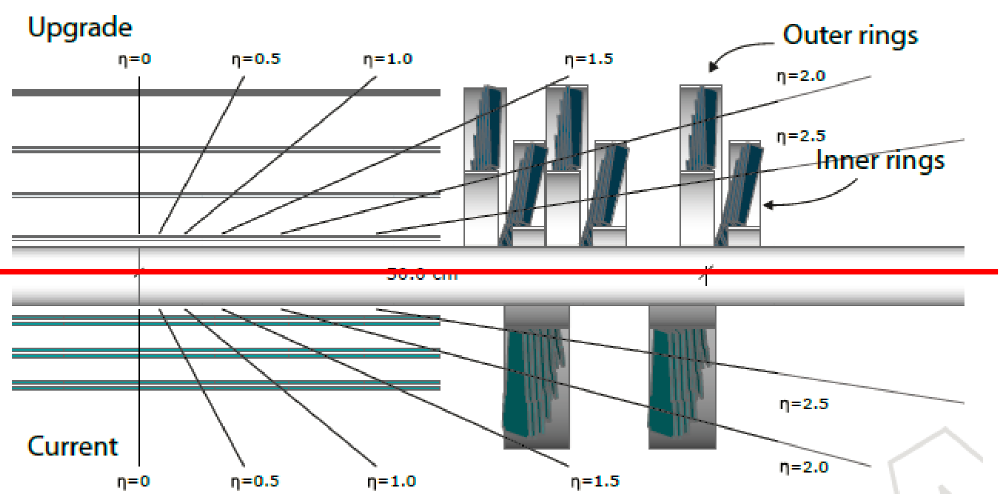
The Phase-1 Pixel Upgrade



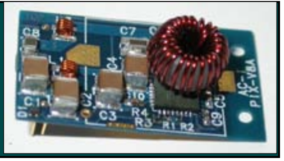
- During LHC Phase 1 the luminosity will be doubled, up to ~ $2 \cdot 10^{34}\ cm^{-2}s^{-1}$
  → **Exchange of CMS pixel detector in shutdown 2016/2017**
  - Optimized readout chip (ROC)
  - Less material, e.g. through CO_2 cooling
  - **Factor of 1.9 more channels → factor 1.9 higher power consumption**
- **Existing services must be re-used**
  → Power losses in cable channels increase by factor ~ 4 → heat load too high
  → will move to a DC-DC conversion powering scheme

Phase-1 layout

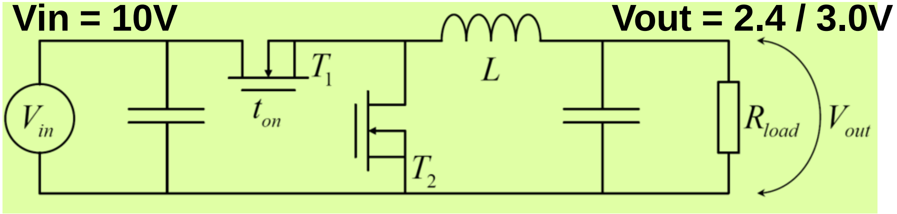
Present layout



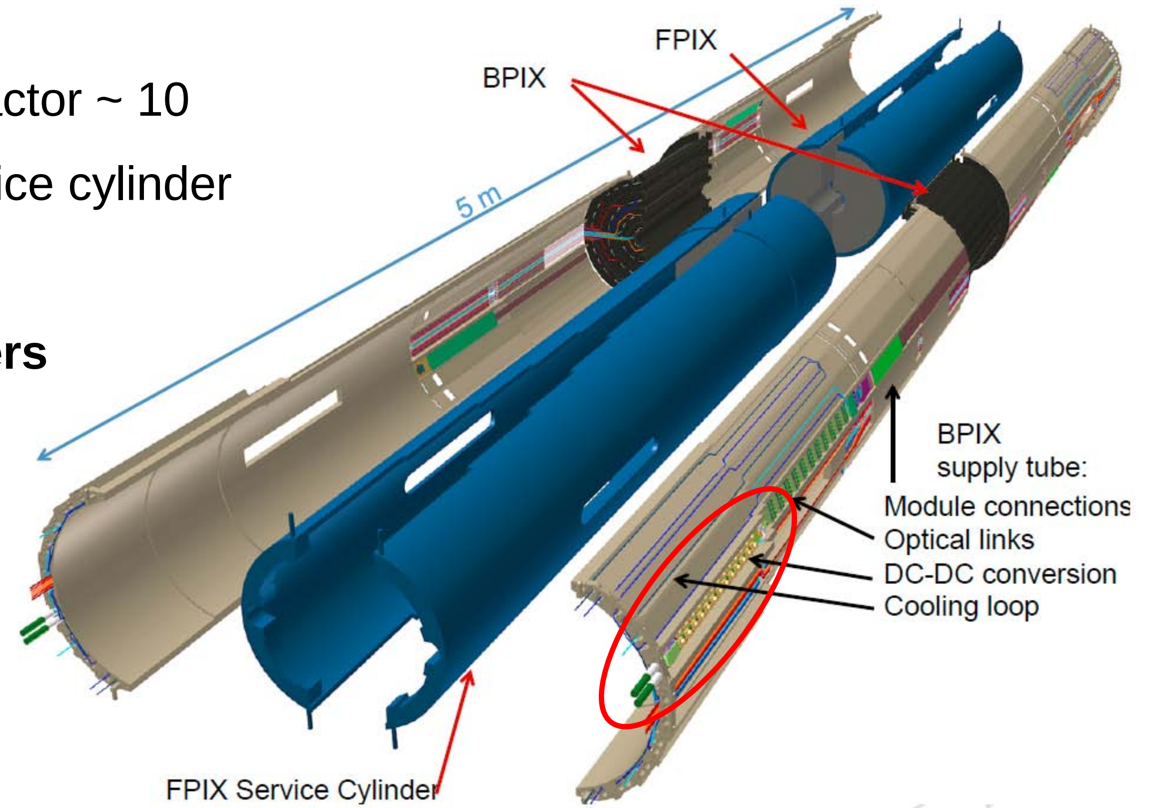
DC-DC Powering for the Pixel Upgrade



- **DC-DC buck converters**
  - Vin = 10V
  - Vout = 2.4 or 3.0V (analog and digital pixel module circuitry)
- Conversion ratio of 3-4 → power losses reduced by factor ~ 10
- Located on supply tube & service cylinder
- Cooled from CO_2 pipes
- **In total 1184 DC-DC converters**



2.2m distance to front-end → material and EMI less critical than in other applications



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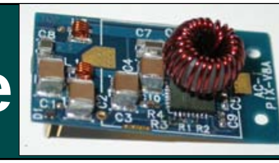
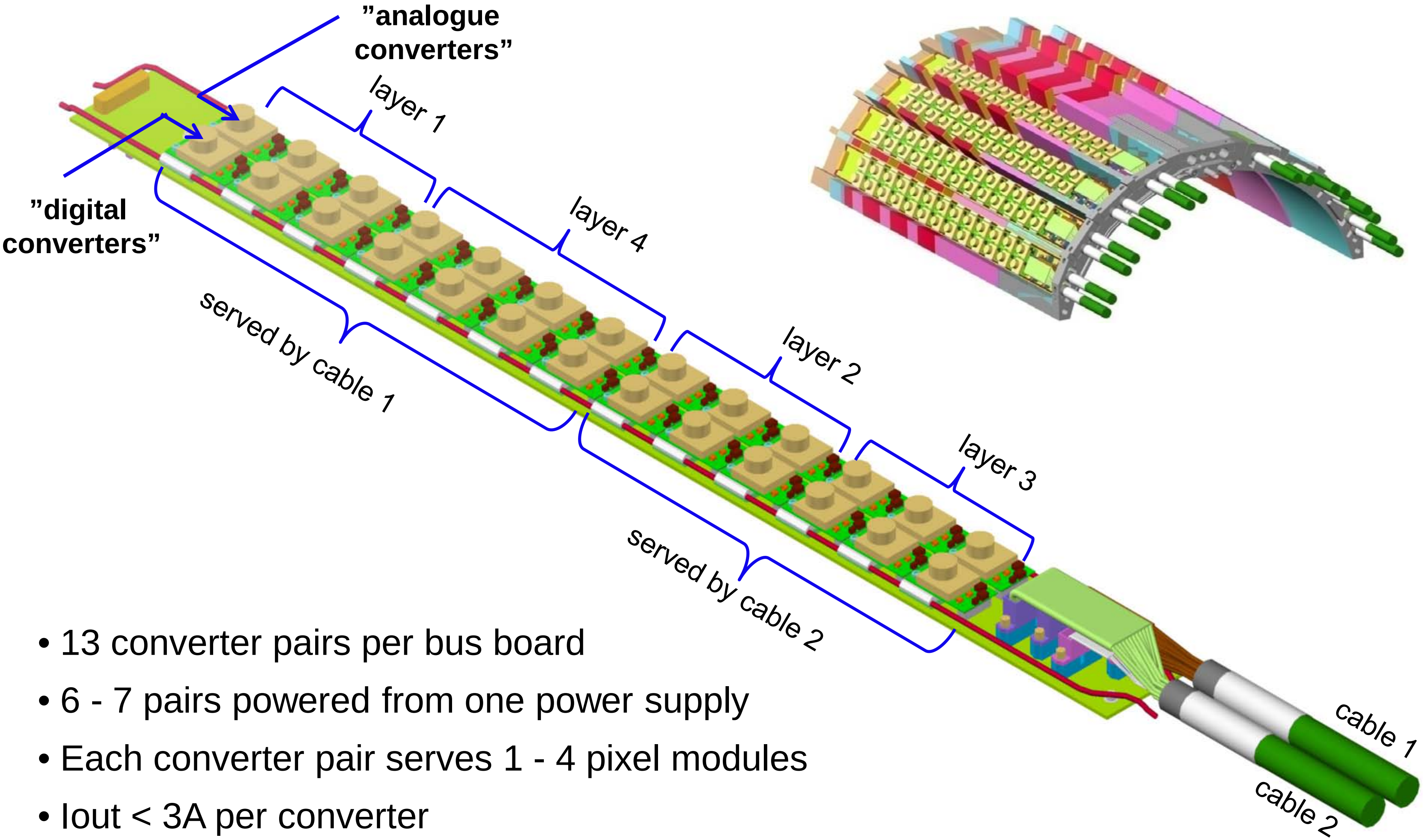
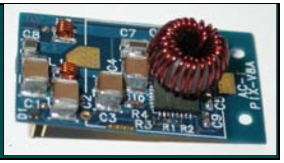




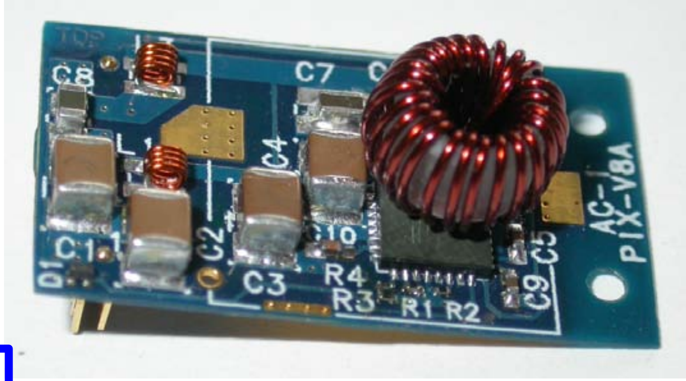
- 13 converter pairs per bus board
- 6 - 7 pairs powered from one power supply
- Each converter pair serves 1 - 4 pixel modules
- Iout < 3A per converter

AC_PIX_V8 DC-DC Converters



Custom rad.-tolerant tolerant buck converters, optimized for our application

V_{out} = 3.0V or 2.4V
Switching frequency f_s = 1.5MHz
2-layer PCB
Toroidal plastic core inductor L = 450nH
Pi-filters at in- and output

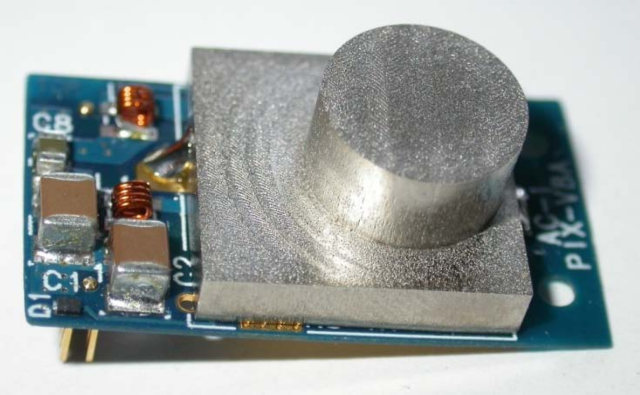


AC_PIX_V8 A: 2.8cm x 1.6cm; ~ 2.0g

ASIC: AMIS4 by CERN-PH-ESE (St. Michelis, F. Faccio)
Latest available prototype in radiation-tolerant
AMIS I3T80 0.35µm CMOS (ON Semiconductor)
[2012 JINST 7 C01072]

Why is a shield required?

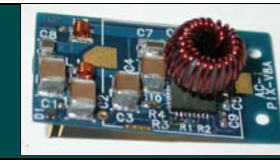
- ✓ to shield the magnetic emissions
- ✓ as cooling contact for the coil
- ✓ to segregate “noisy“ parts from output filters



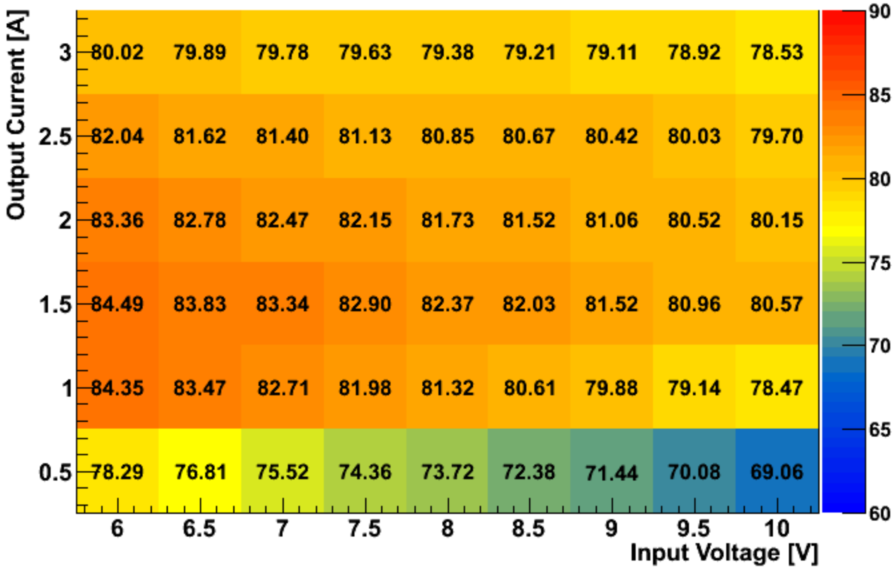
Aluminium shield

→ 60 DC-DC converters have been built

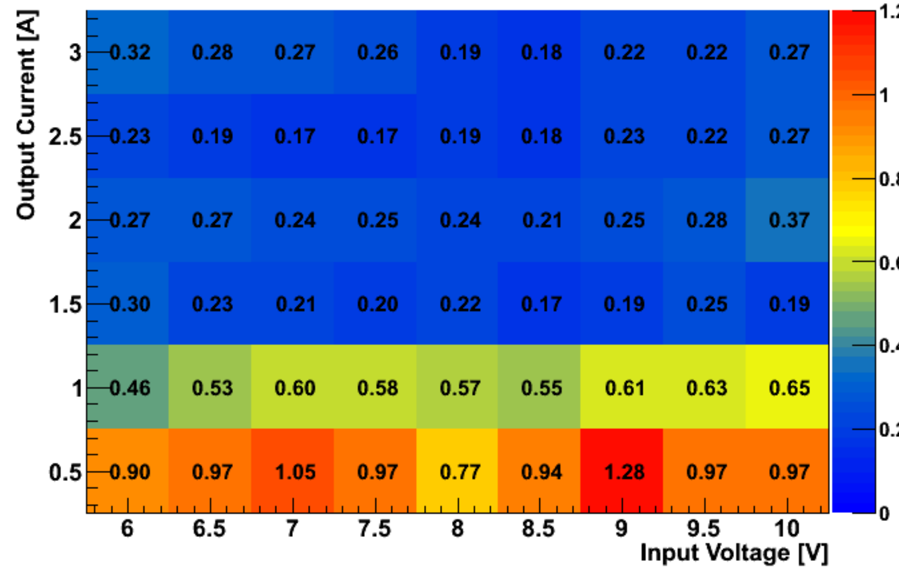
Power Efficiency



Mean efficiency (12 converters) V_{out}= 2.5V

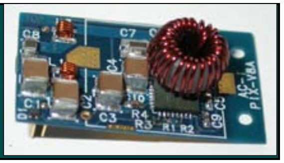


Standard deviation (12 converters) V_{out}= 2.5V

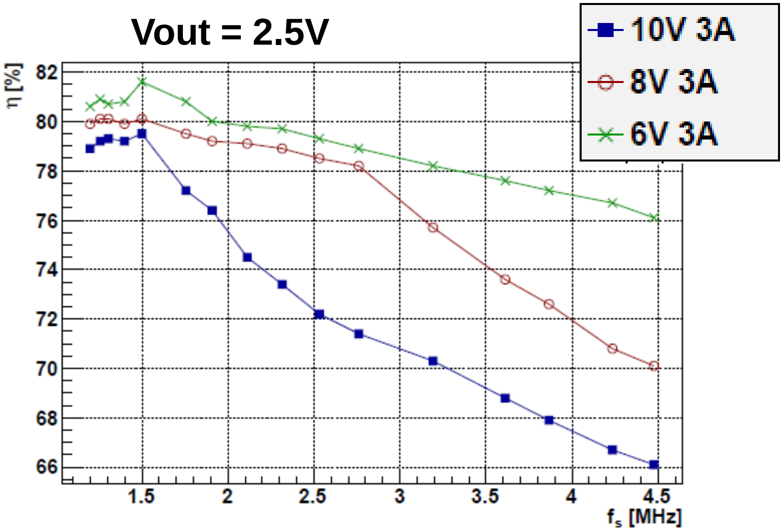


- Mean efficiency and standard deviation based on 12 converters
- Very good efficiency – 80% or higher, except for very low output currents
- Very uniform – SD below or around 0.5%, except for very low output currents (1%)

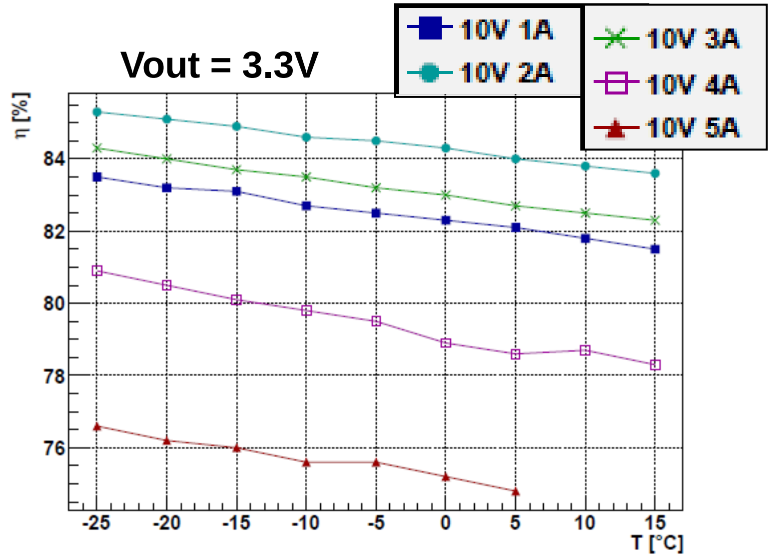
Efficiency vs. f_s and Temperature



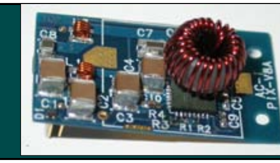
- Switching frequency adjusted with external potentiometer
- **Efficiency is maximal for $f_s \approx$ 1.5MHz**
    - Higher conduction losses for lower f_s
    - Higher switching and driving losses for higher f_s



- Previous measurements with cooling at +20°C
- Efficiency rises with decreasing temperature (lower Ohmic losses)
- **About 0.05% (abs.) increase per K**
- Increase when moving to pixel operating temperatures of -20°C: < 2% (abs.)

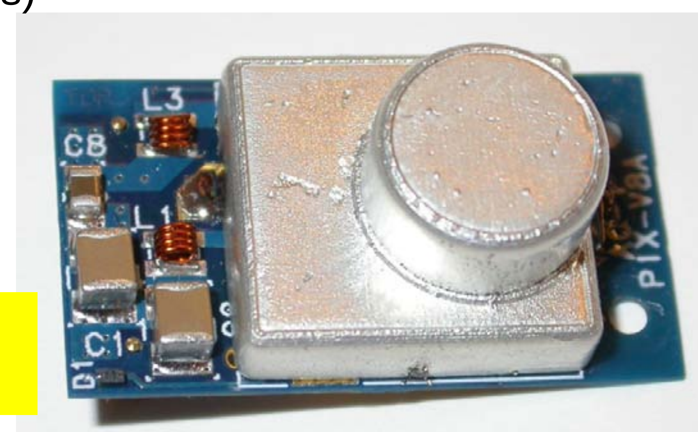


Shielding

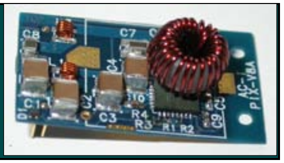


- Space constraints → tricky shape!
- **0.3mm plastic galvanically coated with 30µm Cu + electro-less 1µm Sn**
- Two methods are considered for the body:
  - **Rapid prototyping**: fast and flexible → good for prototyping (and mass production?)
    - Thin layers are difficult (0.3mm still not quite achieved)
    - Radiation hardness to be investigated
    - Price ~ 10 Euro per piece (quote for 3000 pieces)
  - **Injection moulding**: mould is expensive → mass production, when shape is fixed
    - Price ~ 5 Euro per piece (quote for 3000 pieces)

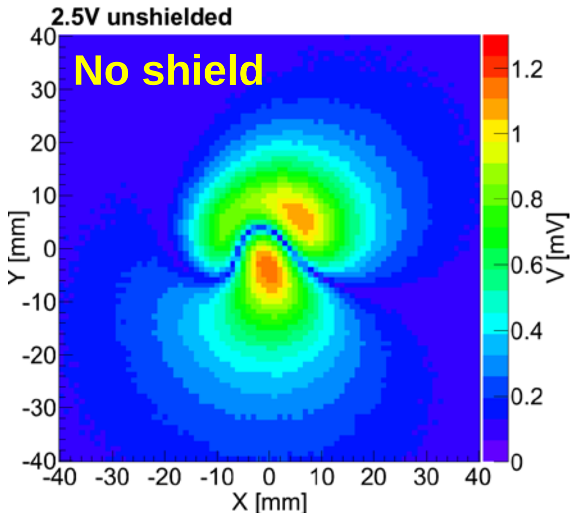
Protoypes made with rapid prototyping



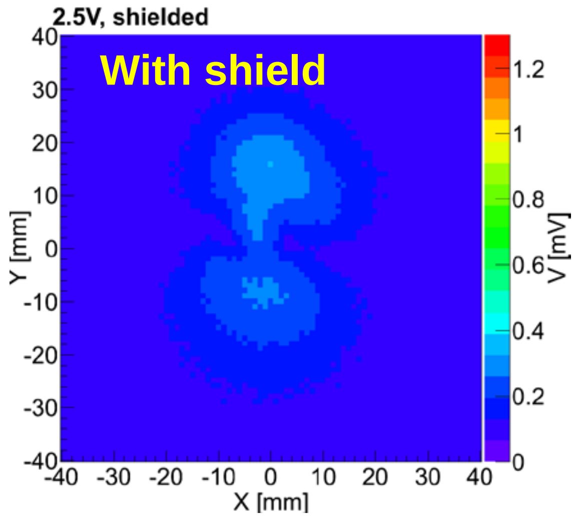
Shielding

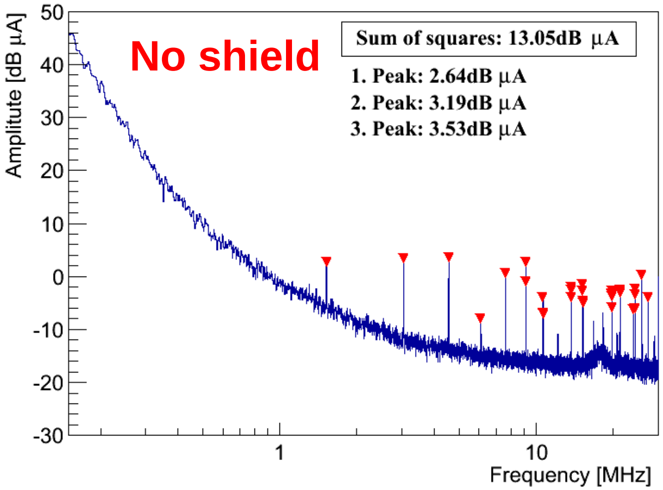


Strong reduction of magnetic emissions and Common Mode output noise:

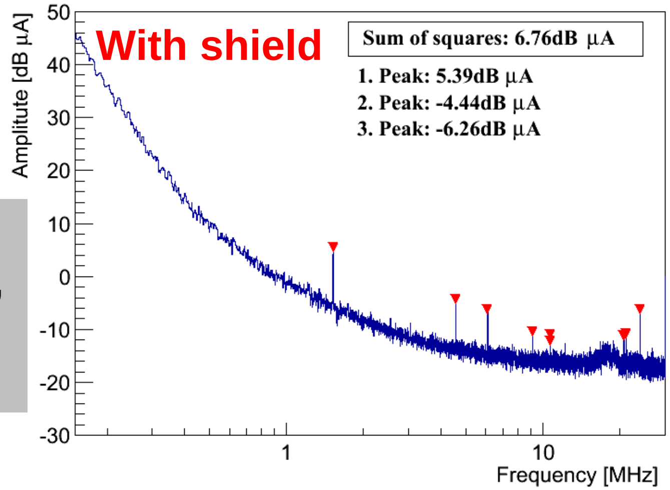


B-field, measured with pick-up probe above coil/shield

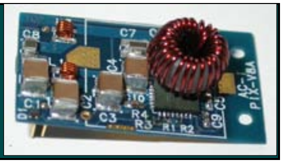


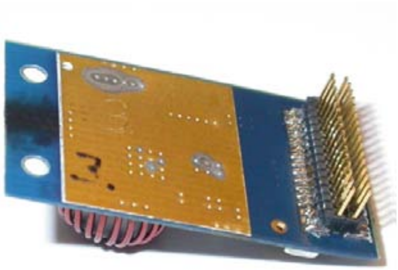


Common Mode output noise spectrum, measured with spectrum analyzer

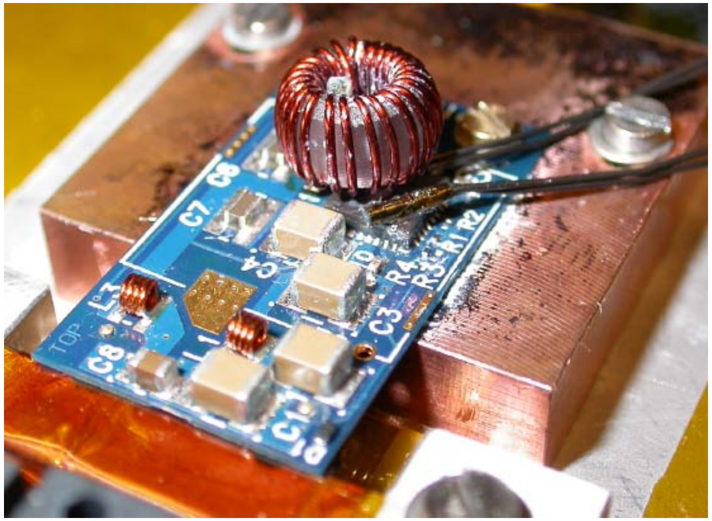


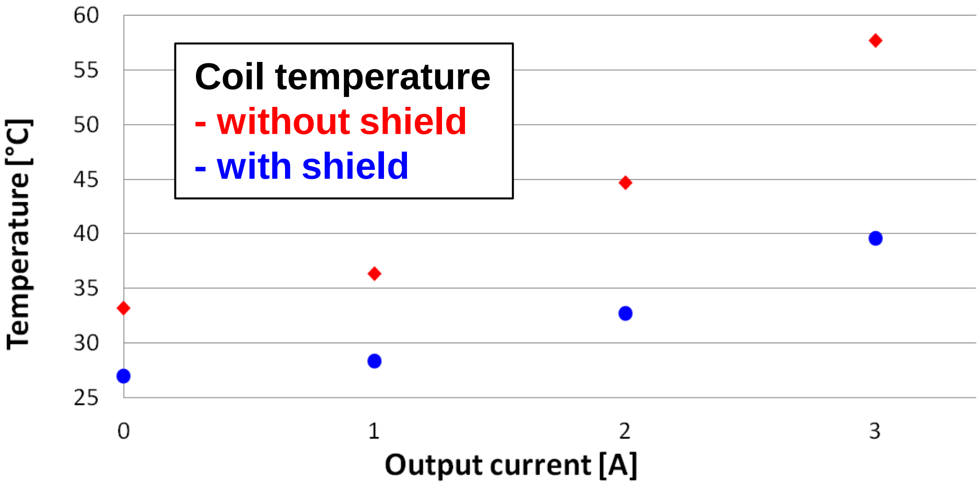
Thermal Studies on Single Converters





- Inefficiency of 20% → converters need to be cooled
- Hot spots: chip and coil
  - Chip cooled from back-side
  - Shield acts as cooling contact for coil
- Measurements with thermistors on chip and inside coil (difficult)
- Shield reduces temperature of inductor by up to ~ 20K





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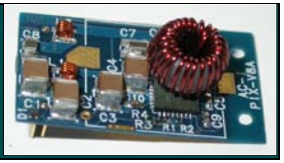
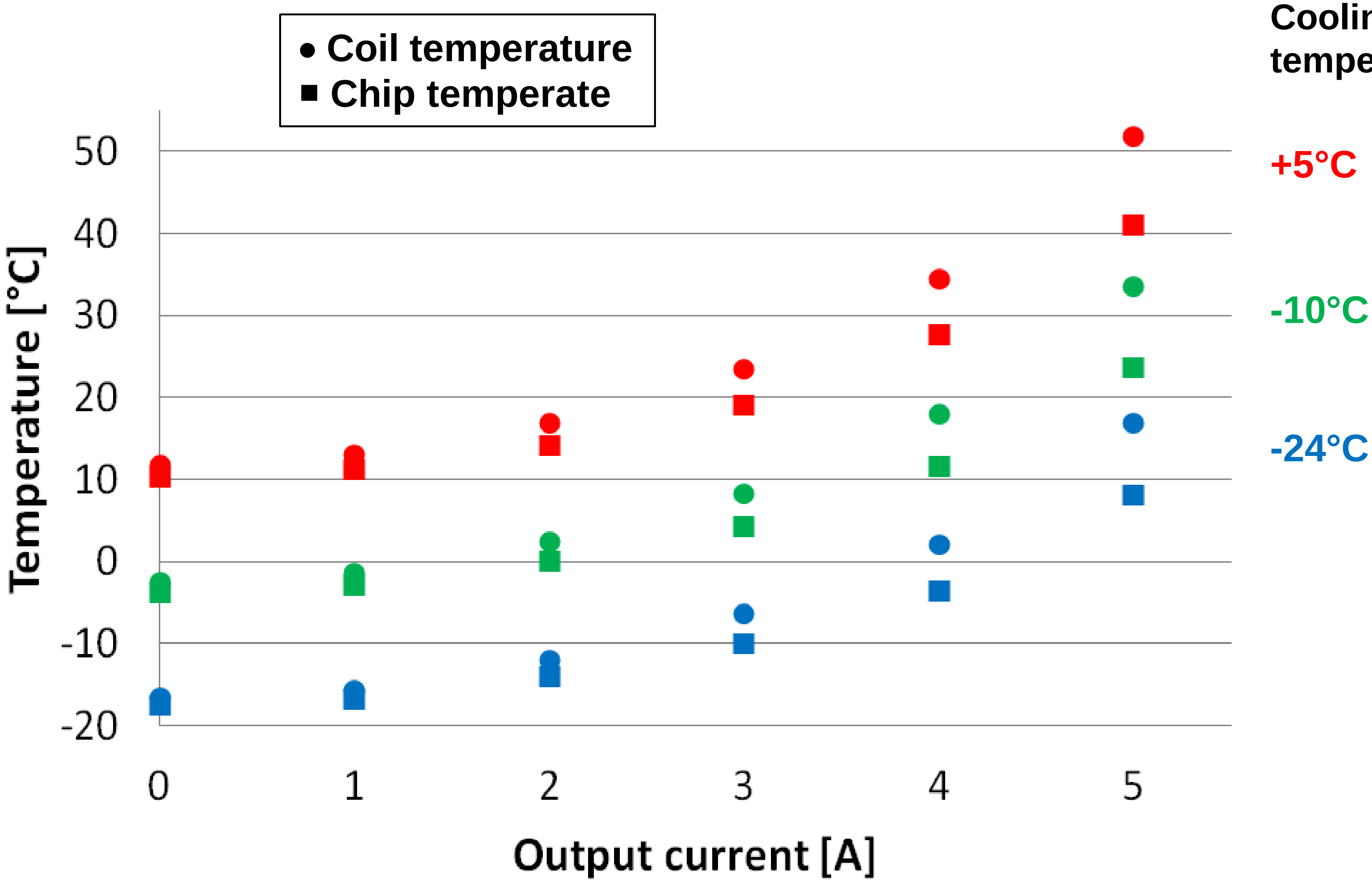
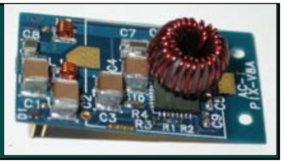
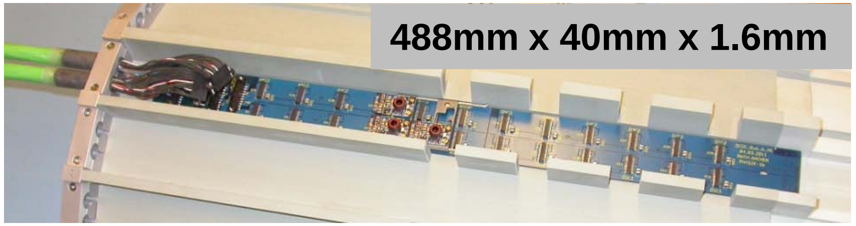


- No thermal problem, even for Iout = 4A

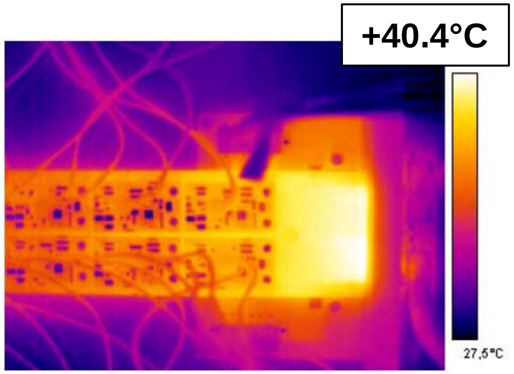


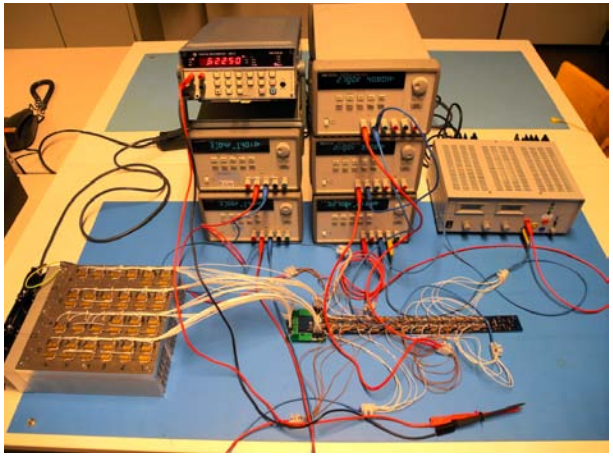
The DC-DC Bus Board

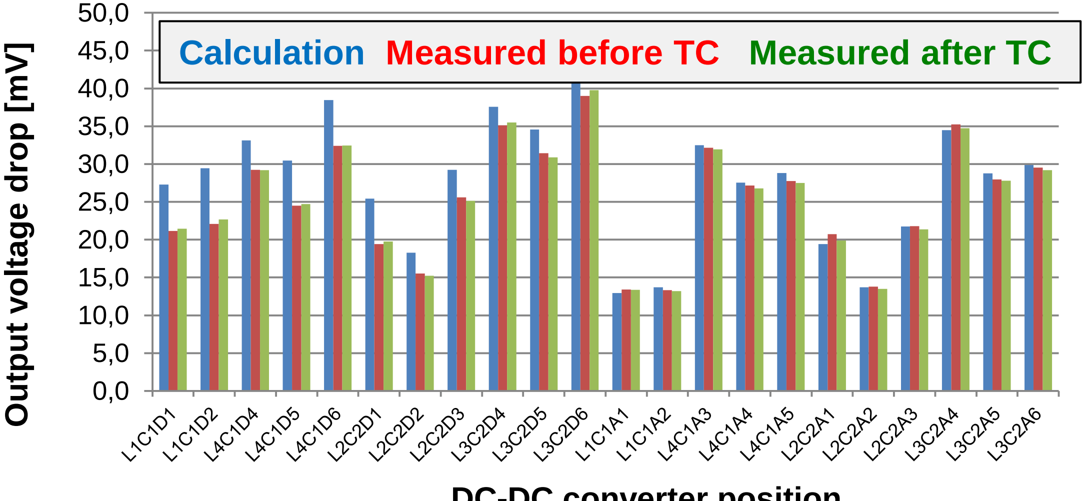




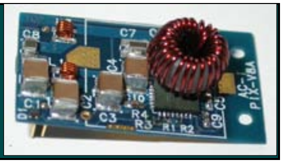
- Input and output voltages, control signals and bias voltages
- 8 Cu layers a 70µm
- Protoype for 24 converters studied
- Voltage drops to be well understood (no remote sensing!)
    - Reasonable agreement with calculation
    - No degradation after 120 thermal cycles between -10°C and +40°C under load





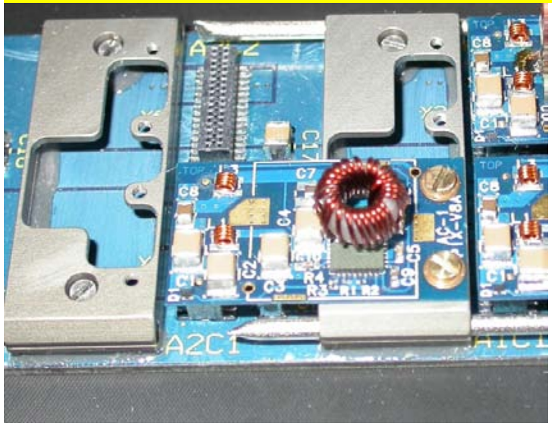


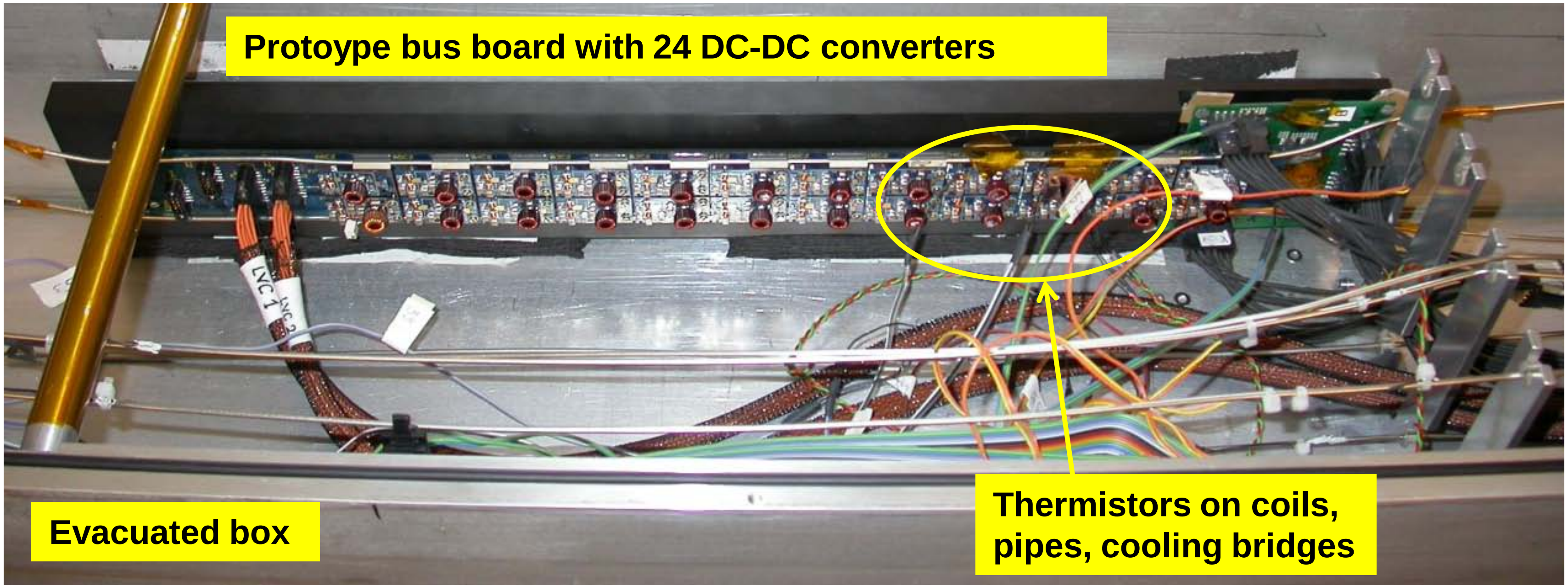
CO_2 Cold Test with Bus Board



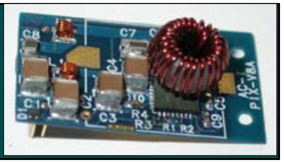
- Two-phase CO_2 cooling system
- Tests performed with fully equipped bus board and lab CO_2 cooling system, operated at -20°C
- Pipes are thin: 1.7/2.0 mm in lab; 1.8/2.2mm in CMS
- A programmable load can be applied to each converter

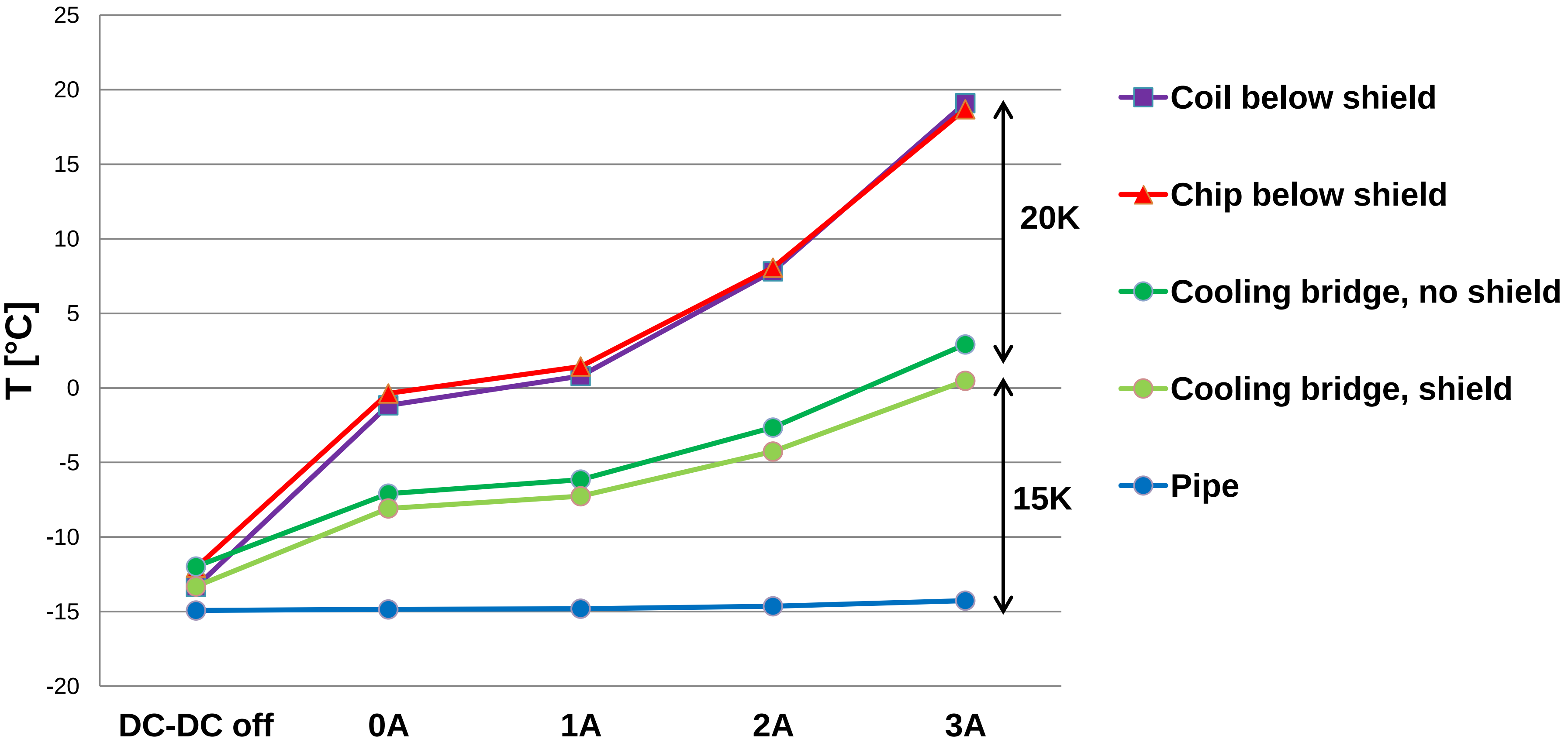
Aluminium cooling bridges





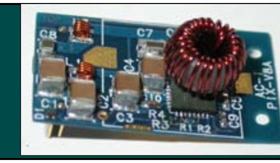
CO_2 Cold Test with Bus Board



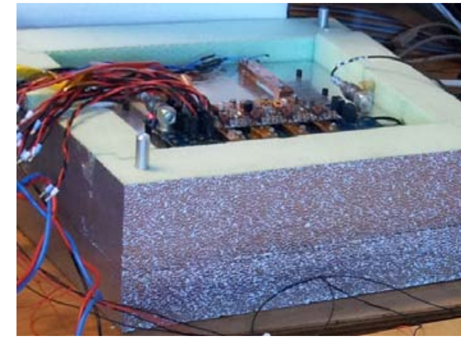


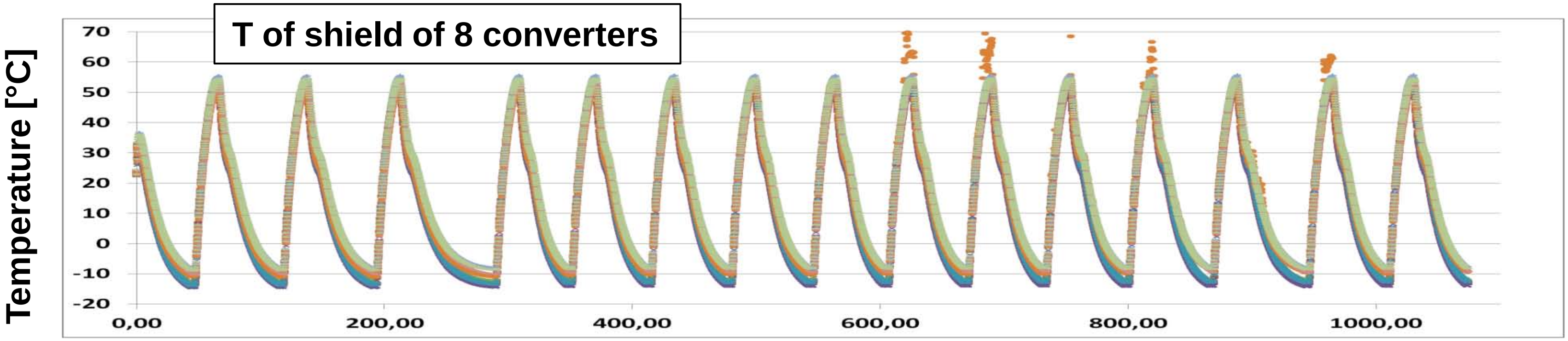
- ΔT between pipe and cooling bridge about 15K → optimization needed
- ΔT betw. coil/chip of shielded converter & cooling bridge about 20K → as expected

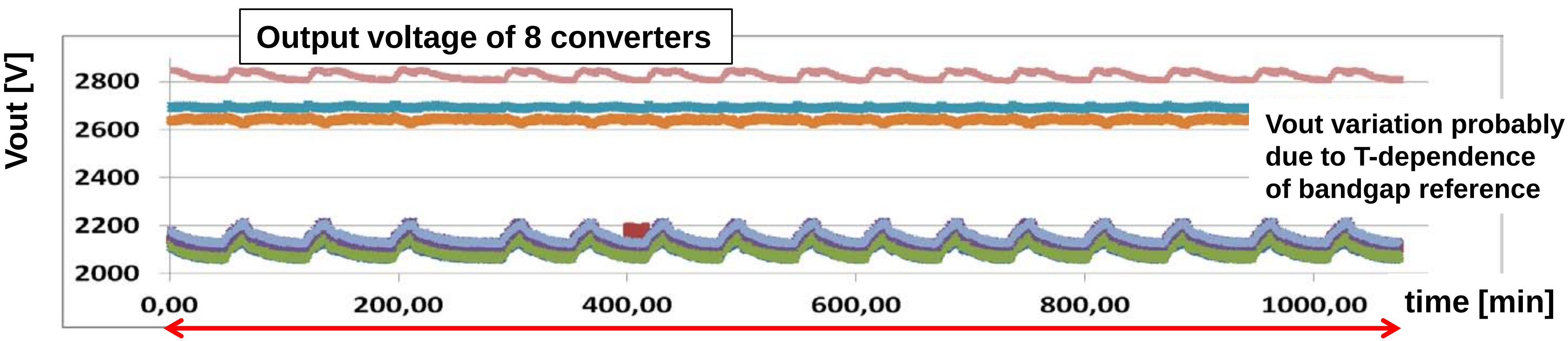
Thermal Cycling



- Different temperatures in CMS: CO_2 cold/warm; power on/off
  - ✓ check if convs. work between -30°C and +35°C block temp.
  - ✓ impose thermal stress (accelerated aging)
- Cold box for 16 DC-DC converters
- 8 converters exposed to 15 cycles → still working fine

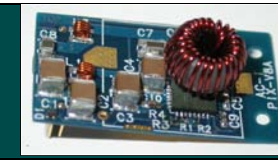




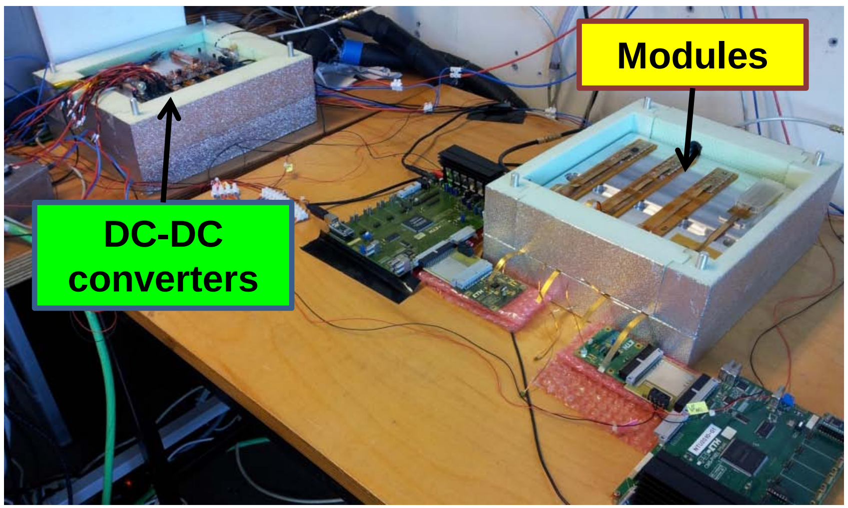


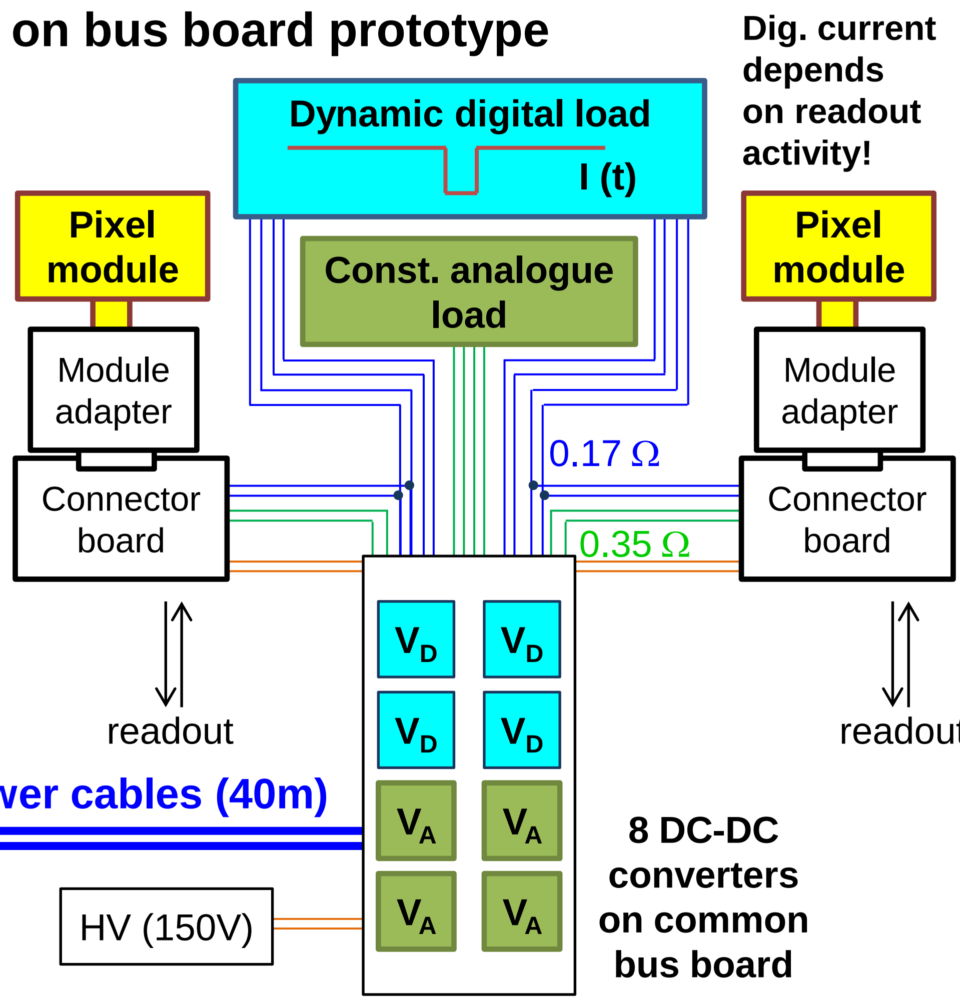
17h

System Tests with Pixel Modules

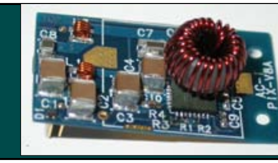


- Check for possible degradation of module performance due to DC-DC converters
- **2 (present-type) pixel modules powered from 1 converter pair**
- **In total 8 pairs of DC-DC converters on bus board prototype**



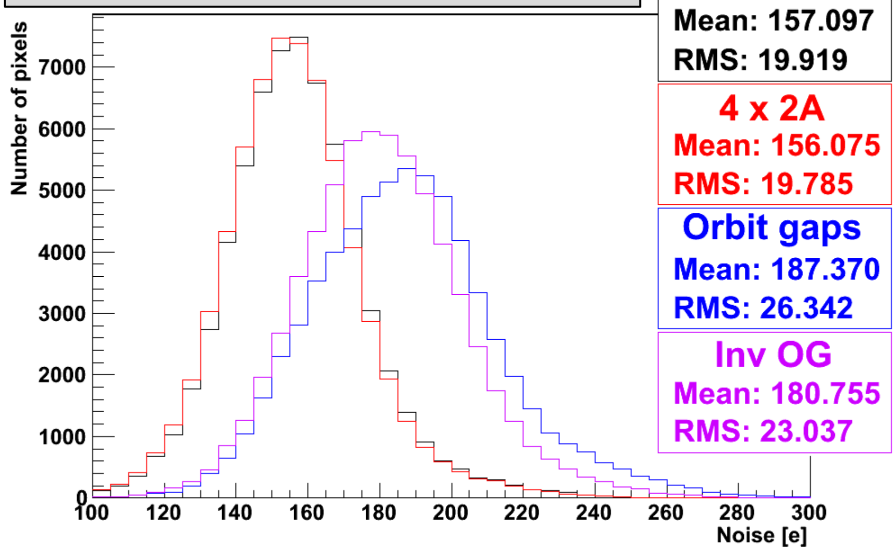


System Tests with Pixel Modules

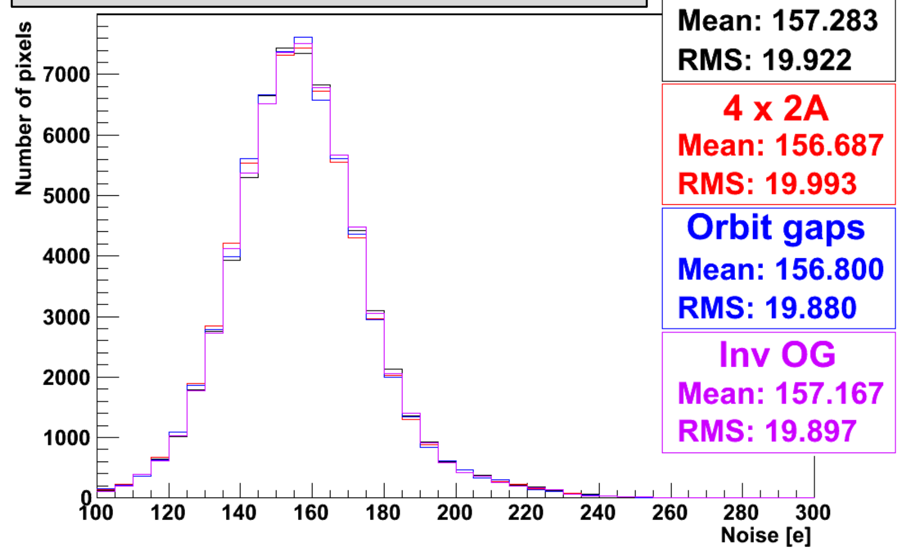


- Noise of each pixel is extracted as width of its “S-curve“
- Comparison betw. conventional powering with CAEN PS and DC-DC powering
  - No difference observed for constant load
  - For dynamic load changes, noise with conv. powering increases by 19 and 15%
  - **DC-DC converters increase robustness, due to local regulation and filtering**

Conventional powering (CAEN)



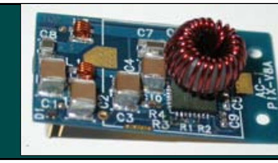
DC-DC conversion powering



Load from pixel modules only
Constant nominal load on all converters

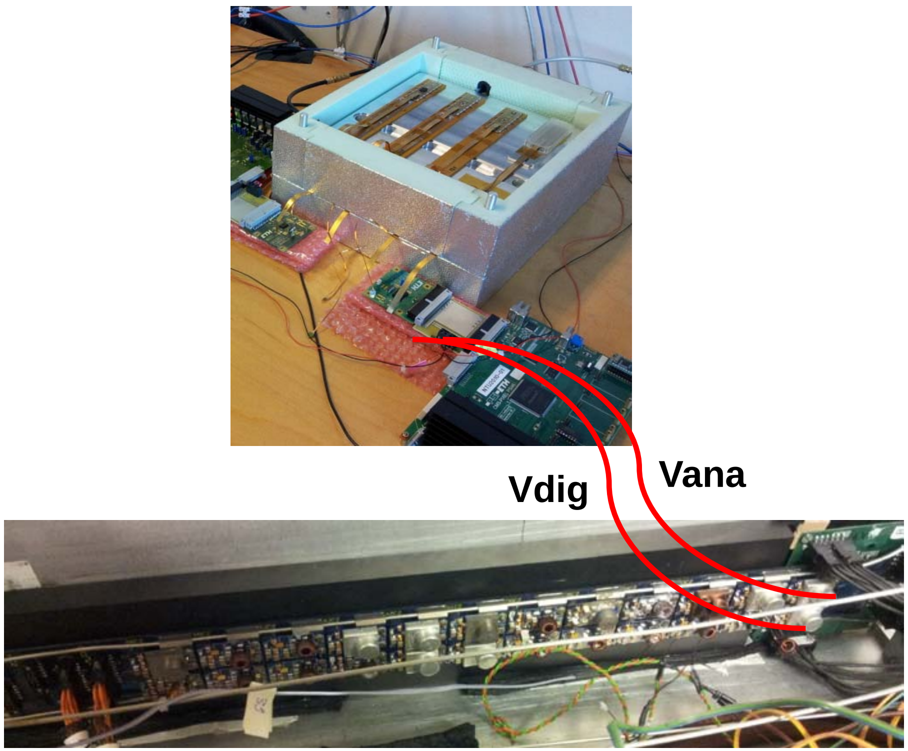
Load changes as expected from LHC orbit gaps
→ drop from 2A to 0A for 3μs every 89μs
Inverted orbit gaps (few filled bunches in LHC)

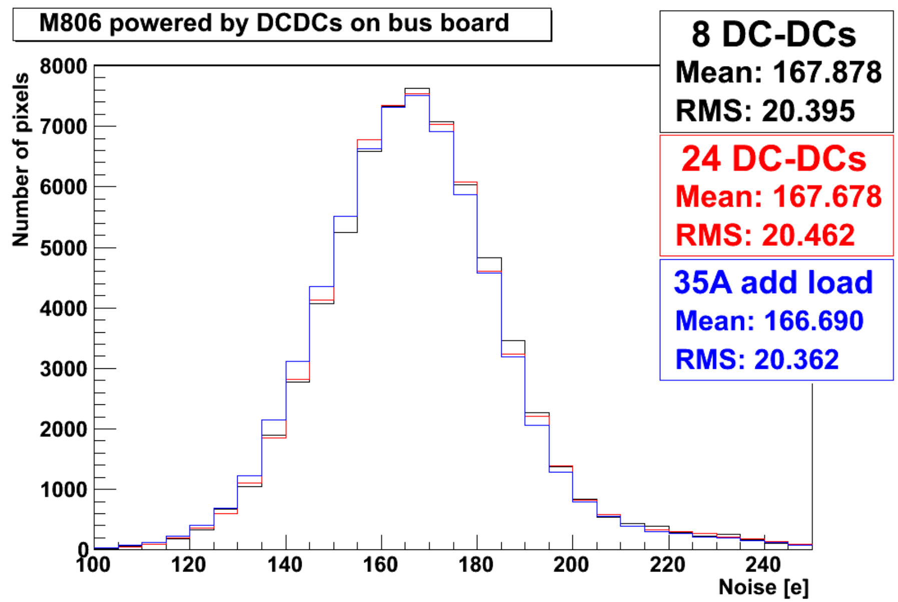
System Tests with Pixel Modules



- 24 DC-DC converters on bus board
- Two pixel modules powered from one converter pair
- 3A load on all analog converters → 35A

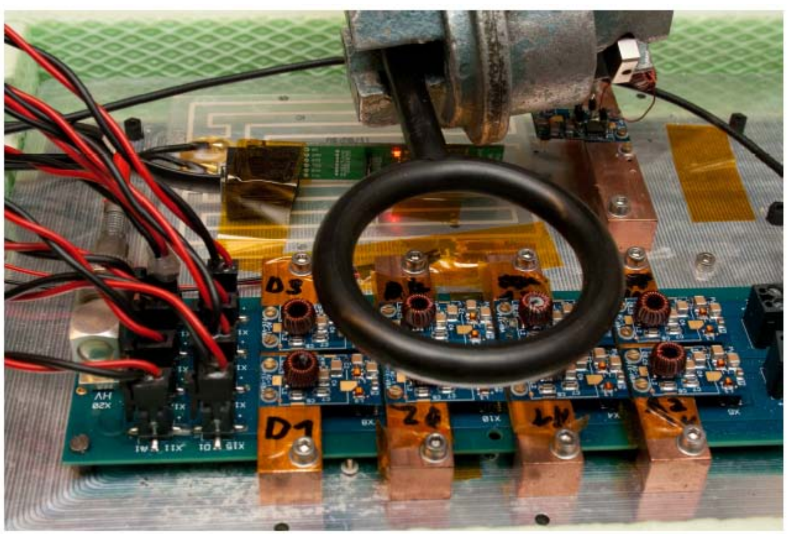
→ No increase of pixel noise wrt 8 DC-DC converters



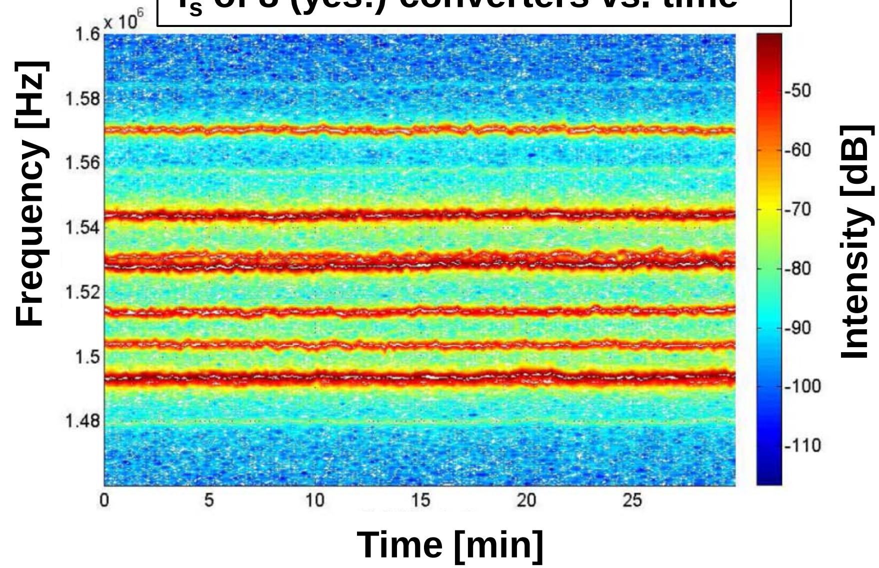


Synchronisation of DC-DC Converters

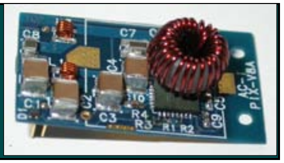
- **Depending on their coupling, oscillators can lock in frequency and phase**
  - Described by the Kuramoto model
  - Many examples in nature: e.g. mechanically coupled metronoms
- Coupling of DC-DC converters on common power line might increase input noise
- **Idea: try to see/induce coupling, and try to change f_s through disturbations**
  - f_s measured with pick-up probe and spectrum analyzer
  - relative phase measured with oscilloscope



f_s of 8 (yes!) converters vs. time

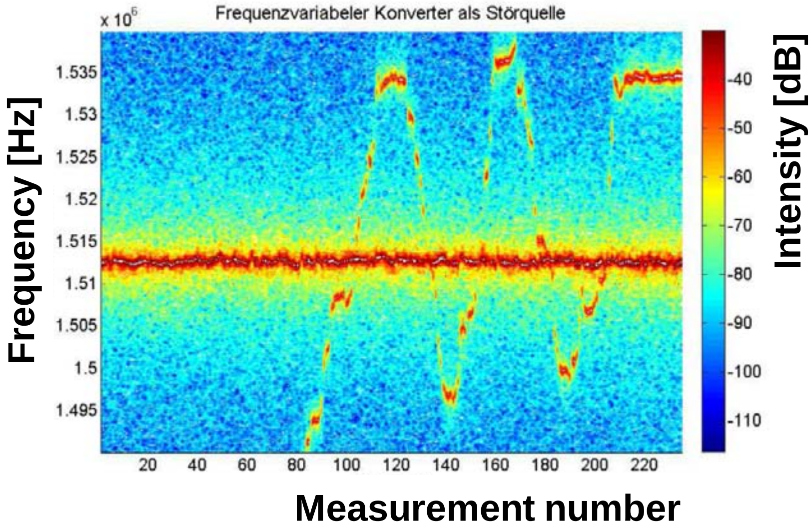


Synchronisation of DC-DC Converters



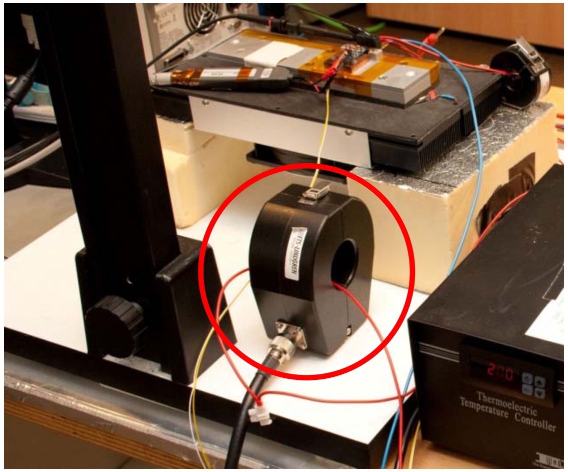
- Two converters operated
  - f_s of one converter adjustable with poti
  - Check effect on the other converter

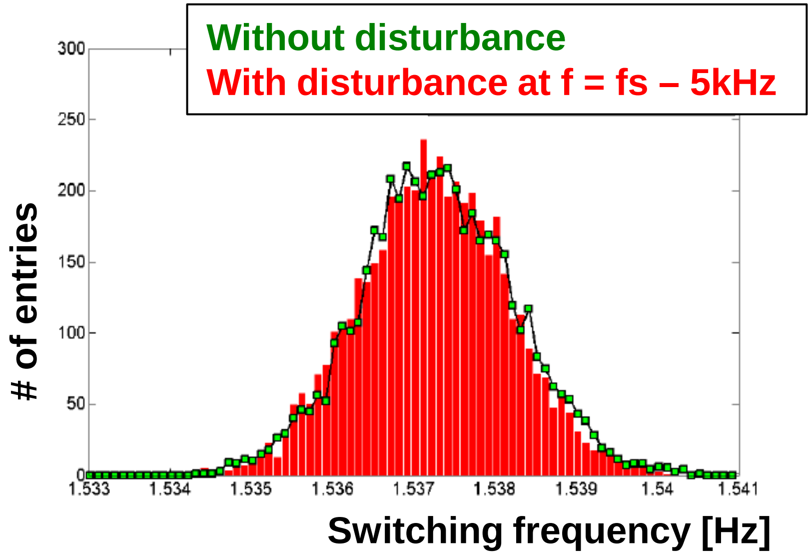
→ no f_s shift or phase locking observed



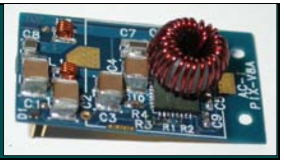
- External disturbation
  - conductive: on input cable ($740mV_{pp}$)
  - radiative: with external coil (~10mW)

→ no significant changes in the frequency distribution of converter observed





Conclusions & Outlook

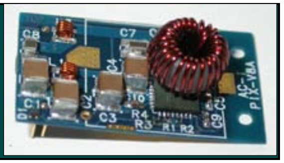


- DC-DC conversion will be used in the CMS Phase-1 pixel upgrade
- DC-DC buck converters based on AMIS4 ASIC extensively tested
  - ✓ Efficieny uniform and high - around 80%
  - ✓ System tests with pixel modules show no degradation
- First system tests with a fully equipped bus board were successfull
- Started to investigate industrialization options and to prepare QA set-ups

- Move to AMIS5 ASIC in Autumn
- Mass production in 2013/2014

Back-up Slides

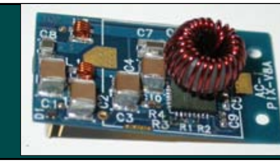
Specification of DC-DC Converters

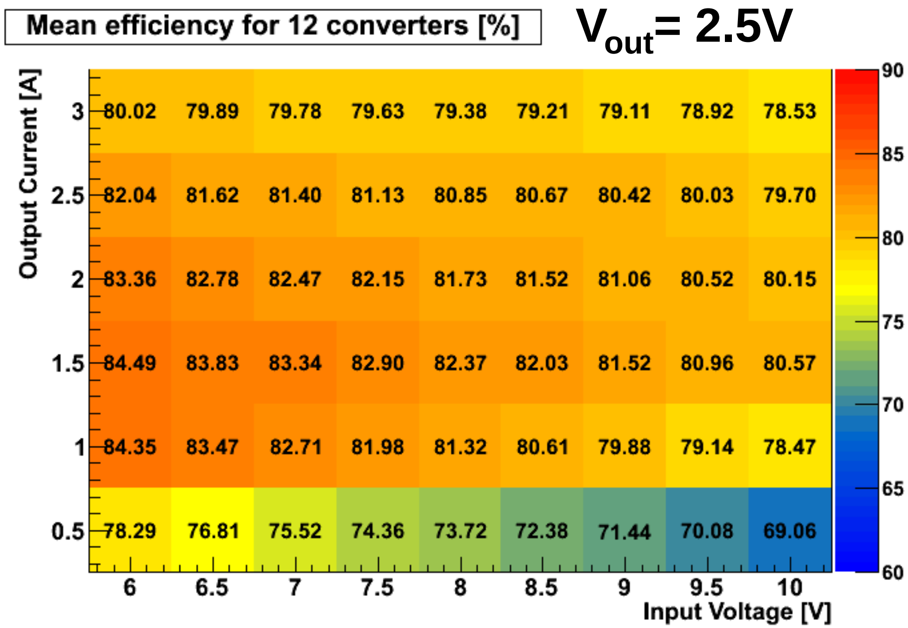


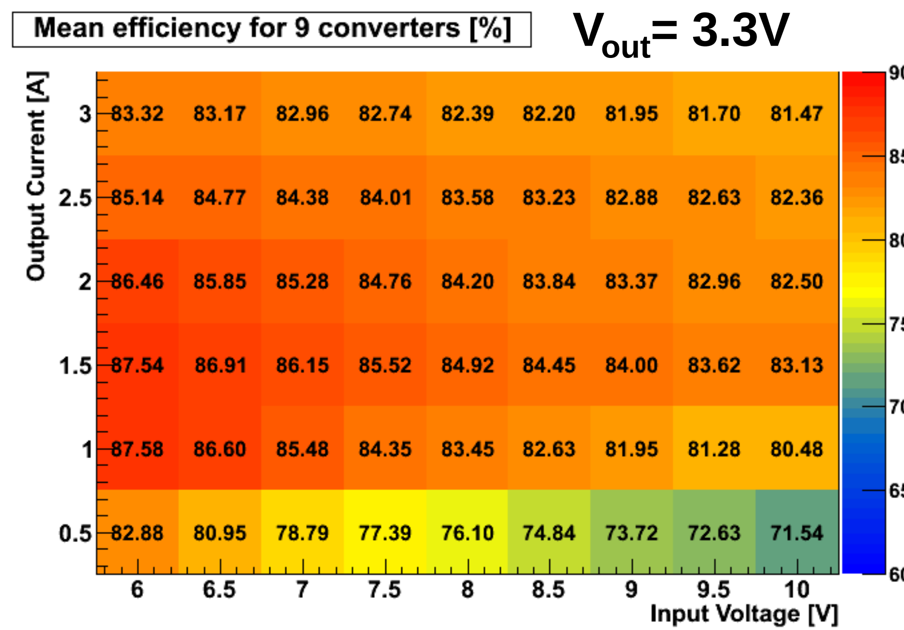
Input voltage	9-10 V
Output voltage	2.4-2.5 V or 3.0-3.3 V
Conversion ratio	3-4
Maximum output current	3-4 A
Efficiency	At least 75%, at nominal operating conditions
Maximal dimensions	3.0 cm x 2.0 cm x 1.4 cm
Radiation tolerance (500 fb^{-1})	100 kGy and 2×10^{14} n_{eq}/cm^2
Protection features	Over-temperature, over-current and under-voltage protection
Control features	Remote disabling and status information
Special requirements	Stable operation under large and fast load variations
Total number required	1184
Total number including spares	1800

Table 7.3: Specifications for DC-DC converters for the CMS pixel upgrade.

Power Efficiency

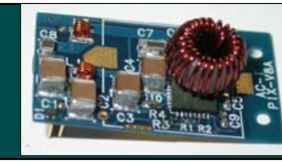


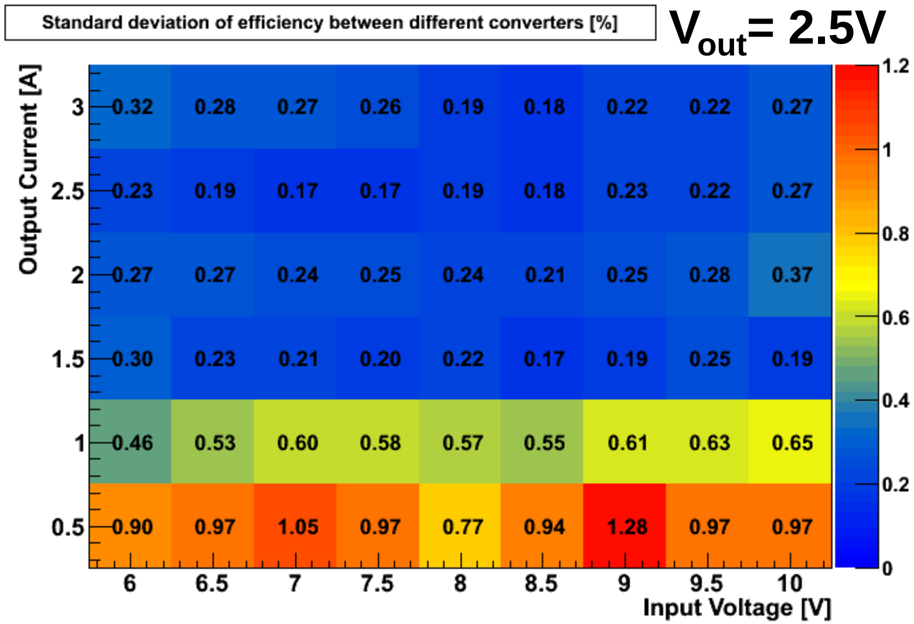


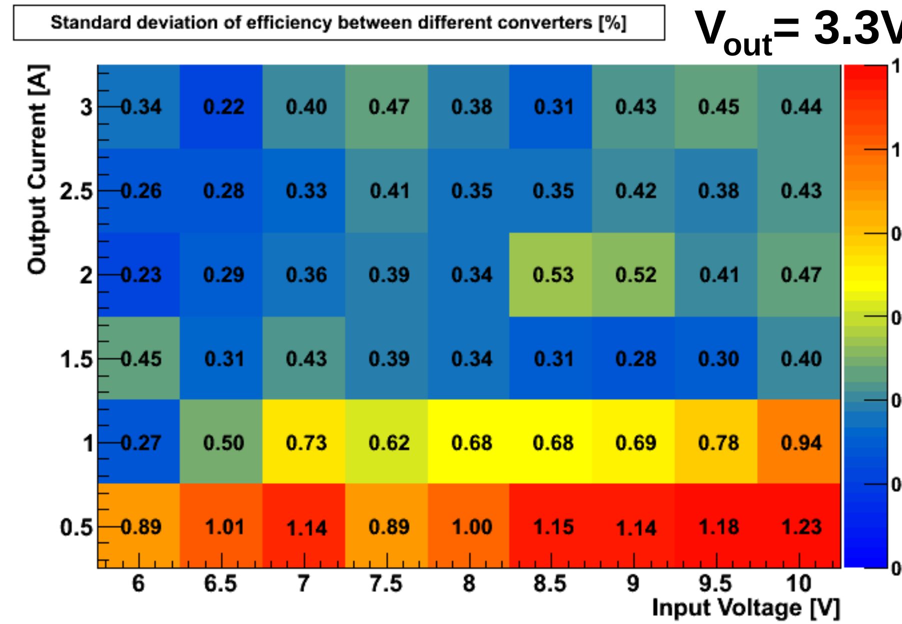


- Mean efficiency is shown based on 12 and 9 converters, respectively
- Very good efficiency – 80% or higher, except for very low output currents

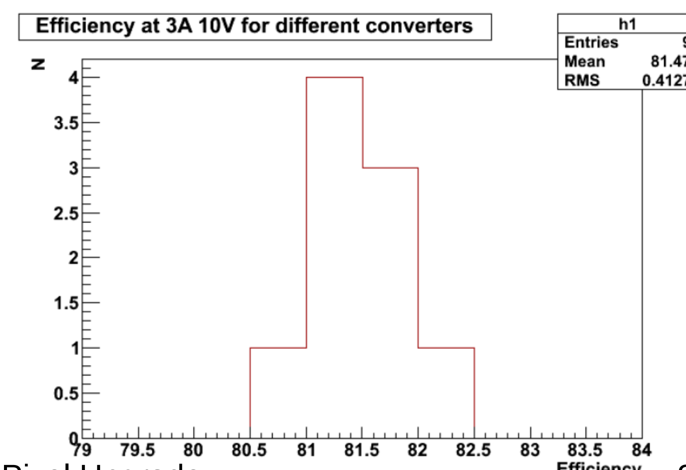
Uniformity of Power Efficiency



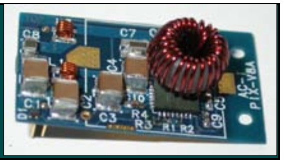




- Standard deviation is shown based on 12 and 9 converters, respectively
- Very uniform – with SD below or around 0.5%, except for very low output currents (1%)



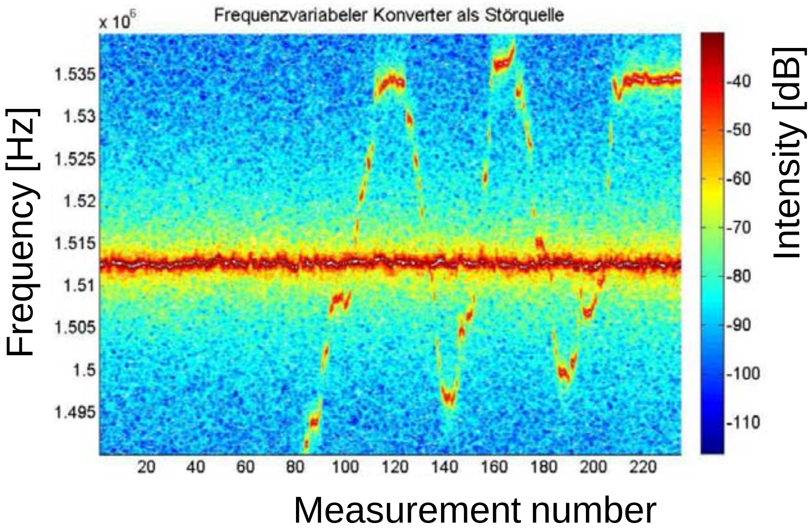
Coupling of DC-DC Converters

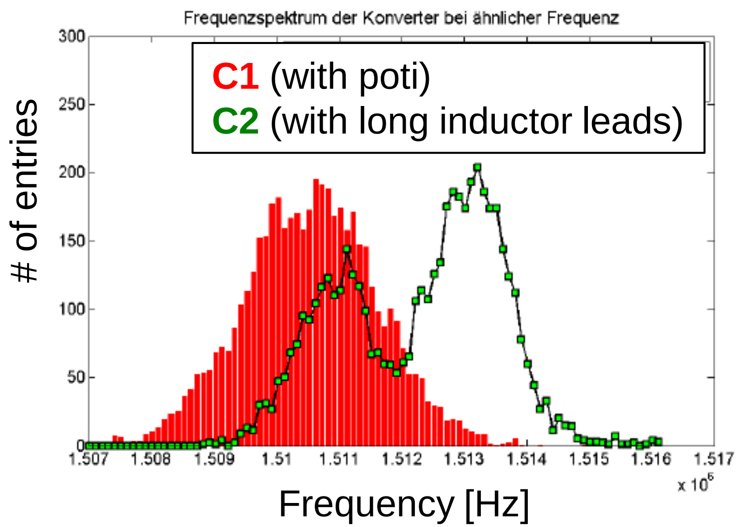


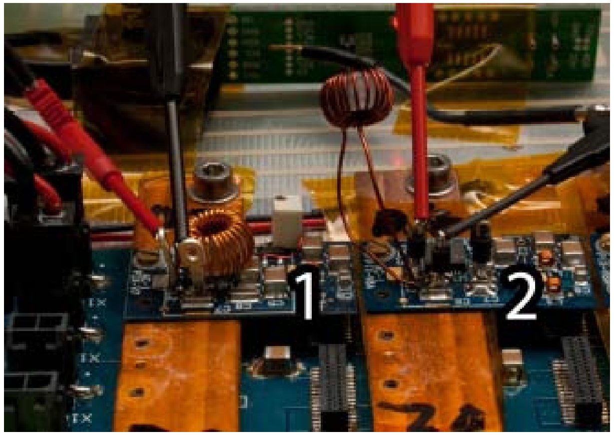
- Two converters operated: “C1“ and “C2“
  - C1: f_s adjustable with potentiometer
  - Check effect on C2 = DUT

→ no f_s shift or phase locking observed

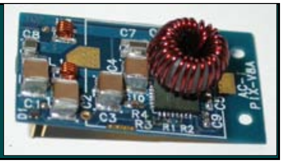
- However, under special, unrealistic circumstances converters do couple
  - C1 with poti, C2 with long inductor leads
  - f_s of C1 slightly detuned → jumps to f_s of C2
  - Phase-locking observed as well







Coupling of DC-DC Converters



Interference induced on input cable (740mV$_{pp}$) and with external coil (~10mW)
→ no significant changes in the frequency distribution (5000 measurements) of DUT