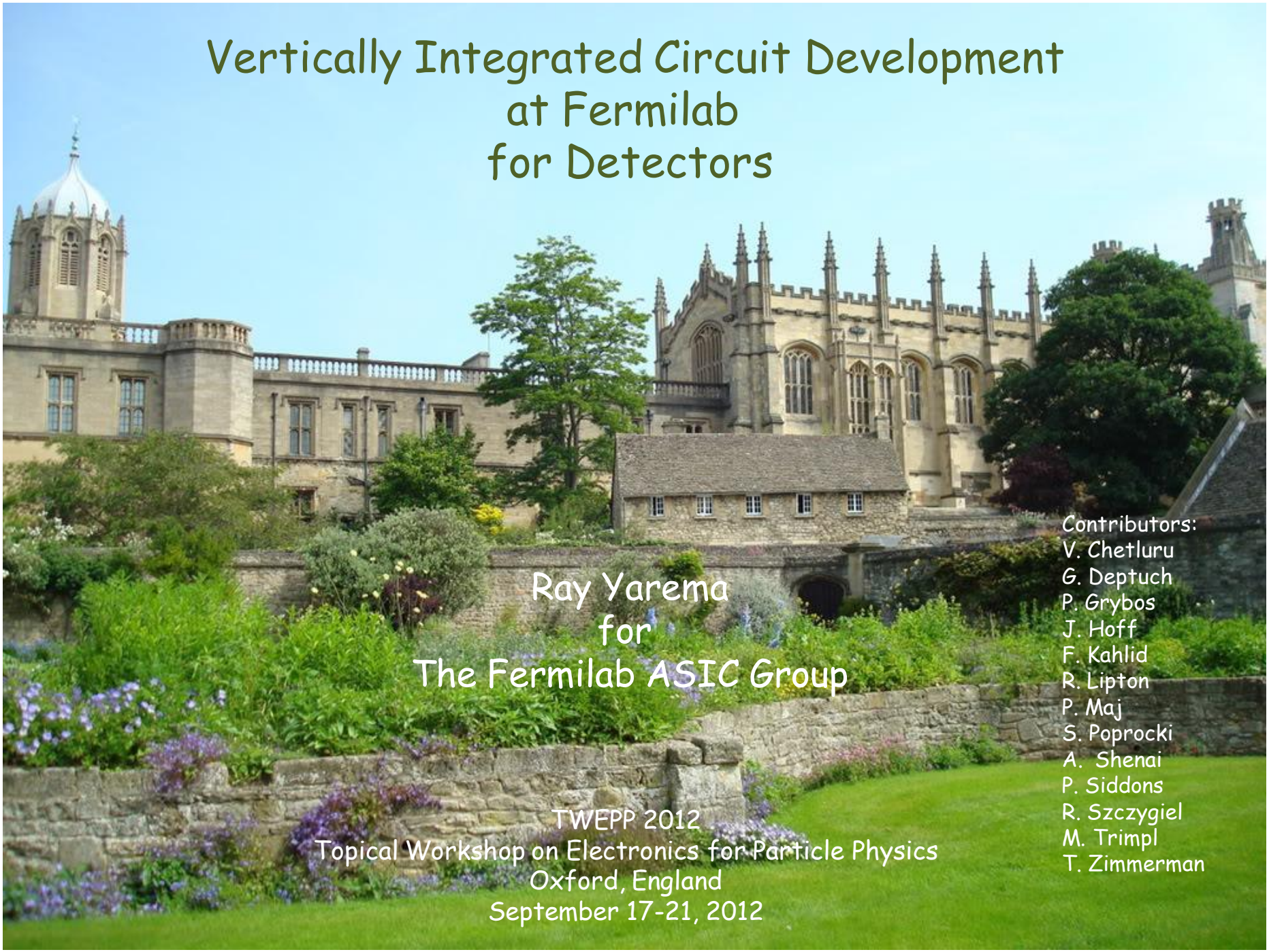
Vertically Integrated Circuit Development at Fermilab for Detectors



Ray Yarema
for
The Fermilab ASIC Group

Contributors:
V. Chetluru
G. Deptuch
P. Grybos
J. Hoff
F. Kahlid
R. Lipton
P. Maj
S. Poprocki
A. Shenai
P. Siddons
R. Szczygiel
M. Trimpl
T. Zimmerman

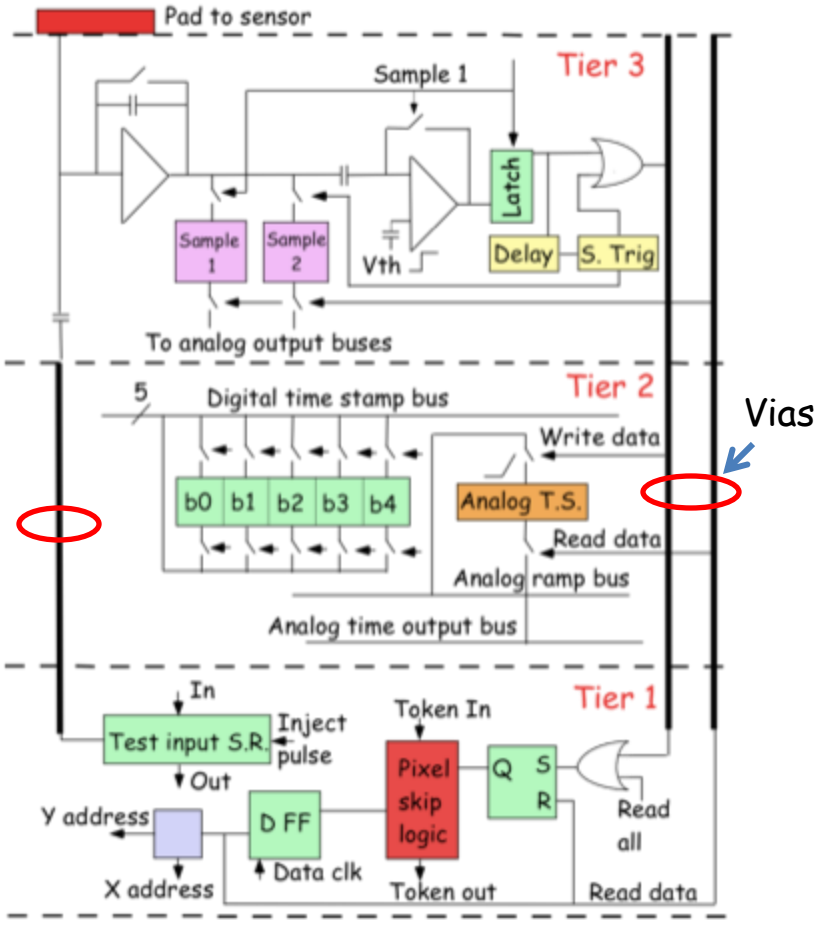
TWEPP 2012
Topical Workshop on Electronics for Particle Physics
Oxford, England
September 17-21, 2012

Introduction

- The inspiration to develop 3D integrated circuits for HEP began a few years ago at Fermilab. The idea of bonding layers of thin readout circuitry and detectors without conventional bump bonds was appealing. We thought that 3D could open the doors to new concepts and significant improvements for detector electronics.
  - Finer pitch pixels
  - Less mass
  - Higher localized on detector functionality
  - Bump bond alternative
  - Non dead space arrays
- Although the 3D technologies were in the relatively early stages of development, we thought the potential benefits were worth the R&D effort. Due to a series of delays and problems which were beyond our control, it soon became clear that we had seriously underestimated the effort required.
- Although the effort has been often frustrating, some positive results can be reported.
- This talk will provide a quick overview of our 3D activities
  - Early history
  - Processes used
  - Major problems
  - Present 3D circuit designs
  - Test results
  - Future including 3D designs

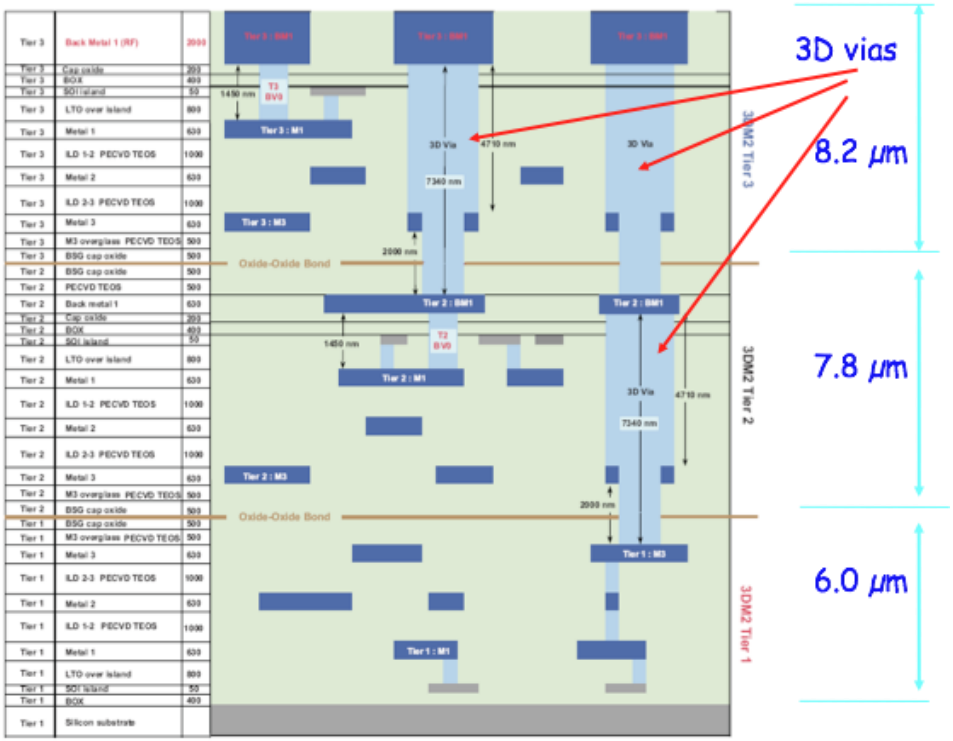
Early History: Design for MIT LL 3D Process

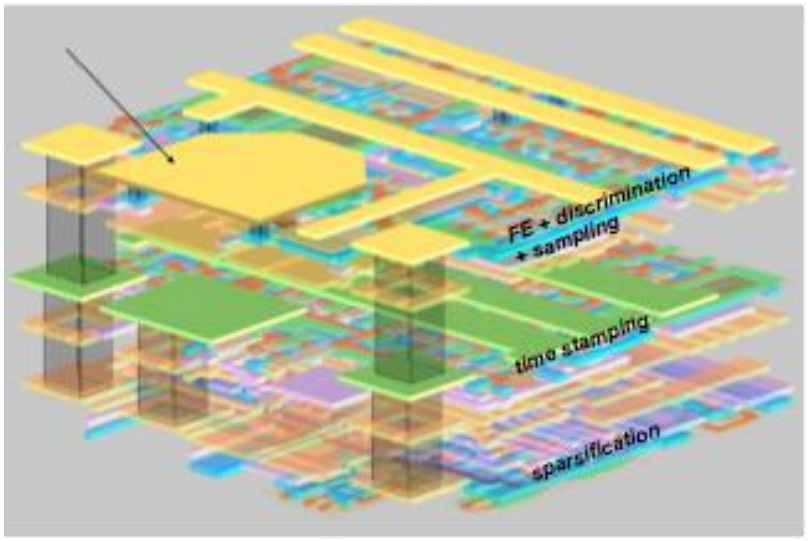
- Our initial 3D design used MIT LL 3D SOI process with 0.18 um features. [1]
- First run had serious processing problems resulting in near zero yield.
- Design was made more conservative and resubmitted.
- Second submission produced better yield and functioning chips.
- Runs funded by DARPA
- Full function 3-tier chip for ILC pixel detector, main features:
  - 64x64 array
  - 20 um (VIP1), 24 um (VIP2a) pitch
  - Digital and analog time stamp circuitry
  - Data sparsification with high speed look ahead for next hit.
  - Pixel analog information output along with time stamp.



Single ILC pixel schematic divided into 3 tiers

MIT LL 3D Process





3D view of an ILC pixel cell showing the 3 tiers and the vias between the tiers.

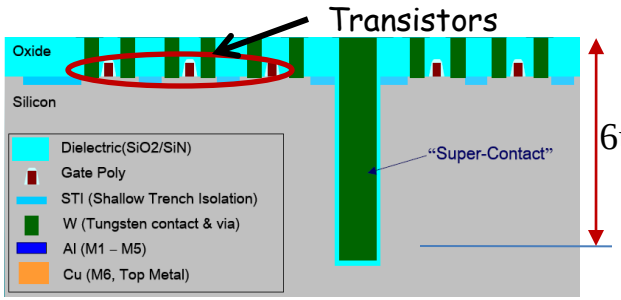
Cross-sectional view of MIT process using oxide bonding on a 3 tier assembly. Top 2 layers are about 8 um thick with 1.2 um vias inserted using a via last process (vias inserted after bonding).

*No problems were identified with the vias during the testing.
*Further work was stopped due to concern about the radiation tolerance and analog performance of the SOI process.

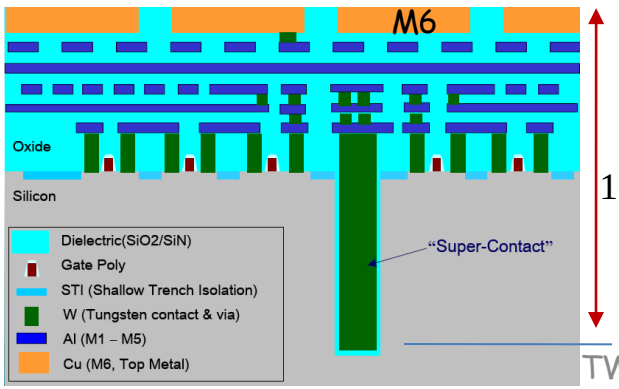
Move to 0.13 um CMOS Process at Global (Chartered) Foundries

- Access to Global foundry thru Tezzaron
- After fabrication of transistors 1 um dia, 6 um deep, blind vias (super contact) inserted (via middle process).
- Super contact filled with tungsten at same time connections are made to transistors.
- BEOL, M1-M6 completed.
- M6 used to make pads for W2W bonding.

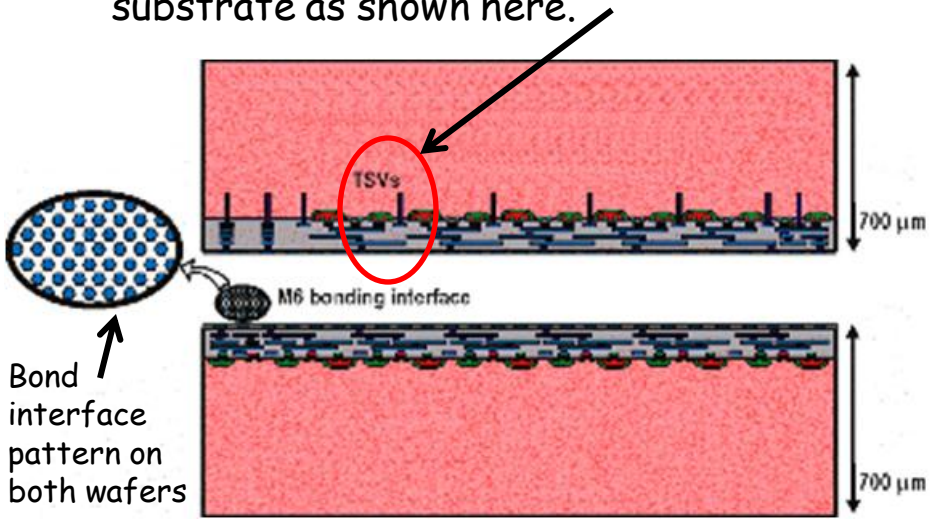
After FEOL fabricate 6 um super contact (via)



Complete BEOL processing



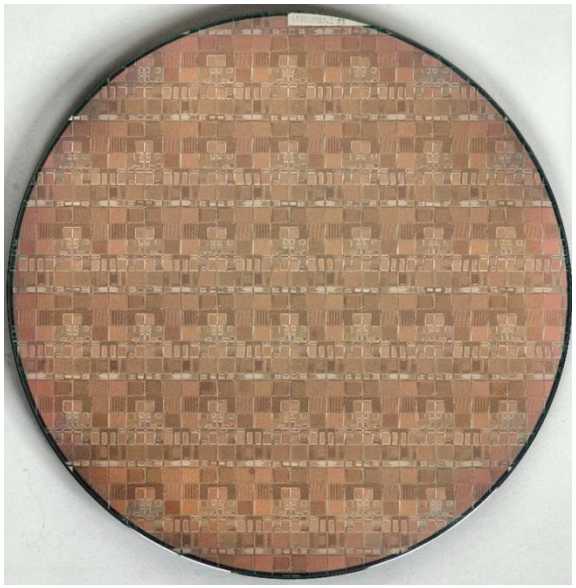
- Very regular pattern of M6 copper bond pads is critical.
- Copper bond pitch is about 4 um
- In 2 tier chip, the wafers are bonded face-to-face with vias pointing into the substrate as shown here.



Bond interface pattern on both wafers

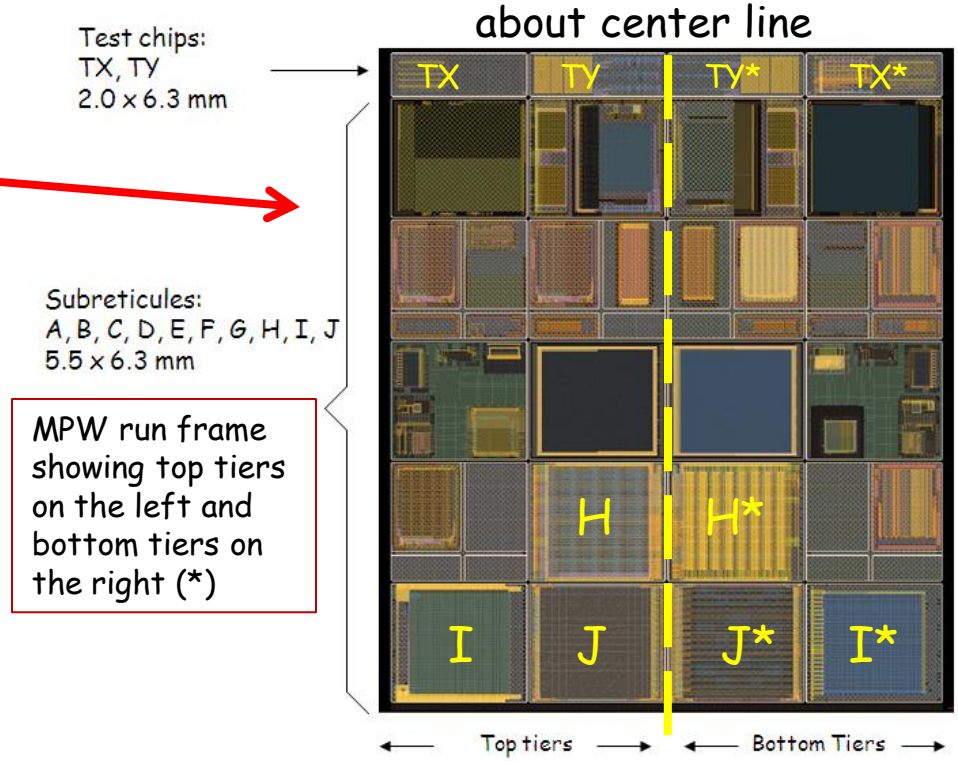
Global foundry Multi-Project Run

- Multi-project run submitted to GF through Tezzaron with numerous designs from 3D consortium.
- One set of masks used for 2 tier 3D circuits.
- Frame divided into 24 subreticules. 12 for top tier and 12 for bottom tier.
- Intended for wafer face to face bonding.
- Produces both normal and reversed designs.
- Designs contributed by France, Italy, Germany, Poland and the US.



Eight inch wafer

Frame show symmetry about center line

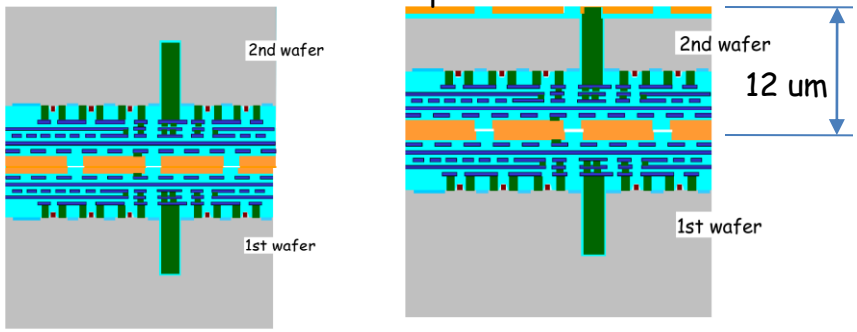


Fermilab designs:
H: VICTR – pixel readout chip mating to two sensors for track trigger in CMS
I: VIP2b – ILC pixel chip with time stamping and sparcification (2 tier version of MIT design)
J: VIPIC – fast frame readout chip for X-ray Photon Correlation Spectroscopy at a light source
TX and TY : test chips

Numerous Problems Encountered

- Design and submission issues [2]
- Fabrication issues
  - Chartered bought by Global
  - Flip-flopped on decision to stop 3D processing on 130nm
  - Knowledgeable foundry personnel lost
  - Full lot of wafers lost due to improper frame placement (1.2 mm off center)
  - New lot re-fabricated

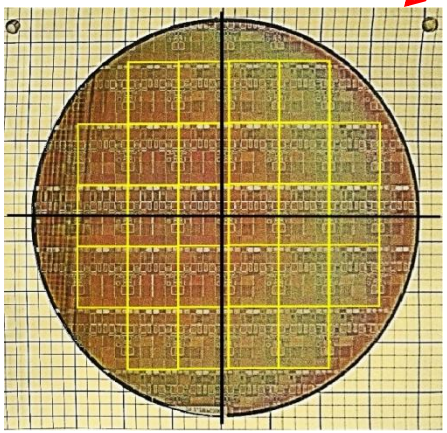
Tezzaron bond process



Flip wafer and bond

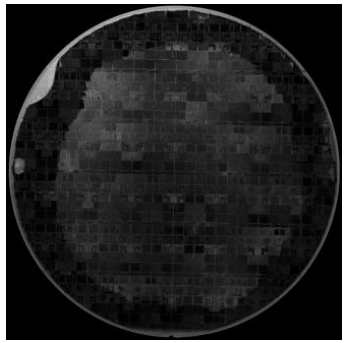
Thin wafer to 12um, add metal

1.2 mm



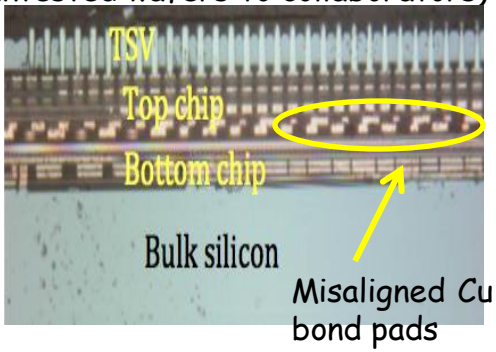
Frames not placed symmetrically about wafer center line – prohibits bonding due to bonder limitations.

First 6 wafers bonded at EVG Tempe, lost due to residual carbon layer



Bonded wafer acoustic image (light sections show poor bonds).Poor bonding may be also due to lack of forming gas [3] in Tempe bonder.

Second 6 wafers bonded at EVG Tempe lost due to misalignment (mistake to send untested wafers to collaborators)



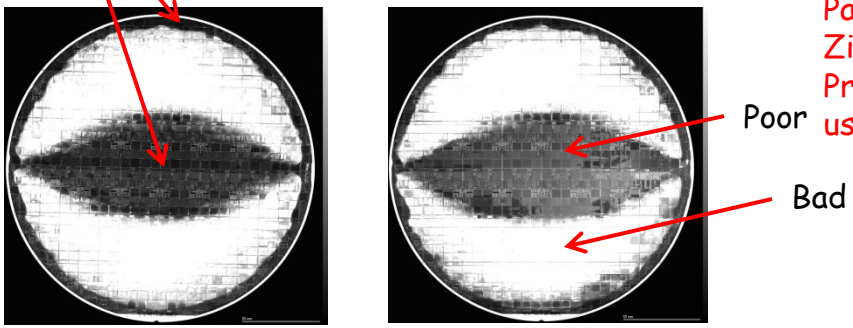
Decision made to bond remaining wafers at EVG Austria due to different wafer alignment process and use of forming gas.

- Bonding started on new lot using Tezzaron Cu-cu bond process
  - Etch surface oxide exposing Cu bond pad (350 nm high)
  - Align for face to face bonding
  - Cu-Cu thermo compression bond
  - Thin one side to expose vias
  - Add metalization for bond pads

Latest Wafer Bonding Results

- Remaining 16 wafers sent to EVG Austria for bonding.
  - Initially 8 wafers would not bond
    - Tried many bond pressures with forming gas.
    - Attributed to larger copper grain boundaries which have been found to develop over time. (Documented by Tezzaron). Wafers were "old".
  - Next 8 wafers sent to Ziptronix for bond pad processing and then sent back to Austria
    - 1 wafer pair broke in the EVG bonder at high pressure
    - 3 remaining wafer pairs exhibited poor bonding due to trapped gas.
      - Cu bond pads insufficiently exposed during etch process.
      - Oxide bond occurred around rim of wafer trapping gas.

Relatively good bonding



Poor

Bad

Bonded wafer acoustic images, white areas are bad bonding

- Decided to try bonding wafers using Ziptronix DBI (Direct Bond Interface) process. [4]
  - No unused wafers left.
  - Ziptonix separated one pair of poorly bonded Tezzaron wafers from EVG in Tempe
  - Wafers were reprocessed for oxide bonding and bonded at Ziptronix.

Simplified Ziptronix process

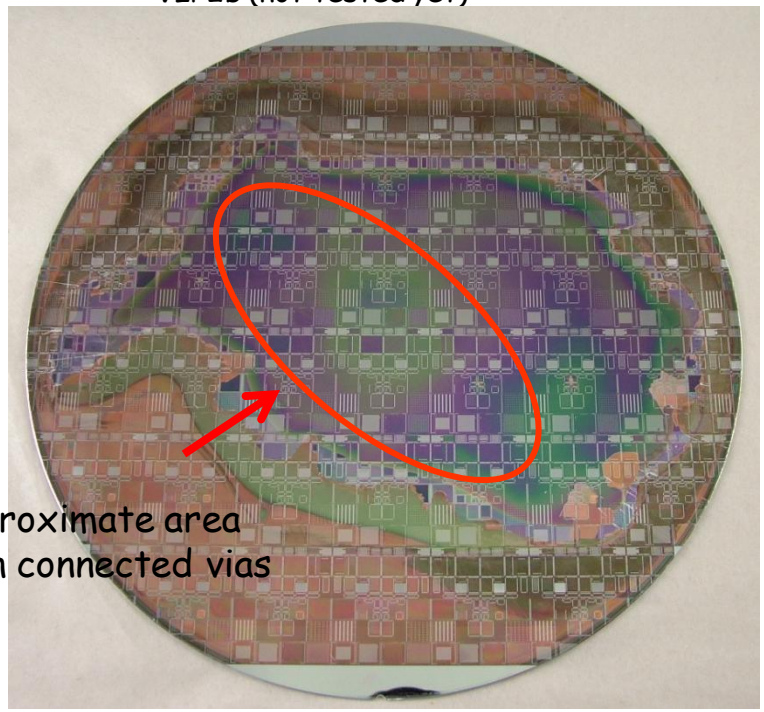
Part of Ziptronix Process used

Ziptonix bonding was not great due to prior history of wafers.

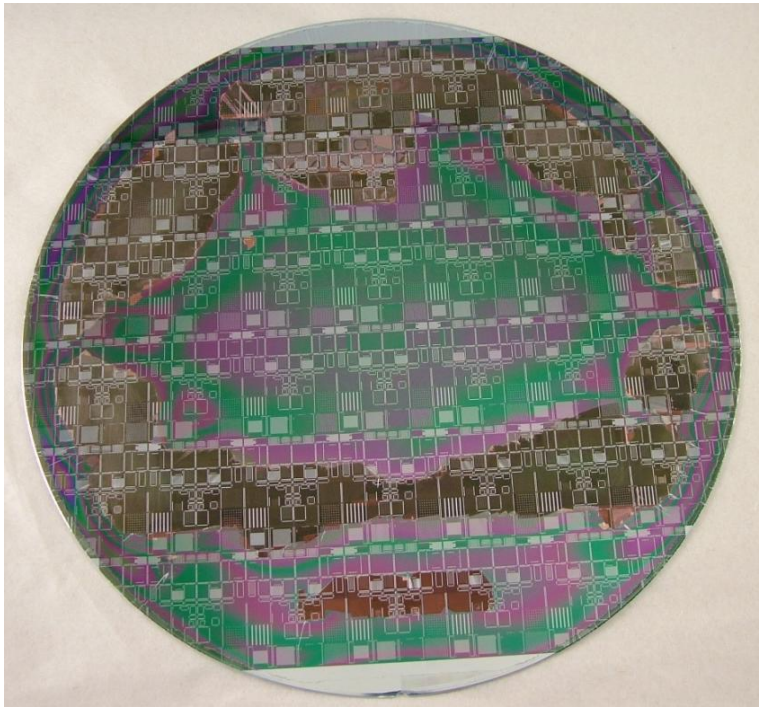
Wafers Diced for Test Parts

- Ziptronix bonded wafer
  - Used refurbished Tezzaron bonded wafers as a test for DBI process
  - Limited number of useable parts for testing
  - Parts distributed to collaborators
  - Fermilab parts
    - VICTR (tested)
    - VIPIC (tested)
    - VIP2b (not tested yet)

- Tezzaron bonded wafer
  - Eye pattern of useable parts (in center)
  - Limited number of useable parts for testing
  - Parts distributed to collaborators
  - Fermilab parts
    - VICTR (tested)
    - VIPIC (tested)
    - VIP2b (not tested yet)



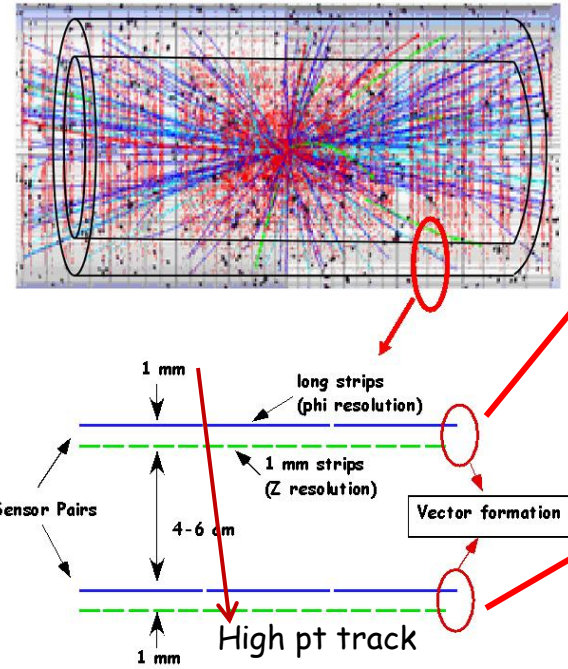
Ziptronix bonded wafer – non-uniformity of Si CMP caused by non-uniform bonded area resulted in right side TSVs being buried and not connected.



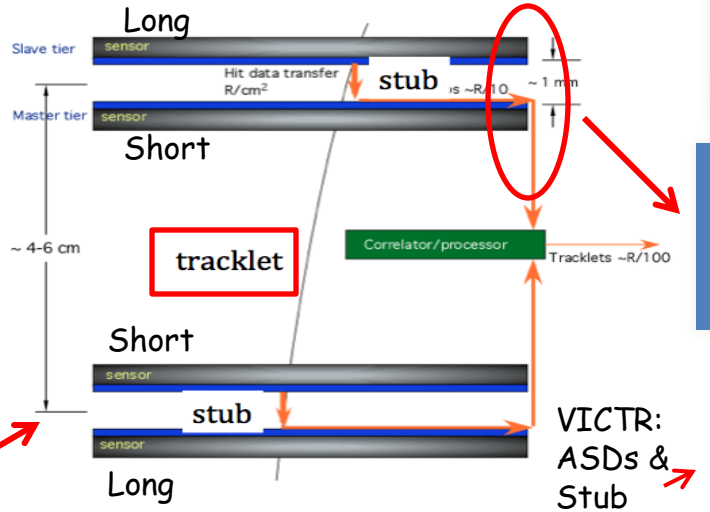
Tezzaron bonded wafer – TSVs appear to connected across the entire bonded area (eye pattern in center).

VICTR (Vertically Integrated CMS TRacker)

- High luminosities at the SLHC will require track trigger to reduce hit densities for data readout.
- Track trigger has several functions
  - Identify particles Pt above 2 Gev for data transfer
  - Identify particles with Pt above 15-25 Gev (low curvature tracks)
  - Provide Z resolution of about 1 mm for tracks above 2Gev with short strips
  - Phi resolution provided by long strips
- Our solution is based on assemblies of sensors and 3D readout chips that forms track stubs and tracklets looking for track curvature. [5]
  - Stubs are found locally from sensor pairs
    - Comprised of a top detector (phi) of long strips
    - A 1 mm interposer
    - The VICTR ASIC with 2 tiers
    - A bottom detector (z) comprised of short strips
  - Tracklets found from a pair of stubs
  - Tracks found by precise extrapolation of tracklets to other layers.
- More sophisticated logic to be added to later versions of VICTR

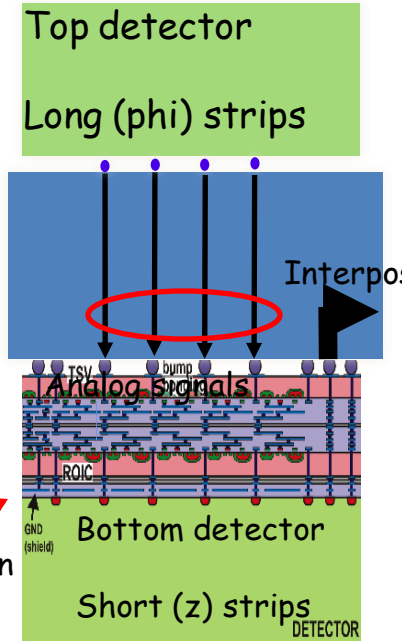


2 layers form a stub



2 stubs form a tracklet

VICTR: ASDs & Stub formation

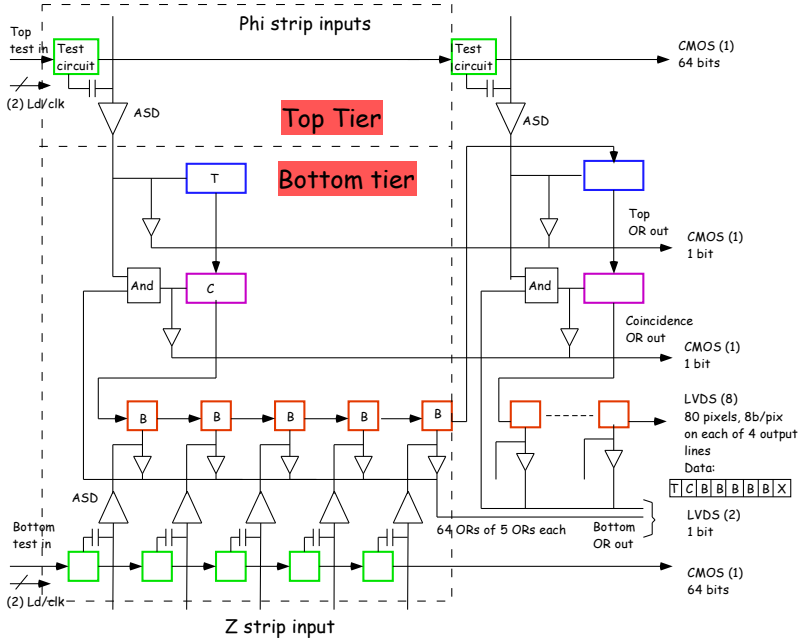


Stub detail

Note: Not to scale

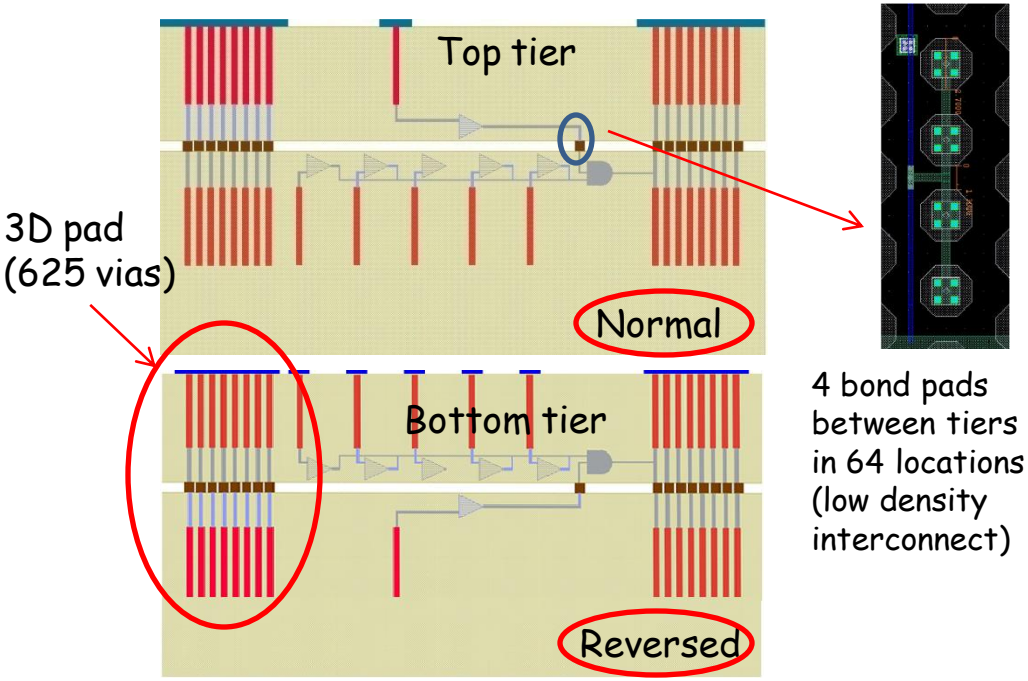
VICTR

- The function of the VICTR chip is to find coincidences between hits on the top strips (phi) and their associated bottom strips (z).
- Features
  - Programmable test input for every strip
  - Fast OR output for Top hits, Coincidence, and Bottom hits.
- Detector arrays for VICTR
  - 64 long strips
  - 5x64 = 320 short strips



Top tier to bottom tier coincidence circuit

- The single mask set wafers provide chips both with the top tier on the surface and the bottom tier on the surface.
- 3D pad connections were incorporated in the VICTR design to allow testing of both versions
  - Top tier, face up is called normal
  - Bottom tier, face up is called reversed.

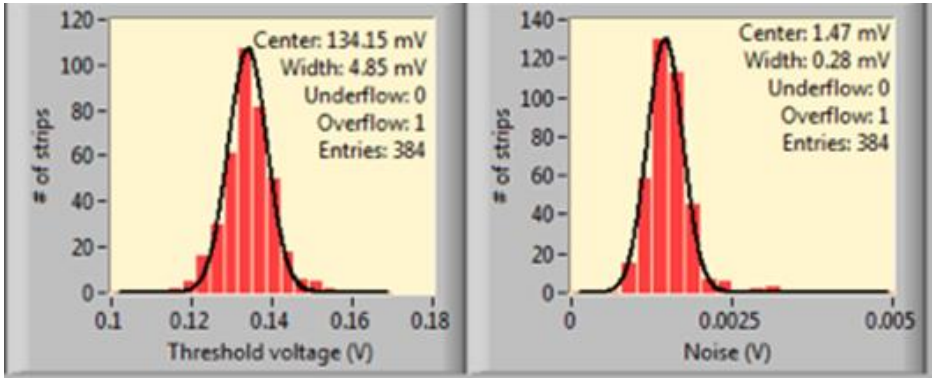


Two versions of VICTR chip

VICTR

- A small number (11) of VICTR chips were visually inspected and selected for testing from both the Tezzaron and Ziptronix bonded wafers.
- Fully functional chips
  - Ziptronix bonded chips: 3 normal, 1 reversed
  - Tezzaron bonded chips: 1 normal
- Partially working chips
  - Ziptronix: 1 normal
  - Tezzaron: 2 reversed
- No inference should be made regarding process yields
- Functions tested
  - Charge injection to top and/or bottom ASD circuits
  - Masking of hit channels
  - Common threshold adjustment for top and bottom ASDs
  - Readout of top, bottom, and coincidence hits.
  - Power dissipation
  - Threshold dispersion
  - Noise

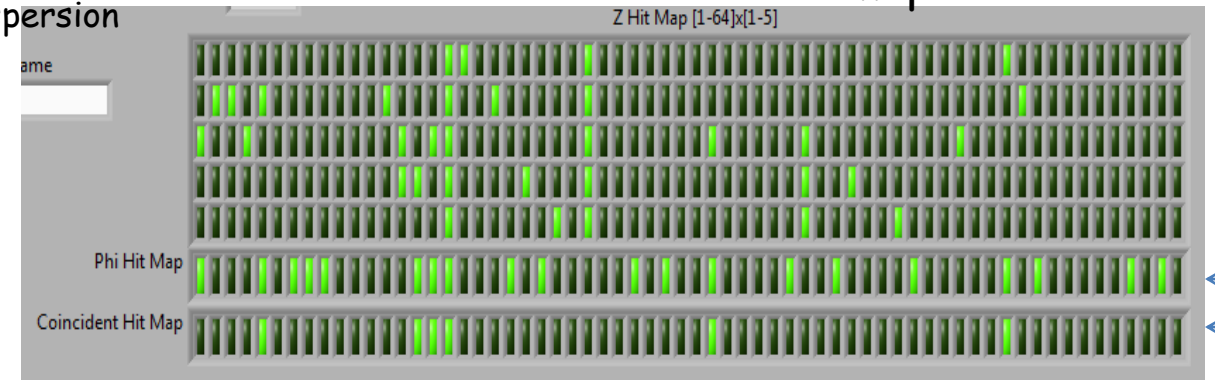
- In order for chips to work, one ASD signal is passed from the top tier to the bottom tier through 4 parallel copper bond connections.
- All signals are brought onto the chip through bond pads with multiple 1 um TSVs. (normal and reversed chips)
- Work is in progress to bond working chip to a detector



Threshold dispersion

Noise

Hit and coincidence map



Bottom strip hits

Top strip hits

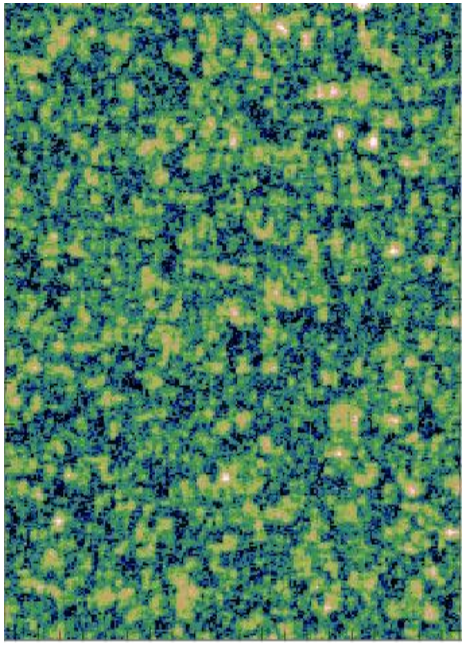
Coincidence

Random noise hits set by lowering threshold.

Green = hit

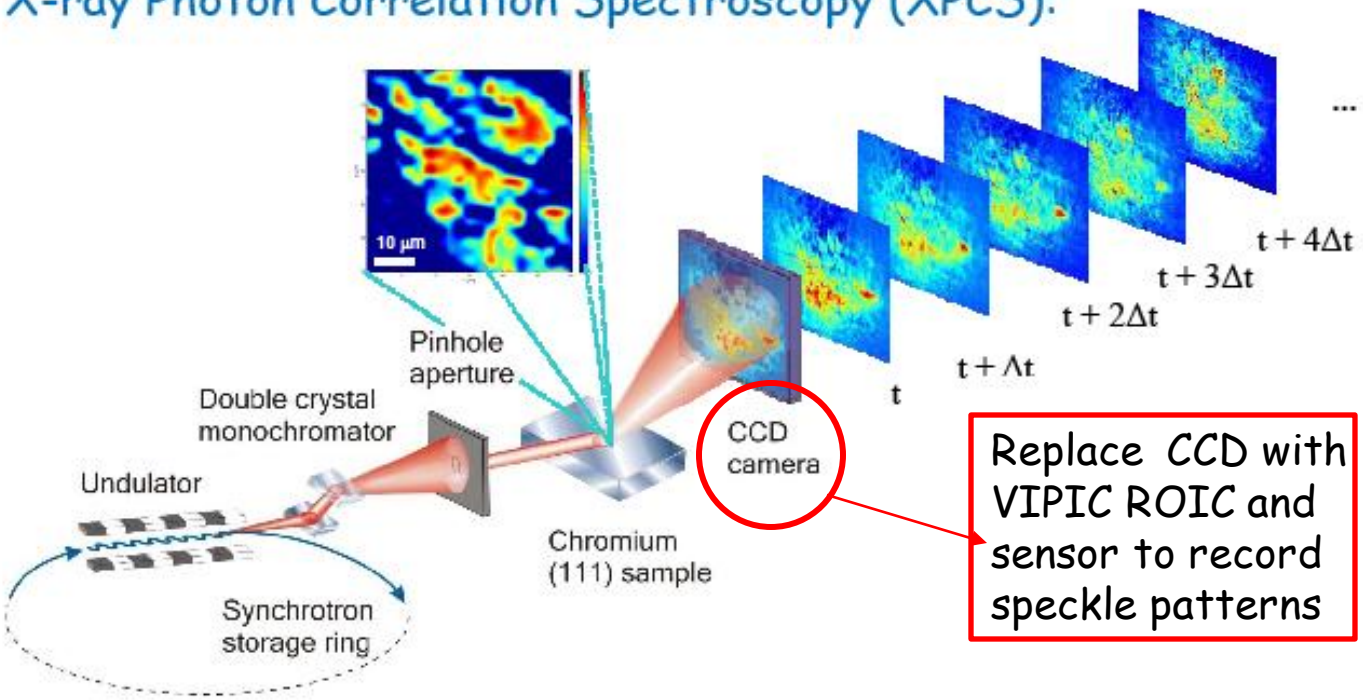
VIPIC for X-ray Photon Correlation Spectroscopy (XPCS)

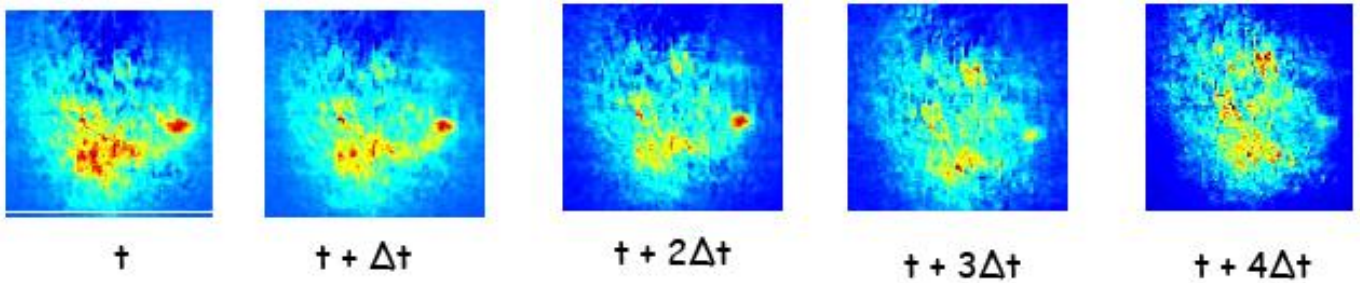
- XPCS is a novel technique that studies the dynamics of various equilibrium and non-equilibrium processes occurring in condensed matter systems [6] (e.g. gels, colloids, liquid crystals, bio-materials, membranes, metals, oxides, magnets, etc.)
- XPCS is based on the generation of a speckle pattern by the scattering of coherent X-rays from a material where spatial inhomogeneities are present.
- If the state of disorder of the system changes with time, the speckle pattern will change. Thus by studying the time dependence of the scattered intensity, one can study the dynamics of the materials both in or out of thermodynamic equilibrium (e.g. diffusion constants, magnetic domain relaxation times, phase transformations)
- Advantages
  - Observe smaller features sizes
  - Can be used to observe charge, spin, chemical and atomic structure behavior.
  - Works with non-transparent materials



Speckle pattern

X-ray Photon Correlation Spectroscopy (XPCS):





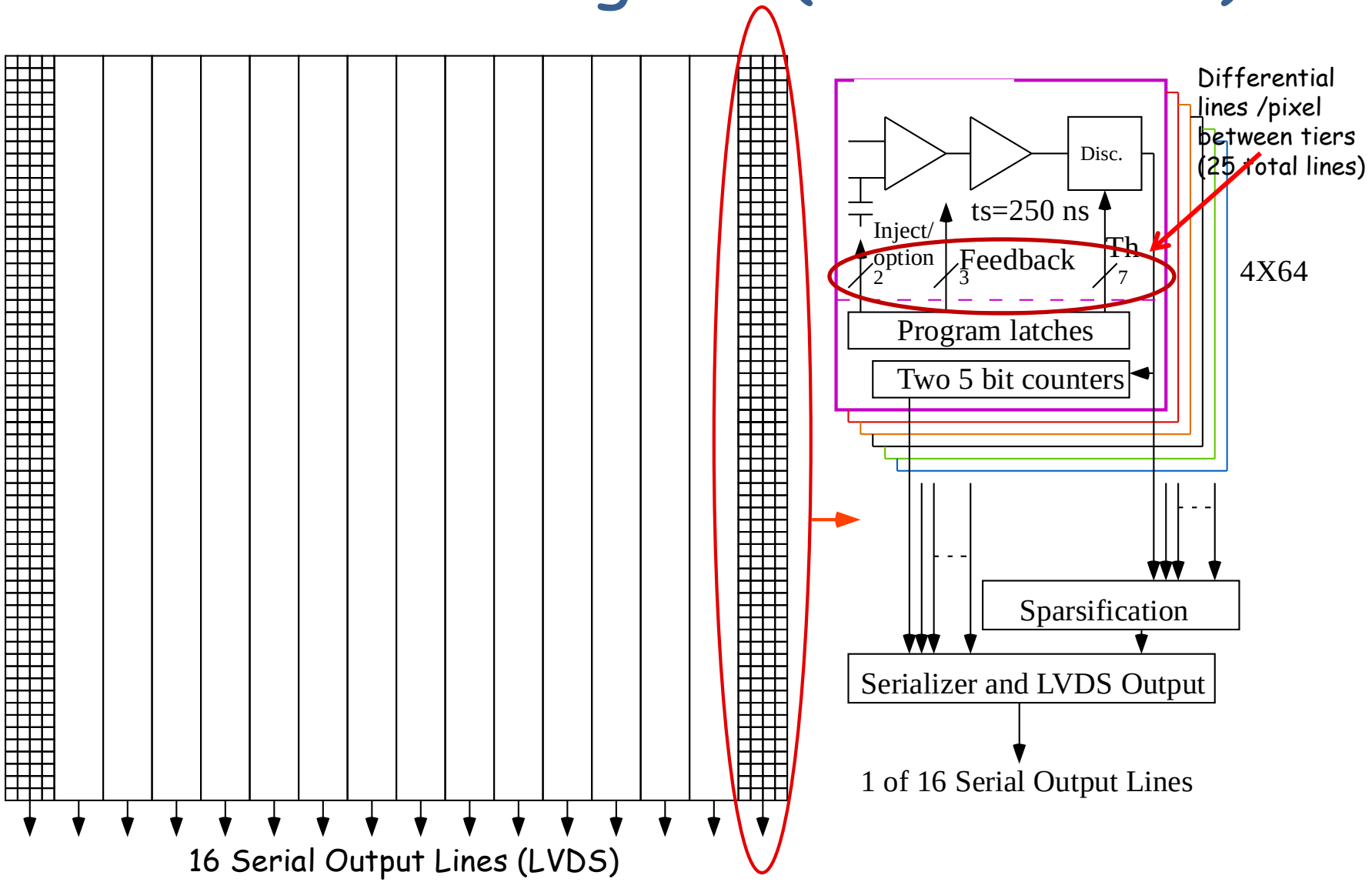
Speckle pattern changes with time

O. G. Shpyrko et al., *Nature* **447**, 68 (2007)

VIPIC (Vertically Integrated Photon Imaging Chip)

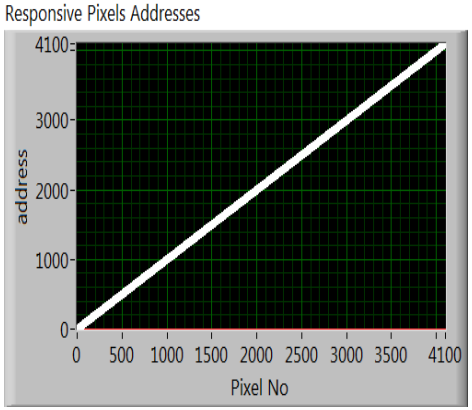
- The VIPIC is designed to quickly count hits in every pixel and read out quickly the hits in a sparsified and dead timeless manner.
- Specifications
  - 64 x 64 array of 80 micron pixels
  - Binary readout (no energy information)
  - Optimized for photon energy of 8KeV
  - Triggerless operation
  - 2 Modes
    - Timed Readout of hits and addresses at low occupancy (10 usec/frame for occupancy ~ 100 photons/cm^2/usec)
    - Imaging – alternating 5 bit counters read out hits in each time slot without addresses but using sparsification
- Relatively complicated communication protocol and a high number of signal lines (25) passed between tiers for every pixel.
- Features (5.5 x 6.3 mm die size)
  - Two 5 bits counters/pixel for dead timeless recording of multiple hits per time slice (imaging mode)
  - Sparsified address generated by priority encoder [7]
  - Generates pixel address in 5 ns regardless of hit pixel location
  - Parallel serial output lines
    - 16 serial high speed LVDS output lines
    - Each serial line takes care of 256 pixels
  - 2 tier readout chip with separate analog and digital tiers
  - Adaptable to 4 side butt able X-ray detector arrays

VIPIC Block Diagram (4096 Pixels)

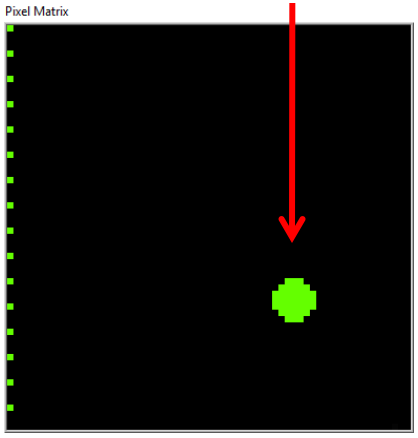


Test Results

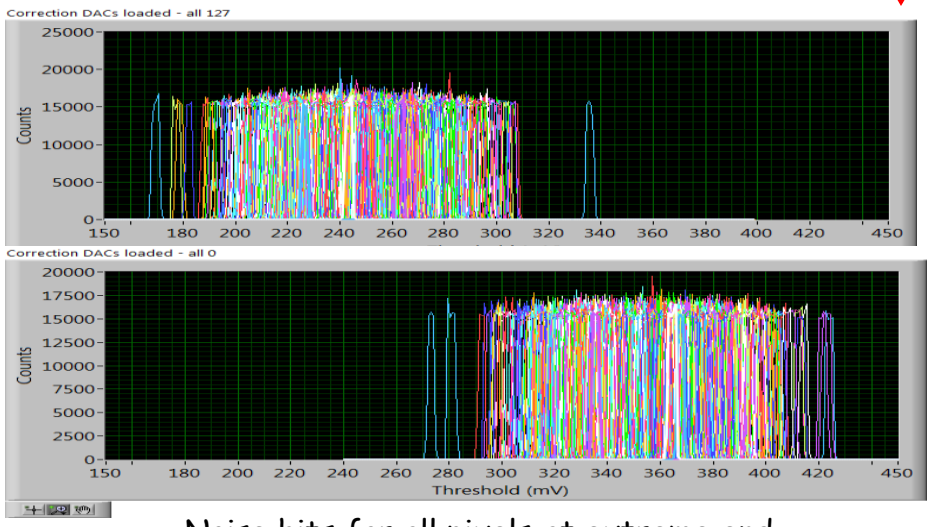
- Bonded 5 chips after visual inspection
  - 1 Tezzaron bonded chip is working
  - 2 Ziptronix bonded chips are working
- Testing confirms operation in both modes [8]
  - Configuration shift registers (up to 49152 bits long) are working.
  - Shifted in 1's to all cells with cal strobe and read out every address in normal readout mode in sequential order.
  - Found address encoder generating proper addresses
  - Thinned analog tier operation closely matches simulated performance. (Power and noise)
  - Reset (kill) all pixels and set pixels in region of interest, found appropriate sparsified addresses
  - Reduced threshold to get noise hits and found pixel counters reading out non-zero values. Chip fully working from input to output
  - Outputs fully functional
    - 16 serializers
    - 16level converters
    - 16 LVDS buffers
  - Changed 7 bit threshold DAC to 2 end values and found appropriate shift in threshold distributions (DAC range wide enough to correct for offsets)
- Future tests: 3 bits for preamp time constant, precise trimming of offsets
- Of the 25 connections/pixel between tiers, 19 appear to be working and 6 haven't been tested yet



Proper sequential address read out when 1's shifted into all cells (using normal read out mode)



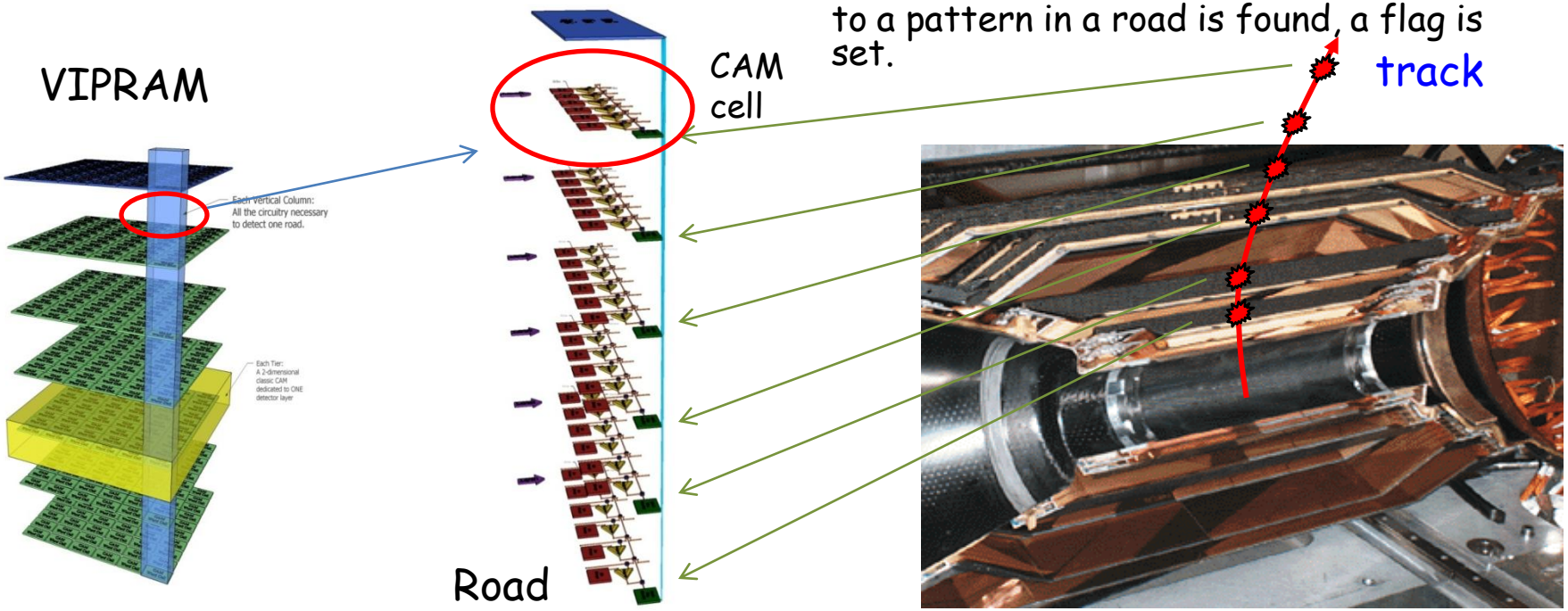
Normal array read out with all pixels killed except small area in green (sparsification works)



Noise hits for all pixels at extreme end of DAC settings

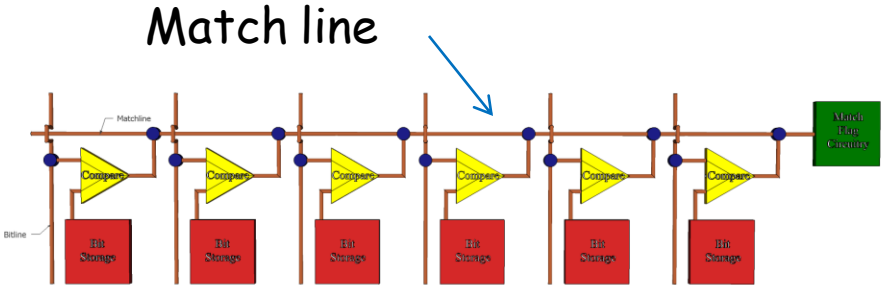
New 3D Effort: VIPRAM

- Particle track reconstruction using fast pattern/track recognition is becoming increasingly more difficult as luminosities increase in HEP experiments
- The Pattern Recognition Associative Memory (PRAM) concept has been successfully used in the AMchip03 at CDF for fast track finding. [9]
- VIPRAM adds the idea of Vertical Integration to increase pattern density and decrease power. [10]
- Monte Carlo simulations are used to create particle track address patterns in VIPRAM corresponding to possible hits in a number of detector layers.
- The stored patterns are then compared in real time to incoming detector addresses and when matches to a pattern in a road is found, a flag is set.

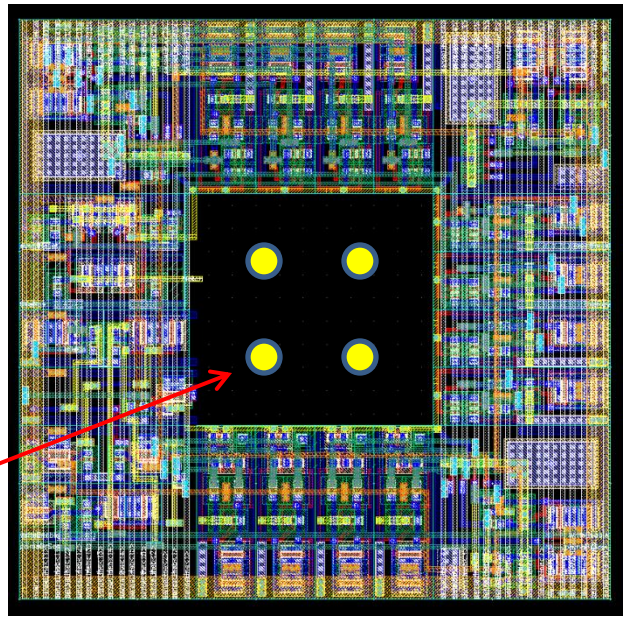


Benefits of 3D to the PRAM Concept

- Traditionally a CAM cell is a linear array of digital comparison and storage circuits with a relatively long match line.
- Several CAMs working together form a PRAM
- 3D allows for a new configuration for the match line and shorter communication to the glue logic which increases speed and lowers power.
- Currently designing a 2D PRAM chip with a 15 bit CAM cell layout in a 128 x 128 array which is easily converted to a 3D stacked assembly
- See poster by Jim Hoff at this conference, "Vertically Integrated Pattern Recognition Associated Memory for Track Finding" [11]



6 bit CAM cell



15 bit CAM cell layout for 2D and 3D

Future

- Positive test results also reported from France, Germany and Italy on other designs – will review at future collaboration meeting.
- 18 new wafers have been fabricated to replace the Global foundries wafers lost in 3D assembly
- The wafer lot has been split into two parts for 3D assembly
  - 8 wafers have had smaller copper pillars (1 um) placed on top of the copper bond pads (2.7 um) which increases the oxide bond area for oxide bonding at Ziptronix
  - 8 wafers have had the oxide recessed by 350 nm for Tezzaron copper-copper bonding at EVG in Austria
  - Assembled wafers expected in 4-8 weeks.
  - 1 wafer was used for 2D parameter testing
  - 1 wafer unused a this time.
- Future at Tezzaron
  - 200-300 mm EVG bonder is on order for delivery in Dec which should reduce the dependence on outside vendors for bonding and reduce fabrication time.
  - The goal is to consolidate all 3D assembly processes in North Carolina except for the via fabrication, thus reducing wafer aging and fabrication time
  - Tezzaron plans to compare bonding results from the Ziptronix and Tezzaron bonded wafers for improved yield in the future.
  - New capabilities
    - 4 Layer Cu BEOL metal cap (in fab; release Feb 2013)
    - 1.2um TSV insertion, near end of line (in fab; release Feb 2013)
    - 3-5 Material handling (GaAs, InP, etc) expected 2013
- MOSIS plans second 3D run for Nov 2012. (First 3 D run near end of fabrication at Global Foundry)

Conclusion

- Much time has passed since designs were submitted to the first 3D multi project run for HEP.
- Numerous problems were encountered at nearly every level resulting in unfortunate delays.
- Recently some positive results have been achieved by Fermilab and other designers from the first 3D run.
- Although there have had many set backs, the first test results are encouraging, demonstrating that 3D integration is feasible.
- We look forward to an easier design flow in the future and fully implementing designs for applications now under consideration.
- Future 3D design submissions handled by MOSIS/CMP/CMC should provide a better interface to users.

References

- [1] Deptuch, G.; Demarteau, M.; Hoff, J.; Lipton, R.; Shenai, A.; Yarema, R.; Zimmerman, T.; , "Pixel detectors in 3D technologies for high energy physics," 3D Systems Integration Conference (3DIC), 2010 IEEE International , vol., no., pp.1-4, 16-18 Nov. 2010.
- [2] R. Yarema, The First Multi-Project Run with Chartered/Tezzaron, Front End Electronics Meeting 2011, Bergamo, Italy, May 24-27, 2011.
- [3] V. Dragoi, et. al., Metal Wafer bonding for MEMS Devices, Romanian Journal of Information Science and Technology, vol 13, no. 1, 2010, p 69.
- [4] P. Enquist, Direct bond Interconnect (DBI) – Technology for Scaleable 3D SoCs, 3D Architectures for Semiconductor Integration and Packaging, Oct. 31-nov 2, 2006, San Francisco
- [5] M. Dell'Orso and L. Ristori, "VLSI Structures for Track Finding," Proceedings in Nuclear Instruments and Methods, vol. A278, pp. 436-440, 1989.
- [6] Shpyrko OG, Isaacs ED, Logan JM, Feng Y, Aeppli G, Jaramillo R, Kim HC, Rosenbaum TF, Zschack P, Sprung M, Narayanan S, Sandy AR.
- [7] P. Fischer, "First implementation of the MEPHISTO binary readout architecture for strip detectors", NIM A461, pp.499-504
- Nature. 2007 May 3;447(7140):68-71.
- [8]P. Maj, G. Carini, G. deptuch, P.Grybos, P. siddons, R. Szczygiel, M. Trimpl, R. Yarema, First three-dimensionally Integrated Chip for Photon Science, to be presented at Vertex 2012, Korea.
- [9] M. Dell'Orso and L. Ristori, "VLSI Structures for Track Finding," Proceedings in Nuclear Instruments and Methods, vol. A278, pp. 436-440, 1989.
- [10] Ted Liu, Jim Hoff, Grzegorz Deptuch, Ray Yarema, A New Concept of Vertically Integrated Pattern Recognition Associative Memory, TIPP 2011 – Technology and Instrumentation for Particle Physics 2011, Direct Science, Physics Procedia (2011) to be published.
- [11] J. Hoff, "Vertically Integrated Pattern Recognition Associated Memory for Track Finding, presented at TWEPP 2012.