Contribution ID: **84** Type: **Oral**

Vertically Integrated Circuits for Detectors at Fermilab

Tuesday, 18 September 2012 11:35 (25 minutes)

The paper reviews the advancements in the three-dimensional integration of circuits for readout of solid-state detectors. It focuses on the details of the first 3D MPW run submitted in the HEP community. New high density circuit bonding techniques, wafer thinning, and submicrometer size TSVs IC provide new opportunities for a detector designer. These opportunities will be presented by looking at various 3D designs indicating that the 3D-IC technology is a reality. However, the problems manifested in the first MPW run, will not be forgotten and will be discussed in detail.

Summary

Commencement of work on three-dimensionally-integrated circuits in the HEP community had barely any delay to the appearance of first commercial 3D-IC design kits. Announcements whetted the appetite of the community and raised confidence in the rapid rollout of 3D-IC technology, which undoubtedly introduces a new quality to integrated readout system for the detectors. The Fermilab team was in this group of a few, who spearheaded the development of 3D integrated circuits for readout of detectors. A fully-depleted CMOS SOI process by MIT-LL and the via-last based wafer bonding technology was used first. Then, the focus was on bulk CMOS wafers with front-end-of-line integrated micrometer-size through silicon vias (TSVs) from a commercial vendor and the Tezzaron wafer bonding technology. The early Fermilab work led to an international consortium, which has grouped major research centers. The consortium submitted the first multi-project wafer (MPW) run to Tezzaron with over 25 different designs in 2009. The run unfortunately has been suffering from multiple problems causing an overall delay to such an extent that no diced, operational 3D parts could be delivered to the participants until the drafting of this abstract. Despite of this apparent cheerlessly picture of the downbeat, the peripeteia, associated with it, have been a source of valuable experiences about 3D-IC processing technology, i.e. requirements for the surface flatness and surface treatment, alignment, gas atmosphere, role of aging of metal bonding posts, etc.. An additional lot of wafers was started due to having the initial stock of wafers used up for bonding attempts that turned out unsuccessful. These extra wafes are near the end of fabrication at the foundry now. By having the conditions of the Cu-Cu thermo-compression bonding process fine-tuned, it is expected that the wafers from the new lot will be bonded successfully. Owing to the fact the reasons of failing with bonding at the first place remain merely obscure, the last pair of wafers from the first lot is currently undergoing a modified bonding procedure, i.e. the Cu DBI® method is used. This method requires a larger part of a wafer covered with planarized oxide. Thus, a deposition of small Cu studs on each of original Cu bonding posts and flowing of oxide on a whole surface, are being done. The review of consecutive steps will be provided at the presentation. Professional brokers have opened an access to the Tezzaron/GlobalFoundries 3D-IC process through the MOSIS MPW scheme in the autumn of last year. The decision draws deeply from the knowledge acquired in the completion of the 3D-IC MPW run by Fermilab and successful accomplishment of another MPW run that was processed in parallel to the HEP one. New high density circuit bonding techniques, wafer thinning, and submicrometer size TSVs IC provide new opportunities for a detector designer. These opportunities will be presented by looking at various 3D designs indicating that the 3D-IC technology is a reality.

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Session Classification: A1b