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Development of the Scalable Readout System for Micro-Pattern Gas Detectors and Other Applications

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Developed within RD51 Collaboration for the Development of Micro-Pattern Gas Detectors Technologies, the Scalable Readout System (SRS) is intended as a general purpose multi-channel readout solution for a wide range of detector types and detector complexities. The scalable architecture, achieved using multi-Gbps point-to-point links with no buses involved, allows the user to integrate different front-end ASICs and tailor the system size to his needs. Current applications include LHC upgrade activities or homeland security applications. The system architecture, development and running experience will be presented, together with future prospects, xTCA implementation options and application possibilities.

Summary

The Scalable Readout System is designed around a bivalent scalability concept, which refers to both applications range and system size. Not limited to a single detector technology, the system needs to respond to a wide range of detector requirements, in terms of sensitivity, time resolution, rate capability, trigger concept, radiation or magnetic tolerance, etc. In the same time the SRS concept has to allow the integration of detectors with different sizes, from small prototypes to large area detectors.

SRS introduces a modular concept that offers the possibility to connect different front-end ASICs to the standard SRS electronics, allowing the user to choose the most suitable front-end for the detector technology employed.

The front-end DAQ unit is composed of a chip-carrier hybrid mounted on the detector, an ASIC-dependent adapter-module hosting the specific electrical interface to the front-end hybrid and an SRS-standard FPGA-based card (FEC) which accepts different adapter modules as plug-in cards.

A number of FEC units can be put together in crates in a rack-mountable system integrating the required number of readout channels. For small and medium-sized systems the FEC card(s) use Gigabit Ethernet to communicate with the DAQ cluster. For large systems, a Scalable Readout Unit (SRU) is supplied which can aggregate up to 40 FEC cards (82kchannels) via a proprietary data-trigger-and-control (DTC) link over conventional CAT6 cables. The SRU DAQ link uses either 10Gpbs Ethernet protocol or another application specific protocol, like S-Link or DDL. The FPGA-based SRU board provides additional logic resources and memory space that can be used for advanced data processing or trigger algorithms.

The entire system uses serial point-to-point links with no buses involved, facilitating scalability, without any loss of performance. Fixed-latency channels are reserved in both directions for trigger primitives, allowing the use of complex trigger schemes.

First delivered systems integrate the APV25 front-end chip with spark protection circuitry and are now employed in different research fields, like sLHC upgrade activities, geophysical muon tomography or homeland security applications. In response to the increasing demand of the community, new hybrids are developed integrating the Beetle, VFAT2 and VMM1 front-end ASICs. A prototype system using Timepix is also under evaluation.

Commercially available HDMI cables are used as high-speed versatile connection between the front-end hybrid and the adapter module, while high-speed electrical or optical links are foreseen for future large-scale systems.

An alternative implementation of the SRS architecture in xTCA industrial standard is under investigation in collaboration with a specialized external team. The industrial standard provides intrinsic compatibility with the SRS topology while enhancing robustness and reliability. In particular the ATCA standard may increase the channel density and potentially provide an efficient DAQ platform for future large scale detector applications in either research or industrial fields.

The system architecture, development and running experience will be presented, as well as future prospects and application possibilities.

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