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The Belle II Silicon Vertex Detector Readout Chain

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The Silicon Vertex Detector of the future Belle II experiment at KEK (Japan) will consist of 6”double-sided sensors. Those are read out by APV25 chips (originally developed for CMS) which are powered by DC/DC converters with floating low voltages on top of the bias potentials. The signals are transmitted by cable links of about 12 meters. In the back-end, the data are digitized and processed by FADC modules with powerful FPGAs, which are also capable of precisely measuring the hit time of each particle in order to discard off-time background.

Summary

In total, the future Belle II Silicon Vertex Detector (SVD) will comprise of 172 double-sided silicon sensors (entirely made from 6” wafers), being read out by 1748 APV25 chips. Those will be operated by floating low voltages with potentials at the respective bias voltages. In order to efficiently utilize existing power supplies from the previous Belle experiment (with a much smaller silicon detector), we will use radiation tolerant DC/DC converters close to the front-end using the AMIS chip presently being developed at CERN.

Being a low-energy experiment, the dimensions are much smaller than at LHC experiments and thus the distance between APV25 chips and the back-end is just about 12 meters, which can be directly linked by copper cables without the requirements of intermediate repeaters nor optical links. The APV25 output signals, delivering a stream of switched analog levels at 40 MS/s, are refurbished in the back-end using Finite Impulse Response (FIR) filters implemented in FPGA firmware. These filters operate in real-time and are capable of removing the effects of both distortions due to frequency-dependent cable attenuation as well as reflections.

Not only digitization and signal conditioning will take place in the back-end FADC modules, but also signal processing, including strip data extraction, pedestal subtraction, a 2-pass common mode correction and zero suppression (sparsification). On top of that, there is one more important feature as described below.

In CMS, the APV25 chips are operated synchronously to the LHC collisions, allowing their built-in “deconvolution” mode to narrow down the effective signal shape and thus unambiguously identify the originating bunch crossing. As Belle II will have quasi-continuous collisions, this method cannot be used. However, the APV25 can also operate in a mode where it records several samples along the shaped waveform for a single event. By default, six consecutive samples will be read out in Belle II. These data will be processed to find the particle timing with a precision of a few nanoseconds. Several lab and beam tests have been performed to demonstrate this powerful feature by offline data processing. In the future, we will implement such an algorithm in the FPGA firmware and simulations have already shown that this can be done with lookup tables providing sufficient precision. Thus, the presumably dominant amount of off-time background hits can be discarded in order to reduce the overall occupancy and data rates.

In this presentation, we will show the existing prototypes for components of the readout chain, the results obtained at beam and lab tests as well as new developments and circuits to be used in the final readout system which is presently being designed and subsequently built.

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