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Upgrade of the COMPASS calorimetric trigger

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In 2009 COMPASS performed a test measurement of neutral Primakoff reactions, characterized by high energetic photons in one of the two electromagnetic calorimeters. Back then a digital trigger had been implemented to the existing readout electronics in order to detect these events. For 2012 a long measurement of these processes is foreseen. In order to extend the cinematic range to lower energetic photons the trigger system is upgraded in a way to be more selective to specific physics channels. In order to do so the hit information is combined and processed in one single FPGA.

Summary

COMPASS is a fixed target experiment at CERN, which utilizes muon and hadron beams. End of 2009 a very short measurement of the Primakoff reaction has been performed. In order to detect these reactions a new digital trigger system for the downstream electromagnetic calorimeter was developed. This system is fully implemented in the existing ADCs which are also used for the readout of the detector. This electronics utilizes a Virtex4 FPGAs combing 16 channels each with a resolution of 12 bit at 80 MHz.

The trigger uses a digital constant fraction discriminator implemented for each channel within the FPGA which determines the signal time with a precision of about 1 ns. The implementation based on the expected cinematic was a summation of energies on consecutive FPGAs. On a VME backplane the sum of up to 512 channels is computed and compared with a threshold. With this simple scheme the trigger rate at a threshold of about 50 GeV already exceeds the maximum possible trigger rate of 50 kHz.

In 2012 a full run of three months is performed for which the system is further upgraded. In order to lower the threshold and still fulfilling the maximum rate capabilities further algorithms and a new backplane card are developed. As the main physics channel to be studied is the pion polarizability, for which th e cross-section for single photon radiation has to be measured a single cluster detection is implemented in addition to the summation trigger that has been already used. The simple pipelined summation is replaced with a full hit transmission to the backplane. This requires many efforts to keep the latency as short as possible as the bandwidth between the FPGAs is limited. The newly developed backplane which has to be able to process all these data uses a Virtex6 FPGA which has enough resources to perform all necessary calculations. In total 6 backplanes are installed and connected by optical fibers allowing to combine the information of all 3072 channels of the detector.

The hit information on the backplane is processed in two steps, once the information coming in is directly processed and stored to the correct time slice. Later the information coming in from other backplanes is collected and combined allowing to make the final trigger decision.

Monitoring is implemented using the Xilinx Microblaze softcore CPU which collects status informations from the logic instances and sends them out via an ethernet interface to a server which stores this information to a database. All these information can then easily be controlled via the COMPASS DCS system.

In this talk the full trigger setup and all processing steps will be presented. Further the performance during the 2012 run will be discussed.

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