The GBLD : a radiation tolerant laser driver for high energy physics applications.

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The GigaBit Laser Driver (GBLD) is a radiation tolerant ASIC which is part of the GigaBit Transceiver (GBT) chip-set. It is aimed to drive both edge emitting and VCSEL laser diodes at a data rate in excess of 5 Gb/s. The GBLD can provide a modulation current up to 24 mA and a bias current up to 43 mA.Pre- and de-emphasis functions are implemented to compensate for high external capacitive loads and asymmetric laser response. The chip is designed in a 130 nm CMOS technology and is powered by a single 2.5 V supply.

Summary

The GBLD is a laser driver designed to target applications where radiation effects are of major concern. It is part of a broader effort to design a bi-directional optical link (the GigaBit Transceiver and the Versatile Link projects) for the HL-LHC.

The GBLD is designed for a data rate in excess of 5 Gb/s and to drive both VCSELs and edge emitting laser diodes. For that purpose, the output stage is split in two halves, each capable to drive a modulation current between 2 and 12 mA each with an output impedance of 50 ohm. It is therefore possible either to use a single driver or the two connected in parallel, thus doubling the modulation current and halving the output impedance. The first configuration is suited for VCSEL, while the second is intended for edge emitting lasers. The modulation current can be controlled via a 6 bit DAC with a resolution of 0.16 mA (single driver) or 0.32 mA (two drivers in parallel). The GBLD also provides the laser bias current in the range 2 to 43 mA via an 8 bit DAC with a 0.16 mA resolution.

Pre- and de-emphasis can be applied independently on the rising and falling edge of the modulation signal, in order to cope with an asymmetric laser response. The emphasis pulse can be adjusted both in amplitude (up to 12 mA) and in time (between 60 and 90 ps) by a 4 and a 2 bits DAC, respectively.

The driver is basically a cascade of resistively loaded differential pairs. Inductive peaking has been used to increase the stages bandwidth. A T-coils based compensation circuit has been used at the input of the GBLD to reduce the capacitive contribution of the protection diodes.

The control DACs can be programmed via a I2C digital interface. Seven 8-bits control registers are used to store the configuration parameters. The control logic has been designed in order to be resistant to Single Event Upsets (SEUs) via Triple Modular Redundancy (TMR). An asynchronous correction logic has been adopted in order to provide error correction when the I2C clock is not present.

The chip is powered by a single 2.5V power supply, in order to use a single supply forboth the laser diode and the laser driver. An internal voltage regulator brings down the voltage to 1.5 V for the internal circuitry.

The GBLD has been designed in a commercial 130 nm CMOS technology and packaged in a 4x4 mm^2 QFN24 plastic package. Test results show a random jitter below 0.8 ps and a deterministic jitter below 15 ps. The 20%-80% rise and fall times are below 60 and 80 ps with and without pre-emphasis, respectively.

The chip has been irradiated with X-ray up to 100 Mrad(SiO2), showing no significant variation in the performances.

This work describes the operation principles of the GBLD circuits and the experimental results.

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