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Low Noise and Wide Dynamic Range Preamplifier and Shaper ASIC for the PANDA-Experiment

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The ASIC design group at GSI developed a preamplifier and shaper ASIC which is optimized for the requirements of the electromagnetic calorimeter of the PANDA experiment. This integrated circuit will be used for spectroscopy and was designed for the readout of a large area APDs with 300pF detector capacitance, a very high dynamic range and an event rate of 350kHz. Each ASIC includes 2 equivalent readout channels consisting of a charge sensitive preamplifier, a three stage shaper and differential output buffers. The on chip implemented programmable voltage references are able to compensate the temperature dependency on the output DC.

Summary

PANDA (antiproton annihilation at Darmstadt) is a next generation hadron physics detector planned to be operated at the future facility for antiproton and ion research (FAIR) at Darmstadt, Germany. As subdetector for measuring neutral and charged particles the electromagnetic calorimeter (EMC) is foreseen. The barrel part of the EMC will consist of about 11000 lead tungstate crystals. Each crystal will be read out by 2 large area avalanche photo diodes that have an active area of about 1 cm2. For the APD readout an integrated preamplifier and shaper was developed in a 350 nm CMOS technology by GSI-Experiment Electronics department.

Each ASIC includes 2 equivalent readout channels consisting of a charge sensitive preamplifier, a shaper stage and differential output buffers. As the input stage a folded cascode circuit was chosen. This stage was optimized for large detector capacitance, 350 kHz maximum event rate and best noise performance.
The following first integrator stage is based on a downscaled version of the preamplifier circuit which fits well to the input
operation point. After the first integrator stage the signal path is splitted into two sub paths. One of these sub paths has an amplification of 32 respectively 16 in comparison to the other to get larger output signals in the low energy range. Each path is built up by two first order integrators. The second integrator provides a differential output signal.
The ASIC is realized in a low power design due to the fact of a power limitation given by the experiment. The operation temperature in the experiment will be T = -25 C.
The fourth iteration of the ASIC (APFEL 1.4) submitted in spring 2012 includes design extensions in the analog and digital paths. The main modification in the analog path is the programmability of the amplification value without effecting the integration time. Therefore the R-C-feedback of the second shaper stage was built up switchable. For flexibility reasons an additional DAC was added to the circuit which separates the two readout channels from each other and allows an individual adjusting of the both readout channels. The on chip test pulser was extended by doubling the number of test pulse amplitudes. The APFEL 1.4 has now four different test pulse amplitudes with the value 1:2:4:8 for each channel. With these test pulses a monitoring of the readout electronics including a rough linearity monitoring is possible.
For programming a two-wire serial interface is implemented. By an 8 bit chip ID a common bus structure of up to 255 ASICs can be realized. One address code is reserved for broadcast communication.
The presented ASIC APFEL 1.4 will be used 2012 to equip a calorimeter prototype build up of 120 lead tungstate crystals.

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