The Upgrade of the PreProcessor System of the ATLAS Level-1 Calorimeter Trigger

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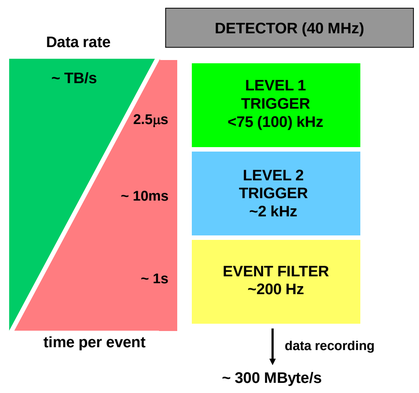
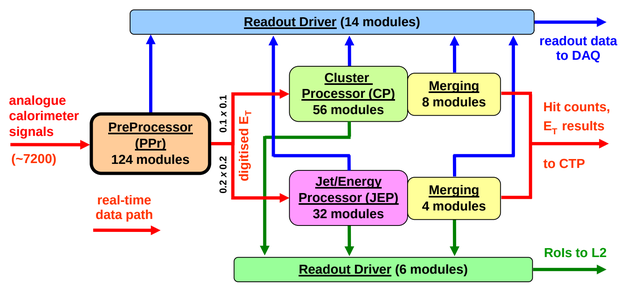
The ATLAS Trigger System

- three levels of event selection to successively reduce the event data rate from 40 MHz (LHC collision frequency) to about 200 Hz (data recording frequency):
  - **Level-1:** entirely implemented in hardware (ASIC and FPGA based), uses coarse granularity calorimeter and muon p_T data;
  - **Level-2 & Event Filter:** software-based, running on large computer farms, have access to full-granularity and full-precision detector data (including tracking).



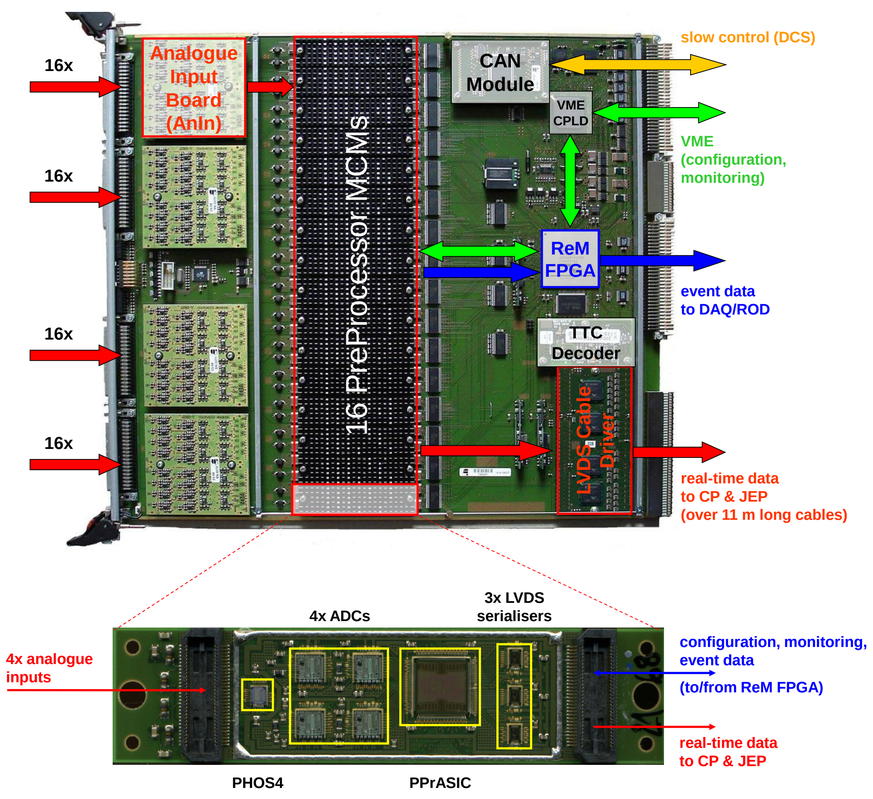
The Level-1 Calorimeter Trigger

- receives about 7200 pre-summed analogue signals from the entire ATLAS calorimetry.
- consists of three main subsystems:
  - **PreProcessor** (PPr): receives, digitises and processes the analogue inputs, and transmits digital data, representing the transverse energy deposits (E_T) for the identified bunch-crossing (BC), to the subsequent processors;
  - **Cluster Processor** (CP): identifies isolated clusters of electrons, photons, taus or hadrons;
  - **Jet/Energy-sum Processor** (JEP): identifies jets and computes the total and missing transverse information.
- transmits the results to **Central Trigger Processor** (CTP) within 2µs after the pp collision has occurred, for the final Level-1 trigger decision.



The PreProcessor System

- highly-parallel system with fast hard-wired algorithms implemented in application-specific integrated circuits (ASICs) and Multi-Chip Modules (MCMs);
- consists of **8 VME crates**, each containing **16** hardware-identical **PreProcessor Modules** (PPMs), that can each receive and process 64 analogue inputs.

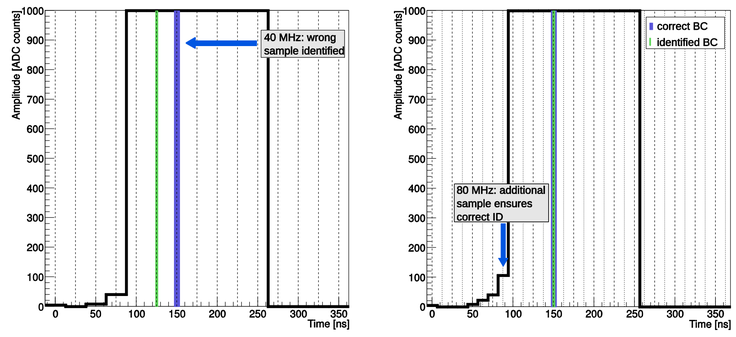


The PreProcessor Multi-Chip Module (PPrMCM)

- carries out the main processing tasks of the PPM;
- is a mini-printed circuit board which holds **9 wire-bonded unpackaged dies**:
  - **4 single-channel ADCs** (AD9042) to digitise the input signals with 10-bit resolution and a sampling frequency of 40 MHz;
  - **1 timing chip (PHOS4)** to adjust the phase of the digitisation strobes with 1 ns resolution;
  - **1 four-channel custom-made PreProcessor ASIC** (PPrASIC) to perform the main trigger-specific data processing:
    - coarse synchronisation of pulses originating from the same collision (16-bit deep FIFO);
    - identification of the E_T deposits per trigger channel and of the corresponding BC in time (FIR Filter and PeakFinder for pulses in linear range, dedicated algorithms for saturated pulses);
    - noise suppression, pedestal subtraction and fine-calibration of the extracted E_T values (LUT);
    - re-ordering of the trigger cells to better utilise the high-speed bandwidth to the CP system (BC multiplexing);
    - pre-summing of 4 trigger channels into a 0.2 x 0.2 jet element for the JEP system;
    - pipelined event data readout for monitoring purposes;
    - rate-metering and histogramming for trigger independent monitoring purposes;
  - **3 LVDS serialiser chips** to transmit the digital results to CP and JEP at a rate of 480 Mbit/s.

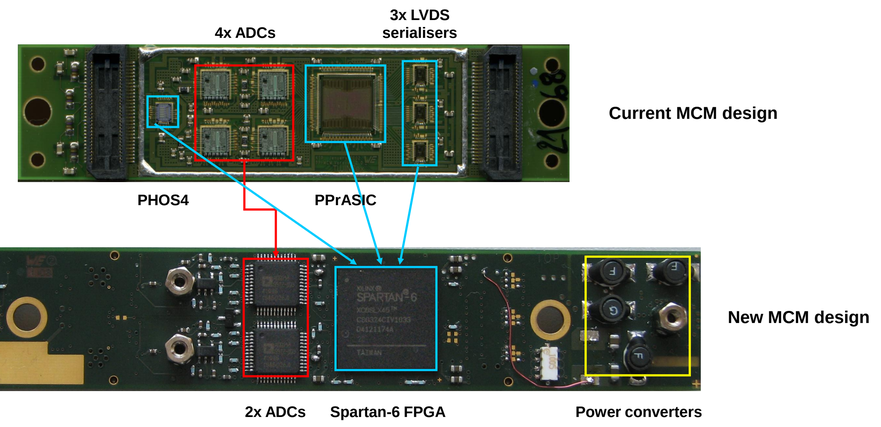
The New PPrMCM

- PprMCM technological decisions were taken more than ten years ago. At that time it was not feasible to have standard, packaged and flexible components which would meet the design requirements;
- modern re-programmable devices, featuring high processing speeds and generous logic and memory resources, allow to improve significantly the capabilities and the performance of the existing trigger algorithms as well as to implement new functionalities:
  - improved bunch-crossing identification (BCID) algorithm for saturated pulses, to handle analogue signals with a rise time longer than 50 ns;
  - improved noise filtering to maximise the energy resolution;
  - dynamic pedestal correction to handle signal pile-up in the detectors at high LHC luminosities;
  - separate fine-calibration for the E_T data sent to CP and JEP;
  - double LVDS data rate output (960 Mbit/s) to the upgraded JEP by transmitting 0.1 *x* 0.1 E_T information.

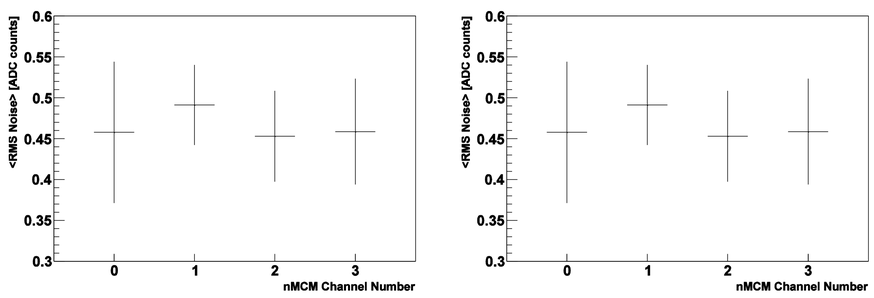


Simulation of the current (left) and improved (right) BCID algorithms for saturated pulses. The latter requires a sampling of the analogue input at 80 MHz

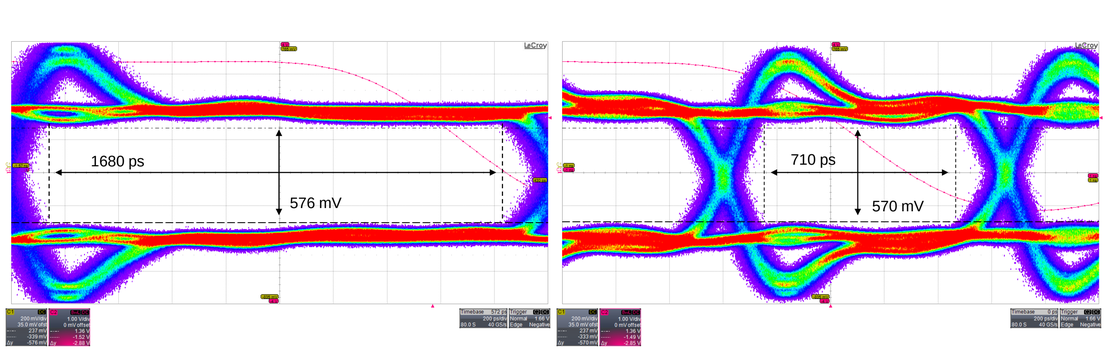
- an MCM substitute, functionally, mechanically and electrically equivalent to the current MCM, has been built at "Kirchhoff Institute for Physics" (KIP) Heidelberg. The new MCM (nMCM) carries the following main components:
  - **2 dual-channel ADCs** (AD9218) with 10-bit resolution and 80 MHz sampling frequency;
  - **1 Xilinx Spartan-6 FPGA** (XC6SLX45-3CSG324) device to take over the functionality of the PHOS4, PPrASIC and LVDS serialiser chips;
- Additionally, it holds:
  - **one EEPROM** device (back side) to store the configuration file of the FPGA;
  - **one SignalGenerator** electronics circuit to act as an on-board test facility.



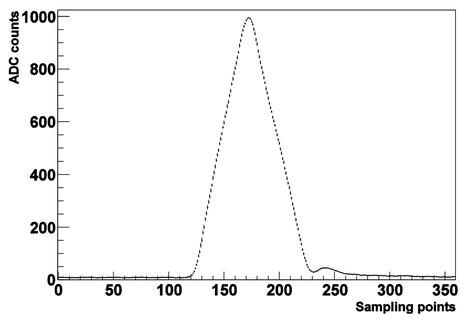
- the functionality of the first nMCM prototype has been tested on the PPM motherboard in the KIP laboratory. Preliminary results from these tests are presented below:



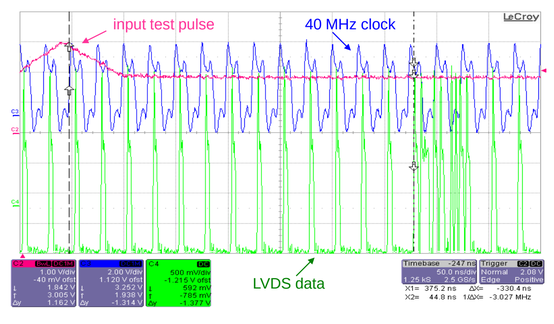
ADC noise tests: mean RMS and mean Peak-to-peak values are below 1 GeV in each trigger channel



LVDS transmission tests at 480 Mbit/s (left) and 960 Mbit/s (right)



Fine-timing tests: pulse reconstruction with 1.042 ns resolution



PPM latency measurements with the nMCM, from the output of the AnIn board to the output of the PPM. The measured value is 330 ns (equivalent to 13 BCs), similar to that obtained with the current MCM (i.e. 325 ns)

- functionality of the PPrASIC, PHOS4 and LVDS serialisers has been successfully implemented and tested in the Spartan-6 FPGA;
- nMCM to be reviewed by the end of 2012 ;
- mass production to start in spring 2013.