Contribution ID: **33** Type: **Poster**

The Upgrade of the PreProcessor System of the ATLAS Level-1 Calorimeter Trigger

Tuesday, 18 September 2012 17:46 (1 minute)

The ATLAS Level-1 Calorimeter Trigger is a pipelined system to identify high-pT objects and to build energy sums within a fixed latency of ˜2 us. It consists of a PreProcessor, which conditions and digitises analogue calorimeter signals, and two object-finding processors. The PreProcessor's tasks are implemented on a Multi-Chip Module, holding ADCs, time-adjustment and digital processing ASICs, and LVDS serialisers. A pin-compatible substitute, based on today's technology, like dual-channel ADCs and FPGAs, has been built to improve the BCID and pedestal subtraction algorithms. Test results with the first prototype are presented.

Summary

The ATLAS Level-1 Calorimeter Trigger (L1Calo) is a hardware-based pipelined system designed to identify high-pT objects in the calorimeters of the ATLAS detector. The system receives and processes 7168 pre-summed analogue signals from the entire calorimetry, and provides results to the Level-1 Central Trigger Processor (CTP) within 2 us after the pp collision has occurred. The L1Calo consists of three subsystems: the PreProcessor, the Cluster Processor (CP) and the Jet/Energy-sum Processor (JEP). The PreProcessor conditions and digitises the 7168 analogue signals, extracts a corresponding digital transverse energy (ET) value from each pulse and identifies it with a specific bunch-crossing, and sends the results in parallel to the subsequent processors. The CP identifies electrons/photons and taus, while the JEP identifies jets and computes various energy sums. Results of these investigations are sent to the CTP for the final Level-1 trigger decision. The PreProcessor is a compact, highly modular system consisting of 124 hardware-identical PreProcessor Modules (PPMs). Each PPM is designed to process 64 input analogue signals, and carries 23 daughterboards and several programmable devices. The main signal processing is performed on 16 four-channel Multi-Chip Modules (MCMs), each of which carries nine wire-bonded unpackaged dies: four ADCs to digitise the input analogue signals, one timing chip to adjust the phase of the ADC strobes with 1 ns resolution, one custom-built four-channel PreProcessor ASIC performing the trigger-specific data processing (synchronisation of the signals from the same bunch-crossing, noise suppression and pedestal substraction, bunch-crossing identification (BCID) and final ET calibration), and three LVDS serialisers for serial transmission of the digital ET values to the L1Calo processors at 480 Mbit/s.

The MCM technology decisions were taken more than a decade ago. At that time it was not feasible to have standard, packaged and flexible components which would meet all the design requirements. An MCM substitute, with the same functionality and similar form factor, has been built to profit from the state-of-the-art electronics and to enhance the flexibility of digital processing. Two dual channel 105MHz ADCs AD9218 are used for compact, packaged, fast, low noise and low power digitisation. A Xilinx Spartan-6 FPGA serves as flexible, low-cost, configurable digital processing unit, which takes over the functionality of the PreProcessor ASIC, of the time-adjustment chip and of the LVDS serialisers. The reprogramability characteristic of the FPGA device will allow to improve significantly the capabilities and the performance of the existing trigger-specific algorithms, which is likely to be required after the LHC upgrade to high luminosity, as well as to implement new functionalities: improved noise filtering and BCID algorithm for saturated pulses, separate ET calibrations for the electromagnetic and hadronic calorimeters, dynamic pedestal corrections, double data rate transmission (960 Mbit/s) to the JEP system. The first prototype of the new MCM has been already built and tested on the PPM motherboard, and detailed test results are presented in this work.

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Session Classification: POSTERS