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The GANDALF 128-channel Time-to-Digital Converter

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The GANDALF 6U-VME64x/VXS module has been developed to cope with a variety of readout tasks in nuclear physics experiments and is amongst others operated at the COMPASS experiment at CERN. Based on this platform, we present a 128-channel TDC which is implemented in a Xilinx Virtex-5 FPGA using the shifted-clock-sampling method. Compared to well-known FPGA designs based on delay-lines, usually comprising only few input signals, this concept permits the implementation of a large number of TDC channels with a mean time resolution of 77 ps in a single FPGA device.

Summary

The GANDALF mainboard comprises two Xilinx Virtex-5 FPGAs. The main FPGA (SX95T) allows for various data processing purposes, whereas the second FPGA (LX30T) is used for data output and for accessing the 144-Mbit QDRII+ and 4-Gbit DDR2 memory extensions. To perform different applications such as analog-to-digital or time-to-digital conversions, coincidence matrix formation and trigger generation, the signal inputs are placed on exchangeable mezzanine cards. Currently high-speed optical interface cards, 8-channel ADC cards as well as 64-channel digital input or output cards are available. GANDALF equipped with digital input mezzanine cards therefore allows for connecting up to 128 LVDS signals in parallel and thus the development of the system as a multichannel TDC.

The design objectives were to implement 128 TDC channels in the Virtex-5 FPGA on the GANDALF mainboard with a time resolution better than 100 ps for precise time-of-flight measurements. Dead-time free digitization, multi-hit capability and adequate hit buffer memory are mandatory. Furthermore, only hits within a variable time window around a given trigger signal are transferred to the output bus and thus to reduce the overall data transfer rate.

In previous TDC-FPGA projects, the input signal is routed through a delay-line, e.g. the dedicated carry chain, and the delayed signals are sampled by flip-flops with one common clock. As a result, the sampling clock period is subdivided into so called TDC bins. Using this concept, a time resolution of several picoseconds is achievable, but the logic consumption for 128 TDC channels would by far exceed the device resources.

For this reason, the shifted-clock-sampling algorithm is introduced: instead of delaying the input signal, the TDC register is sampled by a set of equidistant phase shifted clocks. Our design uses 16 phase shifted clocks with a base clock frequency of 388.8 MHz, which results in a TDC bin width of 160 ps. 8 clocks are generated by two PLLs and distributed via global clock nets across the FPGA. 8 more clocks are produced by locally inverting the clock signal with the clock inverter in every Virtex-5 Slice.

The uniformity of the TDC bins and thus the time resolution is limited by various factors that have to be taken into account during the FPGA implementation process. Main contributors are the sampling clocks phase shift error and the input signal routing skew of the TDC flip-flops. Because the implementation tools do not allow for selecting the routing of specific connections, minimizing the routing skew was a main challenge of this design. This could be achieved by evaluating different placement options of the FPGA flip-flops that form the TDC register. Once the optimal placement and routing inside the FPGA fabric was found, the results could be preserved and duplicated.

As the device utilization of the current design is quite moderate, future work concentrates on the integration of 128 scaler channels for beam profile measurements into the same design.

Primary author: BUCHELE, Maximilian (Albert-Ludwigs-Universitaet Freiburg (DE))

Co-authors: SCHILL, Christian (Albert-Ludwigs-Universitaet Freiburg); MICHALSKI, Christoph Daniel (Albert-Ludwigs-Universitaet Freiburg (DE)); HERRMANN, Florian (Albert-Ludwigs-Universitaet Freiburg (DE)); FISCHER, Horst (Albert-Ludwigs-Universitaet Freiburg (DE)); KONIGSMANN, Kay (Albert-Ludwigs-Universitaet

Freiburg (DE)); GORZELLIK, Matthias (Albert-Ludwigs-Universitaet Freiburg (DE)); JORG, Philipp Karl (Albert-Ludwigs-Universitaet Freiburg (DE)); SCHOPFERER, Sebastian (Albert-Ludwigs-Universitaet Freiburg (DE)); BAUMANN, Tobias (Albert-Ludwigs-Universitaet Freiburg (DE)); SZAMEITAT, Tobias Christian (Albert-Ludwigs-Universitaet Freiburg (DE)); KUNZ, Tobias (Albert-Ludwigs-Universitaet Freiburg (DE))

Presenter: BUCHELE, Maximilian (Albert-Ludwigs-Universitaet Freiburg (DE))

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