Power Pulsing schemes for vertex detectors at CLIC

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Abstract

The precision requirements of the vertex detector at CLIC impose strong limitations on the mass of such a detector (<0.2% of a radiation length, Xo, per layer). To achieve such a low mass, ultra-thin hybrid pixel detectors are foreseen, while the mass for cooling and services will be reduced by implementing a power-pulsing scheme that uses the low duty cycle of the accelerator. The principal aim is to achieve significant power reduction without compromising the power integrity supplied to the front-end electronics. A power-pulsing scheme is proposed for the analog electronics and its electrical features are discussed on the basis of measurements.

Vertex: Power consumption per ladder

The high density of channels implies a high power consumption. Taking advantage of the low duty cycle of the accelerator, the average power can be significantly reduced having the ASIC (CLICPIX) in a low consumption mode for most of the period, turning it on fully just for a small fraction of time around the bunch crossing.

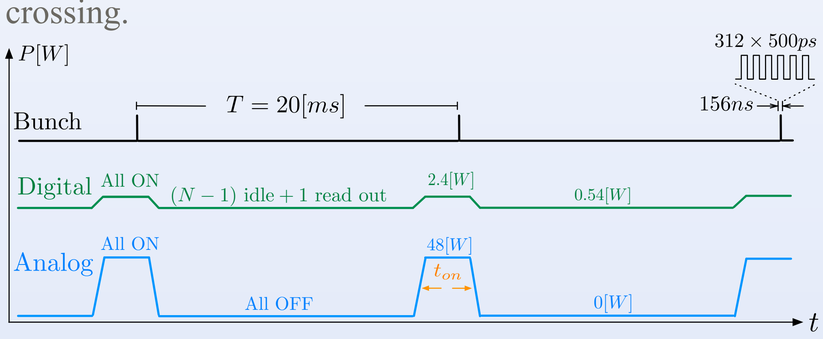

Figure: Analog and digital power consumption per ladder (N=24 ASICs)

Digital and analog power will be supplied separately. The latter is more challenging as it has a higher peak value and changes from no load to full load.

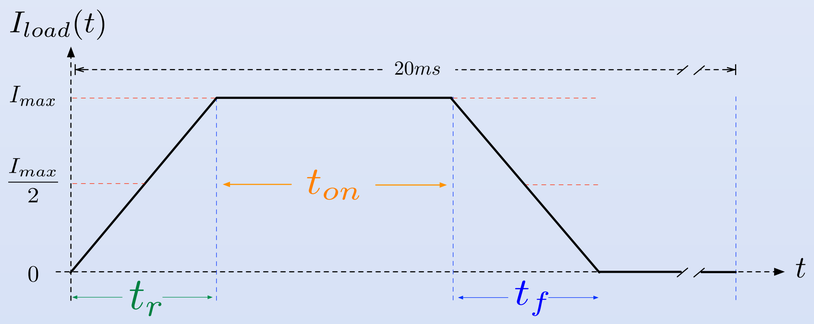

Figure : Analog Load Current

The on time, t_{on}, has to be long enough to turn on the analog electronics and to process the data. It is expected to be close to 15 µs. The rise and fall time, t_r and t_f, are in the order of few microseconds and can be defined by design in order to facilitate the power distribution.

Each ladder of the barrel will be powered symmetrically from both sides. A buck converter allows close regulation and to decrease the current in the back end power cables. The converter (~1%Xo) is placed 30 cm away, outside the vertex barrel region. A thin flex cable provides the power to the load.

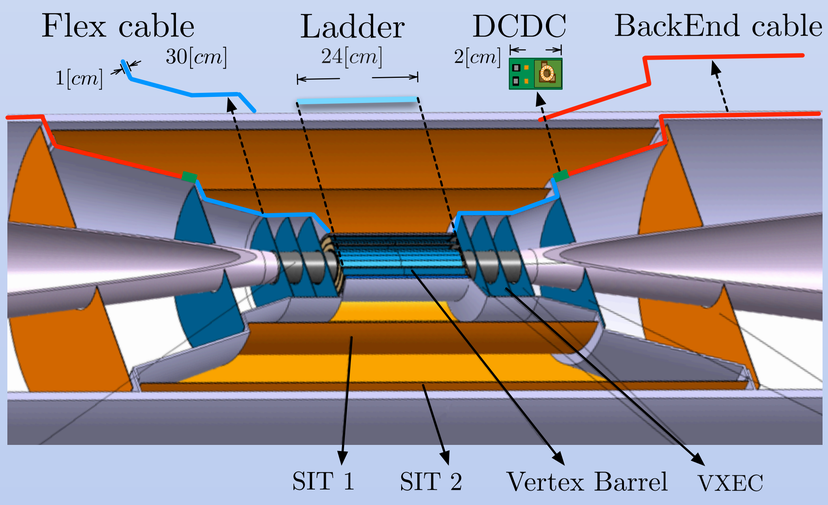

Figure : View into the vertex barrel and endcap (VXEC) pixel layers

The analog voltage required at the ladder is 1.2V, while the digital voltage could be decreased to reduce power consumption. To obtain higher efficiency and lower noise coupling, both will be supplied separately. This poster proposes a low mass pulsed-powering scheme for the analog electronics. The digital implementation will be addressed in a future work.

Challenges

Regulation: within 5% (60 mV) on the ASIC during the acquisition time, t_{on}, expected to be close to 15 µs.

Low losses: < 50 mW/cm^2 in the sensor area, as the heat-removal solution is based on air-cooling to reduce mass.

Material Budget: < 0.2%Xo for a detection layer, leaving less than 0.1%Xo for cooling and services.

High magnetic Field: > 4 [Tesla] restricting the use of ferromagnetic material.

Proposed powering scheme

Several schemes were studied and most of them resulted not to be viable due to excess of material. On the other hand, local regulation seemed to be necessary in order to accomplish the required regulation while supplying more than 20 A along 12 cm of thin cable. The proposed scheme consists of a buck converter placed outside the vertex barrel region, connected through aluminum flex cables to a local regulation based on LDOs and silicon capacitors. The latter are fundamental for material mass reduction.

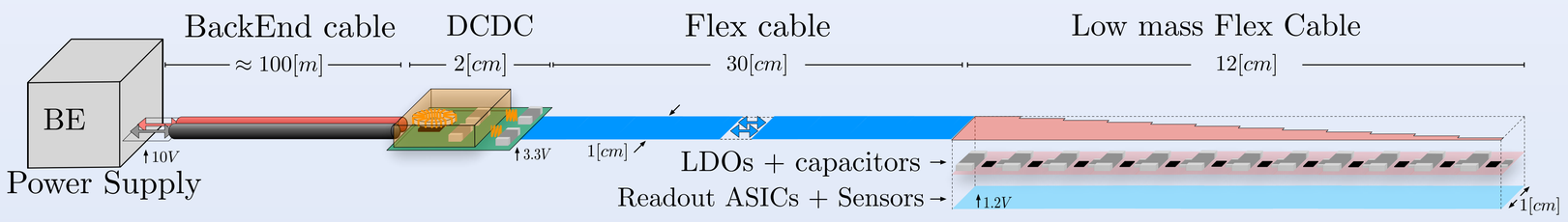

Figure: Half ladder proposed powering scheme

Implementation

The front end readout ASICs are now under development. In order to test the proposed pulsed-powered scheme, their behavior was emulated using an array of MOSFETs commuting at the expected values of current and duration. For convenience the low mass flex, LDO's and capacitors were included. The dimensions were maintained very close to the expected ones.

A commercial buck DCDC converter with air core inductor was used and a 30 cm flex cable of around 50 µm thickness was manufactured.

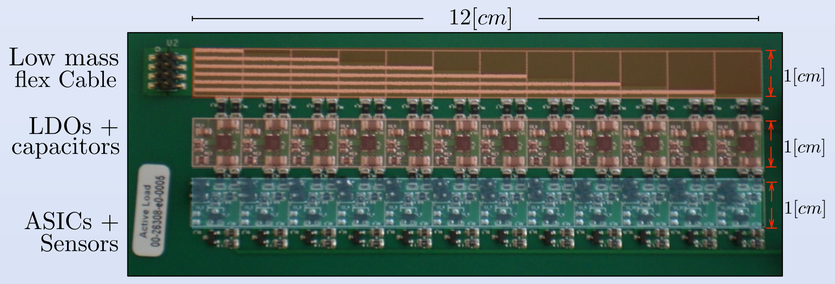

Figure: PCB that emulates the readout ASICs power consumption. It integrates the low mass flex cable, the array of LDOs and capacitors, and their interconnections.

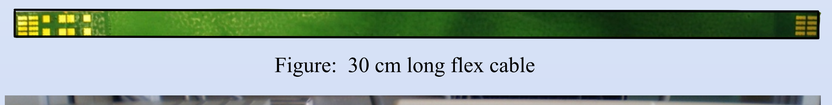

Figure: 30 cm long flex cable

Regulation

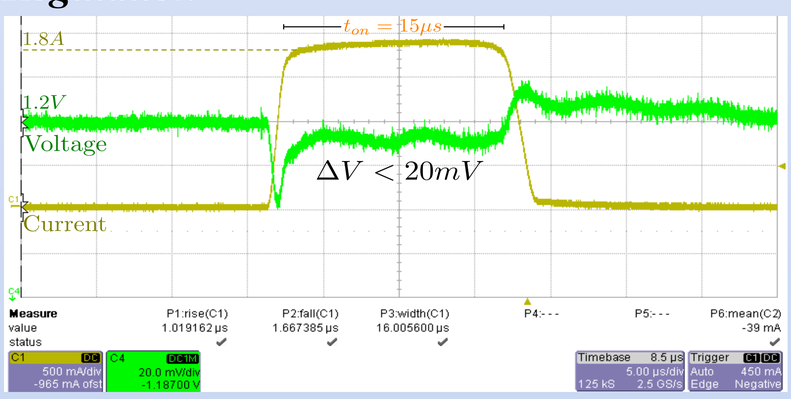

Figure: Measured regulated voltage at the last ASIC

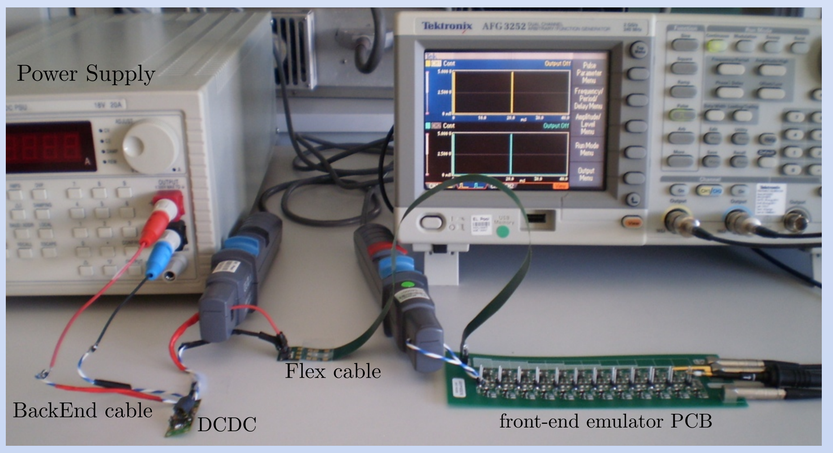

Figure : Implemented setup

The regulated voltage at the last ASIC was measured for t_{on}, t_r, and t_f equal to 15 µs, 1 µs and 1.5 µs, respectively. It is reasonably constant during the on-time, having less than 20 mV of drop during the "plateau", which was achieved using low mass silicon capacitors of 1 µF at the output of the LDOs.

Power Losses

The power losses of the most important components of the scheme were measured for two different conditions:

Power losses	BE cable	DCDC	Flex Cable	FE System Board
[mW]	2.2	267	6	200
[mW/cm2]	0.0042	66.75	0.2	16.7

Table: LDOs ON for the whole period

Power losses	BE cable	DCDC	Flex Cable	FE System Board
[mW]	1.3000	328	6.2	55.0
[mW/cm2]	0.0025	82	0.2	4.58

Table: LDOs ENABLED just for 250 us

To enable the LDOs for a short fraction of time allows reducing the losses in the ladders area (which are critical), as it reduces the unnecessary power burnt by the LDOs at no load condition (which was high for these particular LDOs).

Material Budget calculation for the powering of the ladder area

Part Name	Material	X0 (mm)	length (mm)	width(mm)	thick (mm)	Number	factor	h eq (mm)	% X0
Flex cable dielectric	Kapton	286	120	10	0.05	1	0.54	0.027	0.009
Flex cable layers	Aluminium	88.9	120	10	0.054	2	0.54	0.059	0.066
Input LDO Capacitors	Silicon	93.6	3.2	1.6	0.1	120	1.00	0.051	0.055
LDO regulator	Silicon	93.6	3	3	0.1	12	1.00	0.009	0.010
Output LDO Cap SMD 1206	Silicon	93.6	3.2	1.6	0.1	12	1.00	0.005	0.005
									0.145

Table : Material Budget calculation for the powering of the ladder area, with today's configuration equivalent electrical properties

With today's implementation we achieved a low material solution. Nevertheless, it exceeds the material target due to the high contribution of the flex and the input capacitors. There is still room for improvements (see **Future work**).

Conclusions

A low mass pulsed-powering scheme was proposed for the analog electronics of the future CLICPIX ASIC of the CLIC vertex detector.

The proposed scheme fulfills the regulation requirements, having a voltage drop during the acquisition time of less than 20 mV.

The power losses showed to be well bellow the 50 mW/cm^2 (4.58 mW/cm^2) in the sensor area, leaving enough margin for the digital electronics losses which are expected to be larger.

The material budget showed to be close but above the target. Nevertheless, the approach of using silicon capacitors and aluminum flex cables seems to be the only way to satisfy the material budget requirements.

Future Work

1) To reduce the losses contributed by the DCDC Buck converter: The first approach will be to enable it just during a short period of time, similarly to what was done with the LDOs. A second option will be to use a fixed on-time converter to efficiently manage both full and no load conditions.

2) To reduce the material budget: The flex cable and input capacitors showed to be the biggest contributors to the material budget. For that reason, we will manufacture low mass aluminum flex cables of close to 15 µm thick layers, reducing its mass contribution to 1/3. Secondly, we will study the possibility of reducing the input capacitor value and to obtain higher density silicon capacitors.

3) To propose a powering scheme for the digital electronics, estimating its losses and material budget contribution. The latter is expected to be much lower than for the analog electronics.