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# Power pulsing schemes for vertex detectors at CLIC

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The precision requirements of the vertex detector at CLIC impose strong limitations on the mass of such a detector (<0.2 X0 per layer). To achieve such a low mass, ultra-thin hybrid pixel detectors are foreseen, while the mass for cooling and services will be reduced by implementing a power-pulsing scheme that uses the low duty cycle of the accelerator. The principal aim is to achieve significant power reduction without compromising the power integrity supplied to the FEE. Different power-pulsing schemes are proposed and their electrical features are discussed on the basis of simulations and measurements.

## Summary

The vertex detector is the innermost detector at CLIC, and it is composed by several pixel sensors and readout ASICs arranged in "ladders". Its high density of channels implies a high power consumption that impacts strongly on the required low material budget of the detector. To cope with this and in order to reduce the cable and cooling material at close proximity of the detector, the average power has to be reduced. This can be achieved by means of delivering the power to the front-end electronics as function of the bunch crossing occupancy within a beam cycle. At CLIC, the collisions are intended to occur during each bunch crossing, that lasts 156 ns and that takes place every 20 ms. The readout ASICs can then be active during a time window containing the bunch crossing and remain idle in the other part of the cycle, reducing in that way the average power. The use of the beam duty cycle to reduce the average power is known as power pulsing.

The use of a power pulsing scheme implies that the current has to change suddenly from its idle value (few hundreds of mA) to full load (about 20 Amps) in few microseconds, and then remain constant for enough time to process the events (few tens of microseconds) to finally drop back to the idle current value. During the bunch crossing, the power consumption is at its maximum and constant, and the supplied voltage has to remain within 5% of the nominal voltage in order to allow a correct functioning of the readout ASICs. The latter is particularly challenging, considering the big transient that takes place before the readout process.

Each "ladder"has an active area of around 25 cmˆ2 that consumes close to 50 Watt when active and around hundred times less during the idle time. In order to provide the desired voltage, point of load regulators must be placed close to the FEE. However the material budget constraints makes that those voltage regulators must sit tens of centimeters away of their load, being connected to the FEE by thin and long cables optimized to reduce material contribution.

To cope with these restrictions while satisfying the power requirements, different power pulsing schemes are proposed in this paper. Their electrical features are discussed and compared on the basis of system efficiency, material contribution and voltage regulation. Some of the evaluated schemes are:

- DCDC converter at suitable location with remote sensing compensation.
- DCDC converter with decoupling and storage capacitor networks.
- Constant current charge storage scheme.

The efficiency and voltage regulation of the proposed low mass power pulsing schemes are obtained by means of simulations and experimental measurements on reference setups.

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