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Development of a Readout System for the PANDA Micro Vertex Detector

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The Micro Vertex Detector (MVD) is the innermost tracking detector of the PANDA experiment at the upcoming FAIR facility in Darmstadt. The detector consists of several layers of silicon pixel and strip sensors to obtain precise tracking of charged particles.
For the development of a front-end ASIC a flexible and powerful readout system was developed to interface different ASIC prototypes.
We will present the upgrade of the FPGA-based Jülich digital readout system and measurements of the recent MVD pixel front-end prototype ToPix3. Tests of the implementation of the radiation hard GBT transfer protocol are also shown.

Summary

PANDA is one of the main experiments at the upcoming Facility for Antiproton and Ion Research (FAIR) in Darmstadt. The fixed target experiment will explore antiproton proton annihilation with intense, phase space cooled beams with momenta between 1.5 and 15 GeV/c.
The innermost detector of PANDA will be the Micro Vertex Detector (MVD) which consists of several layers of silicon pixel and strip sensors to obtain precise tracking of charged particles.
A dedicated front-end ASIC has to be developed for the MVD to be able to handle the enormous amount of data which has to be read out to the control room without a trigger signal. The data transport should be done by the GBT protocol and the radiation hard components of the Versatile Link group to reduce errors in the data transmission due to the high radiation environment.

For the testing of different front-end prototypes and larger detector components, a powerful and flexible readout system had to be developed which allows an easy adaptation to the different interfaces of the front-end electronics.

Thus, an FPGA based readout system was developed to easily investigate different types of front-end prototypes for the pixel and strip sensors - the Jülich digital readout system.
The flexibility of the system is achieved with a modular design of hardware, firmware and software.
The firmware, i.e. the FPGA configuration, is written in VHDL. The software framework is written in C++ and declares different communication layers for easy hardware access.
To meet the requirements of the upcoming full size prototypes and online analysis, the custom made Xilinx Virtex4 based readout board was replaced by a Xilinx ml605 evaluation board with a Virtex6 FPGA as the central hardware component. Measurements with the upgraded system have been made with the ToPix2 and ToPix3 MVD pixel front-end prototypes.
To extend the readout system towards the final detector readout concept, the radiation hard optical GBT protocol was implemented into the firmware. First tests to readout the recent prototype ToPix3 via the GBT protocol have been done. For the next prototype ToPix4, a direct interface to the GBT protocol is planned to build up a realistic readout chain for the MVD.

We will present the concepts and the upgrade of the FPGA based Jülich digital readout system and measurements of the recent MVD pixel front-end prototype ToPix3. First tests of the implementation of the radiation hard GBT transfer protocol are also shown.

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