Further Development of the MTCA.4 Clock and Control System for the EuXFEL Megapixel Detectors

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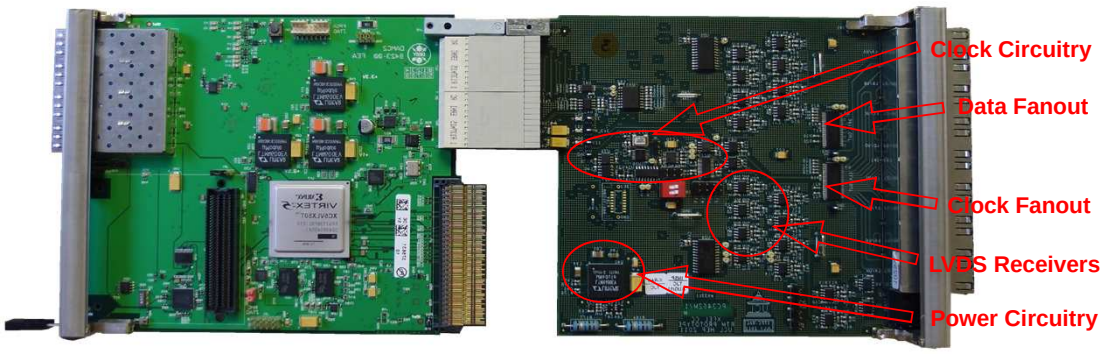
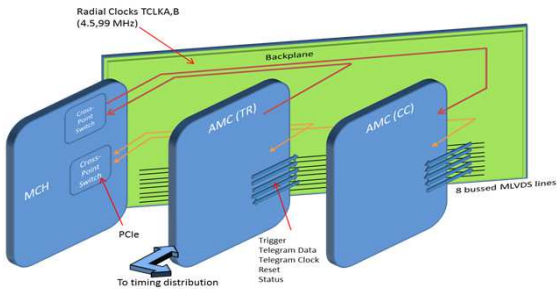
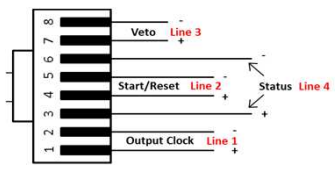
A combination of a general purpose MTCA.4 AMC board and a compatible Rear Transition Module make up the hardware for the Clock and Control (CC) system for the European Free Electron Laser (EuXFEL) megapixel detectors. The AMC board is the DESY designed DAMC2, which has a Xilinx V5LX50T FPGA to provide processing power. The RTM is a custom designed PCB that provides the connectivity to the Front End Electronics (FEE) units at the detector end.

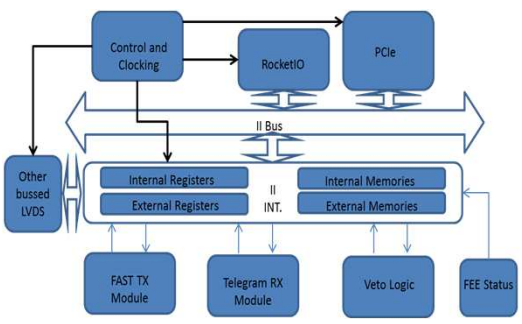


The CC system is responsible for the synchronisation of the detectors and the DAQ system to the general EuXFEL timing. The EuXFEL facility will generate coherent and intense X-ray flashes with a ~4.5 MHz bunch frequency. The Timing Receiver (TR) board housed in the same crate as the CC system delivers the bunch clock to the CC through the MTCA.4 backplane.



The link between a FEE unit and the CC system consists of 3 LVDS pairs to transfer the 99 MHz clock, FAST data and the VETO information and 1 pair to receive the status information from the unit. One CC RTM can support up to 16 FEE units which in turn support a 1 mega pixel detector.





The FPGA firmware for the CC system is built around a bus/register structure called the II Bus, whose registers are accessed through either the PCIe link to the crate processor or the blocks attached to the bus. The EuXFEL central software system controls the CC system through the PCIe link.

The FAST TX module generates the messages to the FEE units. Additional test modules can be attached to the II Bus such as the PRBS generator block which can be used to test the data link.

Telegram RX module receives the telegram data from the TR board through the MTCA.4 backplane and extracts the train ID numbers and the bunch pattern index values from the serial data received.

FAST MESSAGES TO THE FEE UNITS

Command	Start Bits	Payload	Purpose
START	1100	Train ID (32 bits) + Bunch Pattern Index (8 bits) + Checksum (8 bits)	Notifies FEE of coming train
STOP	1010	None	Notifies FEE that the train ended
RESET	1001	None	Reset FEE
Reserved	1111		

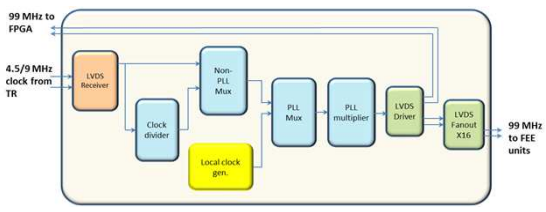
VETO MESSAGES TO THE FEE UNITS

Command	Start Bits	Payload	Purpose
VETO	110	Bunch ID (12 bits) + 0000	Identifies bunch ID to be vetoed
NO VETO	101	Bunch ID (12 bits) + 0000	No veto defined for that bunch ID
GOLDEN	111	Bunch ID (12 bits) + 0000	Identifies bunch as golden
Reserved	100	Bunch ID (12 bits) + 0000	

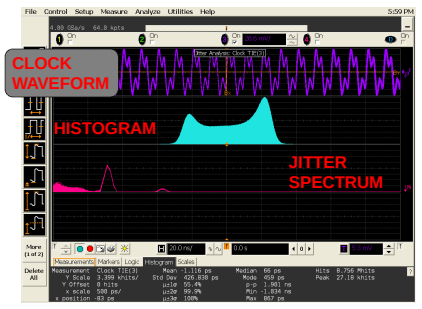
The CC system sends a data packet (FAST data) synchronously to the 99 MHz clock to the FEE units which includes synchronising information such as the start and the end of bunch trains along with the train ID numbers and the bunch pattern index values.

The Veto logic module processes the veto information coming through the SFPs and formats the data to be sent synchronously to the 99 MHz clock to the FEE units.

The clocking circuitry on the RTM includes a local crystal oscillator, PLL and non-PLL based multiplexers in order to provide an uninterrupted, stable clock to the final PLL which multiplies the bunch clock to provide the 99 MHz clock. This clock is then converted to differential and goes into a 1:16 LVDS fanout chip. A copy of this clock also goes back to the FPGA through the RTM connector.

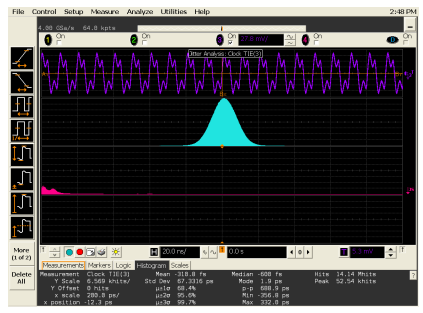


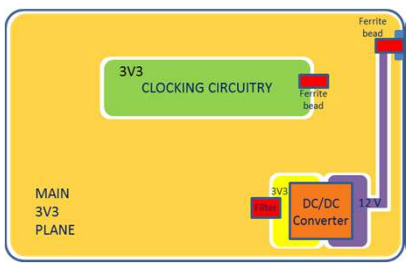
One of the most important performance metrics for the CC system is the jitter on the 99 MHz FEE clock. The jitter for this clock was measured using an Agilent MSO scope with the Agilent supplied jitter analysis software EZJIT. The types of jitter measured are the Time Interval Error (TIE), the period jitter and the cycle to cycle jitter. Only TIE results are shown here.



The current configuration of the CC RTM showed a high TIE and period jitter reading on the 99 MHz clock with the shape of the histogram suggesting a high amount of deterministic jitter. The jitter spectrum gives clues about the main source of the jitter. There is a high peak around the 780 KHz and a smaller peak at double this frequency. This corresponds to the switching frequency of the DC/DC converter, LTM4600EV. Therefore, the main jitter contribution comes from the ripple on the 3.3 V output from the DC/DC converter.

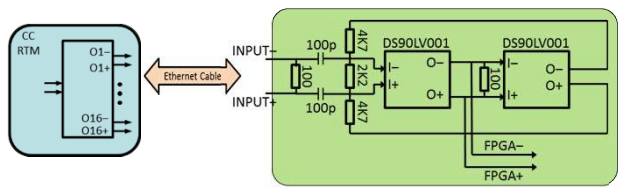
Further tests involved applying filtering on the 3.3 V rail to reduce the jitter readings. In order to do this, LTM4600EV was soldered on a small PCB and this PCB is attached to the CC RTM by cables so that it received the 12V RTM power from the DAMC2. The most promising jitter readings were obtained when a LC filter (1uH/1UF) is attached to the output of the DC/DC converter in addition to the required capacitors.





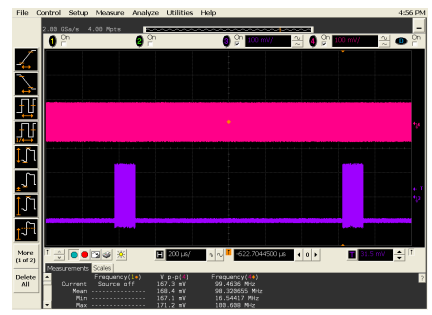
We envisage further improvements when this filtering scheme is employed on the final version of the CC RTM and the voltage plane for the clocking circuitry is separated from the main power plane by a ferrite bead.

Reliable data and clock transmission over long cables in the absence of a DC balanced data is an important performance metric. The space limitations in the experimental area necessitates long cable lengths.



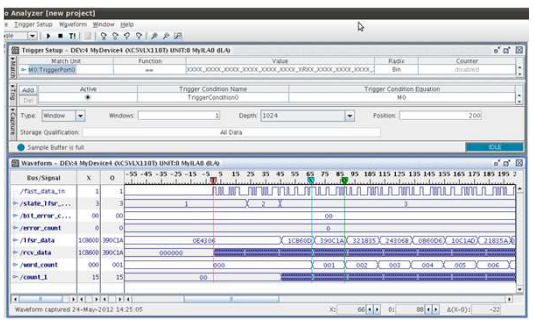
The clock and the data links to the FEE units are AC all coupled. Because the data sent to the FEEs is not DC balanced, a special circuitry on the receiver side is used to alleviate the DC wander. This circuitry limits the maximum cable length to be used for the FAST data link.

The tests involved using the worst case signal which would cause maximum DC wander on the AC coupled data link. The data is generated such that short bursts of 22–bit Pseudo Random Bit Sequence (PRBS) words are interspersed between long sequences ones or zeros. The sequence always starts with a predefined start word for synchronisation.

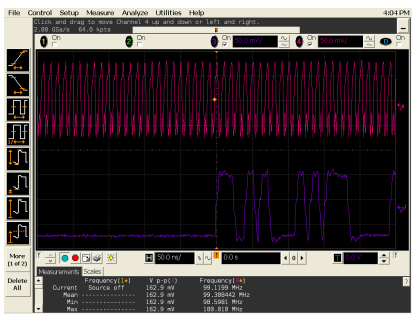


The receiving circuitry transfers the data to the FPGA on the receiver card and the data is compared to the data generated on the receiver card in tandem. In the receiver firmware there is a word and a bit error counter to observe the error rate. The Chipscope analysis software running on the receiver provides the ability to view the data transmission and the error rate.

DATA RECEPTION ON THE RECEIVER FPGA AFTER 30M CAT6 SFTP CABLE



CLOCK AND DATA AFTER 30M CAT6 SFTP CABLE AT THE RECEIVING FPGA INPUT



The tests were performed using Ethernet cables of lengths 10m, 15m, 20m, 30m and 50m. There were no errors observed during a period of more than 24 hours with the CAT6 SFTP cables up to 30m. If there is a need to support a 50m cable length MLVDS drivers are going to be tested for data and clock transmission.

This poster presents the initial performance related tests with the first prototype of the CC hardware and further development to improve the performance. Initial tests confirmed that the MTCA.4 solution involving a general purpose AMC and a RTM tailored for the specific functionality is valid for the 2D pixel detector clock and control system. The tests involving the actual FEE hardware and a prototype DAQ system integration test are being done and the final version of the CC hardware is currently being developed.

European XFEL

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