Contribution ID: **62** Type: **Poster**

Further Development of the MTCA.4 Clock and Control System for the EuXFEL Megapixel Detectors

Tuesday, 18 September 2012 17:35 (1 minute)

The clock and control (CC) system for the EuXFEL megapixel detectors was presented in TWEPP 2011. It consists of a multipurpose MTCA.4 AMC card with an FPGA and a custom designed Rear Transition Module (RTM). This paper presents the experiences with the system since its first prototype and the development of the final hardware. Experiences with the hardware included the tests performed to evaluate the system functionality such as Front End Electronics (FEE) communication and the performance metrics such as the FEE clock jitter. The final version of the CC hardware along with the associated firmware are also presented.

Summary

The Clock and Control (CC) system for the EuXFEL megapixel detectors is based on a combination of a general-purpose MTCA.4 AMC board and a compatible Rear Transition Module (RTM), whose general structure was presented at TWEPP 2011. The CC unit sits in a MTCA.4 crate along with the timing receiver (TR) board and the crate CPU. At the detector end there are Front End Electronics (FEE) which transport the detector data to the train builder (TB) which in turn sends its data to the PC farm. The CC system is scalable by installing slave CC units in the same crate. The first prototype of the system was manufactured in early autumn 2011.
The firmware for the CC system is built around a bus/register structure called the II Bus whose registers are accessible through either the PCIe link or the functional blocks attached to the bus. The EuXFEL central software system controls the CC system through the PCIe block which provides the link to a CPU unit on the crate. The FAST data block on the firmware diagram generates the FEE messages whose further details are also presented. There are additional functional blocks for test purposes such as the Pseudo Random Bit Sequence (PRBS) generator block that is used to test the performance of the data link to the FEEs. The veto logic block's first function is to gather the data coming on the SFP inputs through the RocketIO module from the veto sources and to make decisions on which bunch data is to be rejected by the FEEs. The second function is to generate messages to be sent on the veto link to the FEEs.
After ensuring the correct power-on according to the MTCA.4 standards and basic functionality, various performance metrics were investigated by extensive tests. The tests involving PRBS data transmission over the LVDS data and clock link have been performed on different length of cables. They included continuous 22-bit PRBS patterns and relatively short bursts of PRBS patterns interspersed within longer periods of continuous zeros or ones to test the LVDS level-shifting circuitry on the receiving side. These will be explained in detail along with the diagrams. The tests measuring the jitter in the form of Time Interval Error on the 99 MHz clock were performed. The test point is at the first output of the 1:16 LVDS fanout buffer. The equipment consists of an Agilent MSO8104 scope with the EZJIT software and a 800 MHz differential probe. The details of these tests will be presented along with the modifications to get better jitter readings.
The final version of the CC system hardware will be presented along with the required modifications to the next version of the DAMC2 circuitry. This involves being able to supply the 99 MHz FEE clock to the CC slave boards in the same crate. The slave boards will have the same hardware as the master in order to reduce costs and design effort.

Primary author: MOTUK, Erdem (University College London)

Co-authors: POSTRANECKY, Martin (University of London (GB)); WARREN, Matt (University College London (GB)); WING, Matthew (UCL)

Presenter: COOK, Sam (University College London)

Session Classification: POSTERS