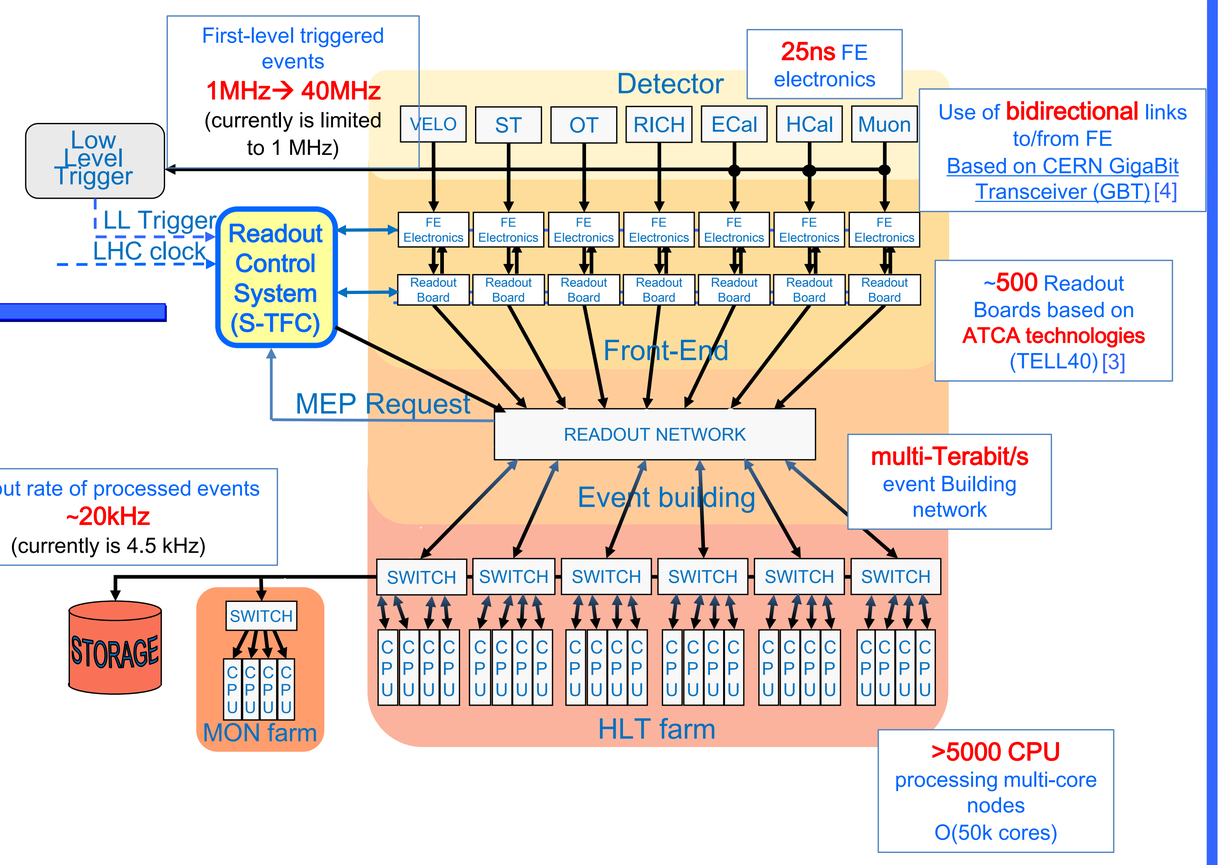
A new Readout Control System for the LHCb Upgrade at CERN

F. ALESSIO, R. JACOBSSON
CERN, Geneva, Switzerland

1. The upgrade of the LHCb readout system

Upgraded LHCb detector in 2018 to probe New Physics to a percent level
- run at x10 designed instantaneous luminosity, up to maximum $2*10^{33}$ cm^{-2} s^{-1}
- replace current sub-detectors with more rad-hard detectors, no spill-over, more granularity
- improve hadronic trigger efficiencies for luminosities above $2*10^{32}$ cm^{-2} s^{-1}

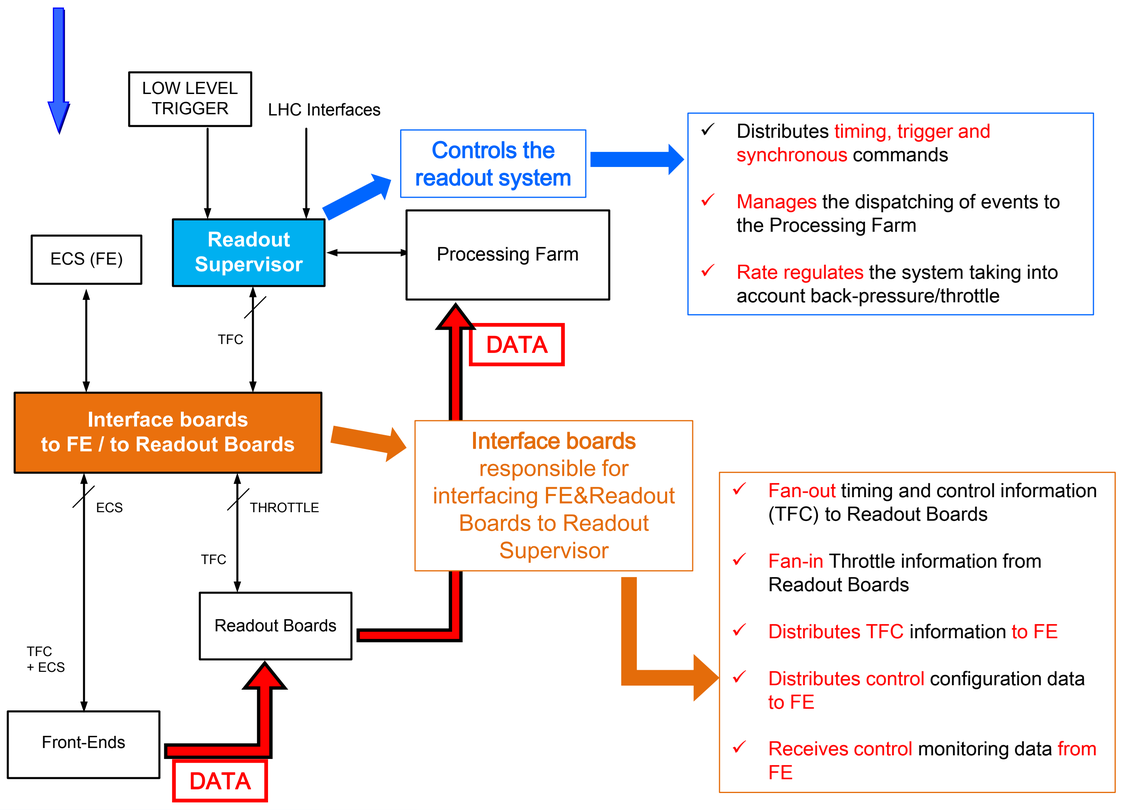
Read out each bunch crossing to the full LHC frequency of 40 MHz [1]:
- all detector data passed through the readout network every LHC clock cycle
- fully flexible software trigger analyzing events at 40 MHz and selecting them at > 20kHz



2. Upgraded Timing and Fast Control System

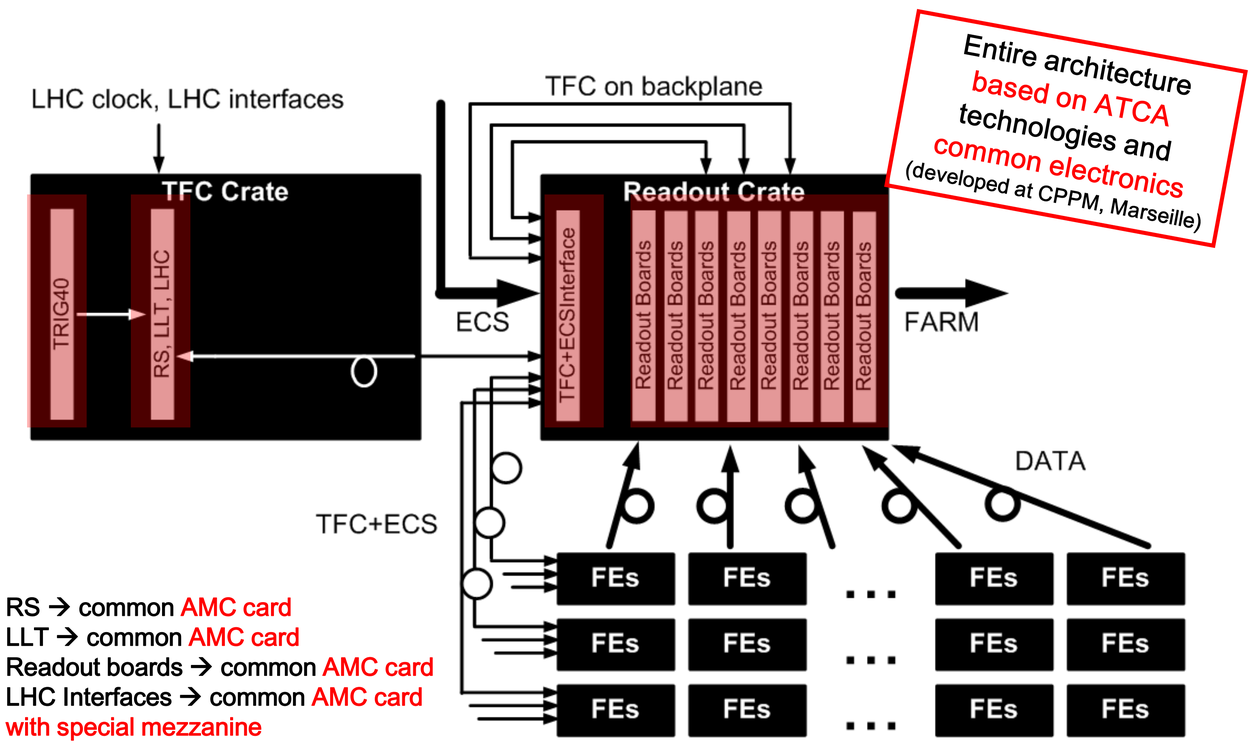
System and functional requirements of the new Readout Control System [2]

⇒ Bidirectional communication network
⇒ Low clock jitter, fully controlled phase and latency
⇒ Interface with the LHC
⇒ Connection with the Low Level Trigger
⇒ Events rate control
⇒ Destination control for the packets of events
⇒ Information about the registered events via an appended event data bank
⇒ Sub-detector calibration triggers
⇒ Partitioning to allow running any ensemble of the detector
⇒ Support and interface with the old TFC system. “hybrid” operation
⇒ Test-bench support and flexibility for early setups of upgraded sub-detectors



3. The physical upgraded TFC System

Physical representation of a partitioned readout slice in the upgraded readout system

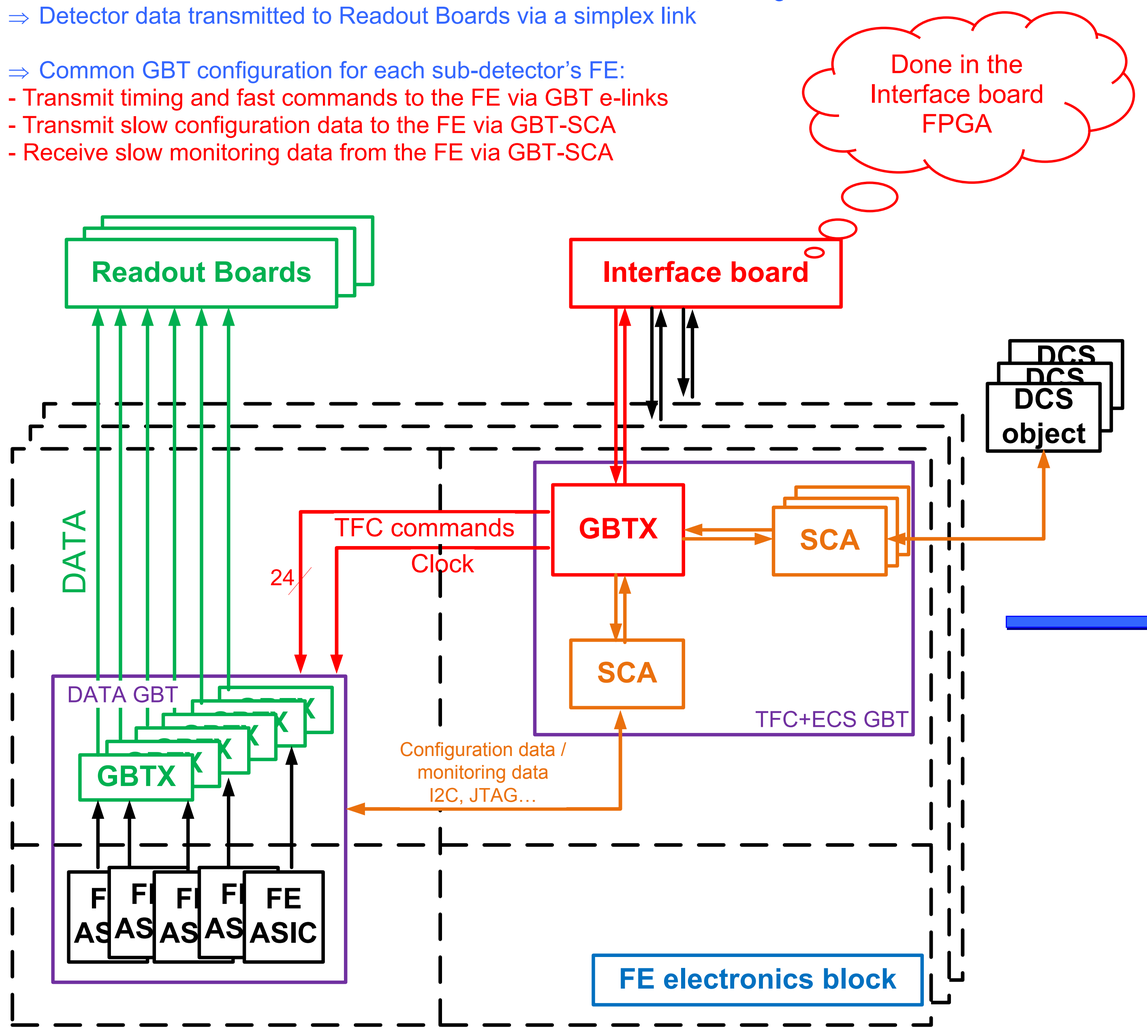


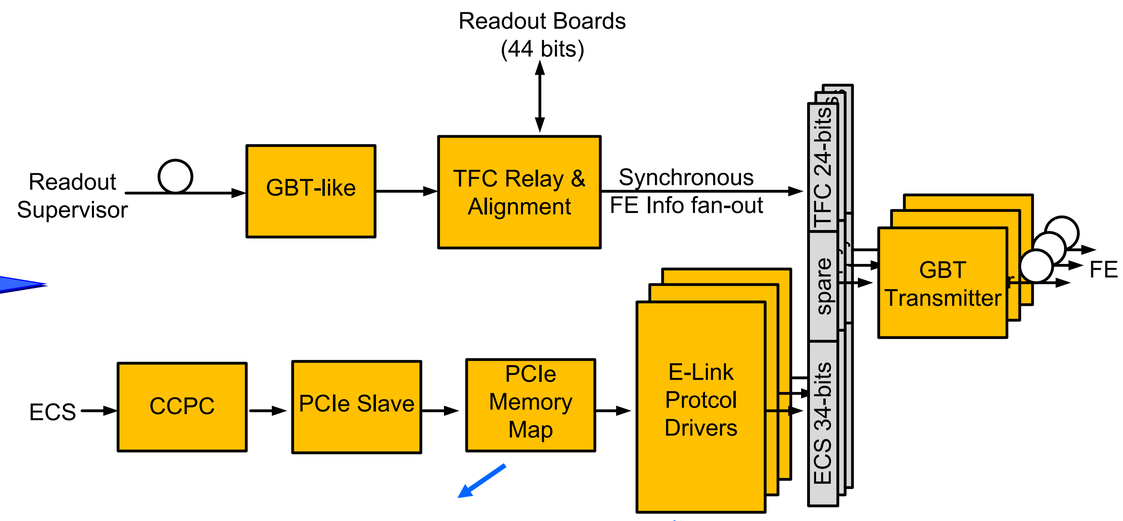
4. Timing, fast and slow control to the FE via GBT

Implementation of the new Readout Control system drives the GBT configuration at the FE

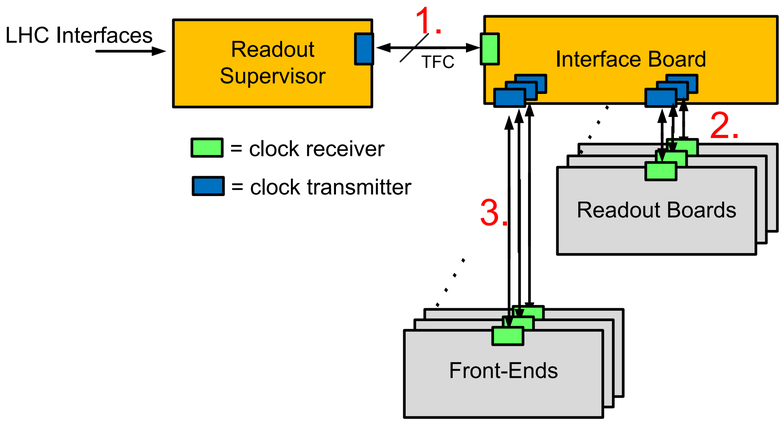
⇒ Transmit fast and slow control to the FE via the same GBT link, sharing the bandwidth
⇒ Detector data transmitted to Readout Boards via a simplex link

⇒ Common GBT configuration for each sub-detector’s FE:
- Transmit timing and fast commands to the FE via GBT e-links
- Transmit slow configuration data to the FE via GBT-SCA
- Receive slow monitoring data from the FE via GBT-SCA





5. Clock distribution via the new TFC system



Particular care must be given to the clock distribution in order to have full control of phase and latency across three types of links:

1. FPGA-to-FPGA links via optical fibers
   - need validation of FPGA technologies
2. FPGA-to-FPGA links via ATCA backplane
   - need validation of ATCA technologies
3. GBT-to-GBT links via optical fibers
   - include clock distribution to each FE chip

6. Future plans

First prototype of the new Readout Control system will be available end of 2012 [2]:

⇒ first version of Readout Supervisor and Interface boards’ FPGA code for LHCb test bench
  - based on a first hardware prototype developed at CPPM, Marseille [3]
⇒ first version of clock-level simulation framework for code verification and development

The system as planned allows “hybrid” operation of the LHCb readout system:

⇒ “old” and “new” together!
⇒ possible to install new sub-detector test-bench for commissioning after LHC first long shutdown
⇒ even possible to improve some of the LHCb physics potential between 2015-2018

References:
[1] K. Wyllie, F. Alessio, R. Jacobsson, N. Neufeld, “Electronics Architecture of the LHCb Upgrade”, CERN LHCb Public Note, LHCb-PUB-2011-011
[2] F. Alessio, R. Jacobsson, “System-level specifications of the Timing and Fast Control system for the LHCb Upgrade”, CERN LHCb Public Note, LHCb-PUB-2012-001
[3] J-P Cachemiche et al., “Study for the LHCb upgrade readout board”, JINST 5 (2010) C12036
[4] Moreira P et al., “The GBT Project”, Proceedings of TWEPP09, pp. 342-346