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A new Readout Control system for the LHCb Upgrade at CERN

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The LHCb experiment has proposed an upgrade towards a full 40 MHz readout system in order to run between five and ten times its initial design luminosity. The entire readout architecture will be upgraded in order to cope with higher sub-detector occupancies, higher rate and higher network load. In this paper, we describe the architecture, functionalities and the first hardware implementation of a new Readout Control system for the LHCb upgrade. The system is based on FPGAs and bi-directional links for the control of the entire readout architecture. First results on the validation of the system are given.

Summary

The LHCb experiment has proposed an upgrade towards a 40 MHz readout system in order to run between five and ten times its initial design luminosity, by improving the trigger efficiency. The entire readout architecture will need to be upgraded in order to cope with higher subdetector occupancies, higher rate and higher network load. Here, we describe the new architecture, new functionalities and the first hardware implementation of the new LHCb Readout Control system for the upgraded LHCb experiment.

The system is based on a single new Readout Supervisor which instantiates several masters to allow partitioning of the LHCb sub-detectors. In the upgraded scenario, the new Readout Supervisor is responsible for distributing the LHCb bunch clock, timing signals, and synchronous and asynchronous commands to the Readout Boards and the Front-End electronics, including the event destination information. Moreover, the new Readout Supervisor is responsible for the rate regulation of the system by taking into account back-pressure from the Readout Boards and the event filter farm. The communication with the Readout Boards is ensured by a shared high-speed bi-directional optical link network for both the distribution of timing and synchronous control information, as well as trigger/throttle communication. In this regard, a new Readout Interface board with fan-out capabilities for timing and synchronous information and fan-in capabilities for throttle and rate regulation of the system, interfaces the Readout Supervisor to the Readout Boards. Moreover, the Readout Interface board is responsible for distributing the timing and synchronous control information required by the Front-End electronics. We have also proposed that this board takes care of the exchange of Experiment Control System information with the Front-End electronics, by transmitting configuration data to the Front-End electronics in parallel to the readout control information, and receiving monitoring data from the Front-End electronics. The new architecture of the system also allows "hybrid"operation by supporting the old readout control system. This will allow the LHCb experiment to perform a staged upgrade of the readout architecture, by improving the performance of the old system up to the completion of the upgraded system.

We present here also a first hardware implementation of the system, based on a custom-made AMC card, compatible with the ATCA technology and developed at CPPM in Marseille (France). This electronics card is equipped with an ALTERA Stratix FPGA and transmitters/receivers for the distribution of data and commands via optical fibres, the ATCA backplane and an RTM module. In this paper, we outline the real-time implementations of the new Readout Control system, together with solutions on how to handle the synchronous distribution of timing and synchronous information in such a complex system entirely based on FPGAs and optical links in order to control the whole upgraded LHCb readout architecture. At the end, we also outline results from the first successful validation tests on the AMC board and the plans for the deployment of the system in the global LHCb upgrade readout architecture.

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