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Low-power High-Speed CMOS I/Os: Design Challenges and Solutions

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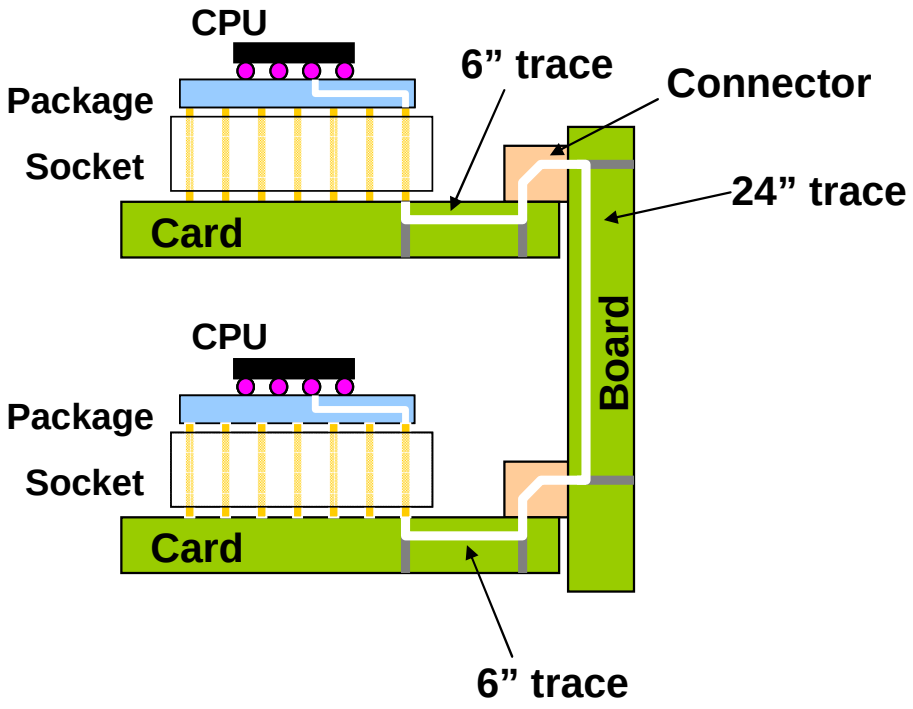
I/O Link Technology group @ IBM ZRL

What we do

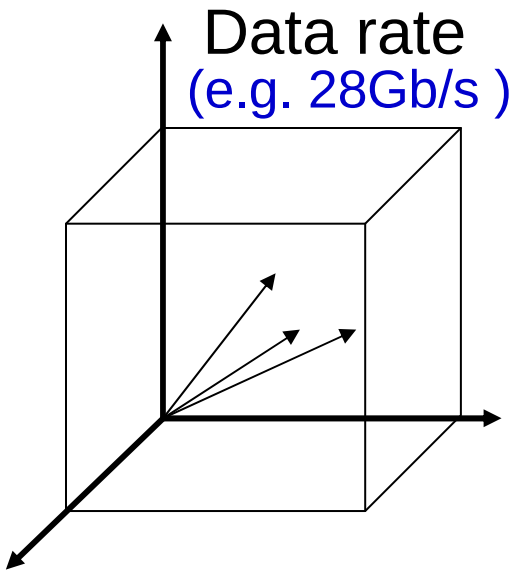
- I/O PHY circuit design
- backplane and chip-to-chip (e.g. processor, memory)

Technical goals to meet

- Distance: 10-100cm
- Attenuation: 10-40dB
- Data rate: 3-40 Gbit/s
- Energy/bit: <10pJ/bit
- Chip area : 0.1 mm^2



General research directions



Distance (=allowable channel attenuation
~equalizer complexity

(e.g. 28Gbit @ 30dB channel attenuation measured at $f_{baud}/2$)

Side conditions: chip area, testability, standard compliance, reliability etc.

Outline

- **Introduction**
  - **High-Speed I/Os in the wireline link space**
  - **Equalization techniques**
- **Low-power Transmitter**
  - SST vs. CML driver
  - Ultra-low power TX → Avoid TX-FFE
- **Low-power Receiver**
  - Power-optimal amplification
  - Incomplete Settling / Integrating Buffer
  - Low-power DFE Architecture
  - Low-power clock generation
- **Digital approaches**
  - ADC
  - DFE implementations
  - Analog vs. Digital

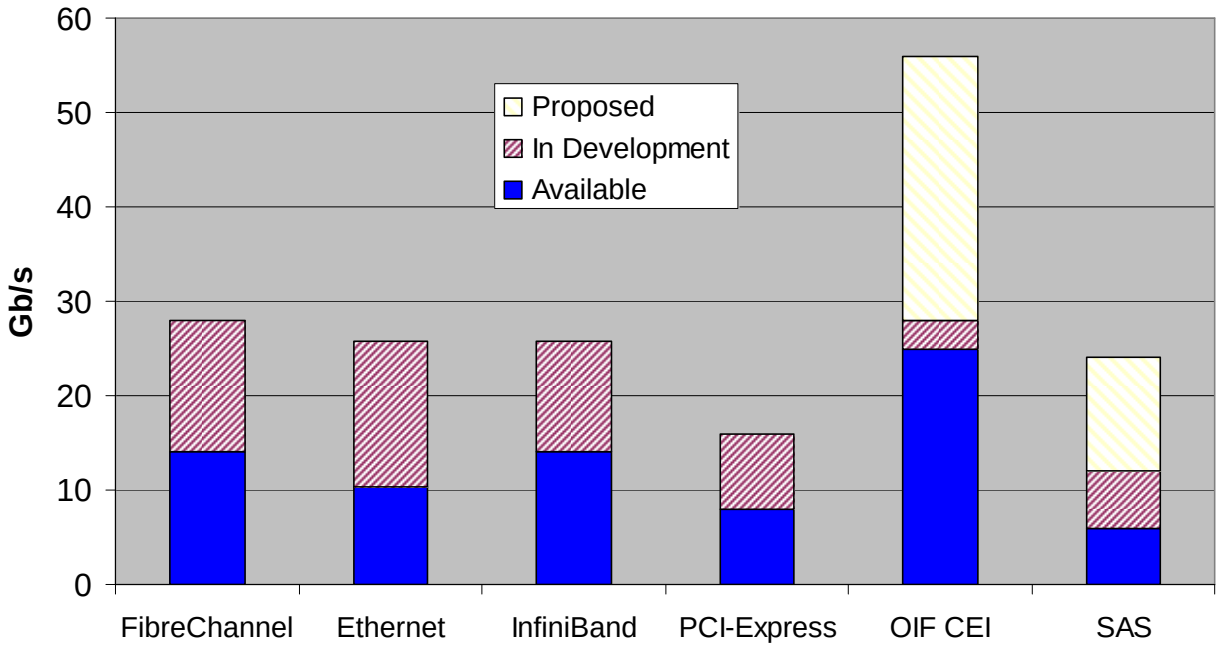
High-speed I/Os compared with other wireline links

	High-speed serial (backplane or chip-to-chip)	Gbit Ethernet 1000Base-T 802.3ab	10Gbit Ethernet 10GBase-T 802.3an
Bidirectional	-	YES	YES
Data rate/lane [Gbps]	3-20	2 * 0.25	2*2.5
Rate/channel BW (HSS=1)	1	2	10
Coding	NRZ	PAM-5 + Trellis	PAM-16 + LDPC
Equalization	≤5 tap FFE ≤15 tap DFE	12 tap FFE 14 tap DFE	16 tap THP
Echo canc	-	60 Taps	>200 Taps
X-talk canc	-	75 tap NEXT	NEXT+FEXT
Energy/bit	x1	x10	x50

Case #1 High-speed I/Os (up to now): Simple, analog, rather low-power
Case #2 Ethernet over copper: Digital (ADC) + lots of signal processing

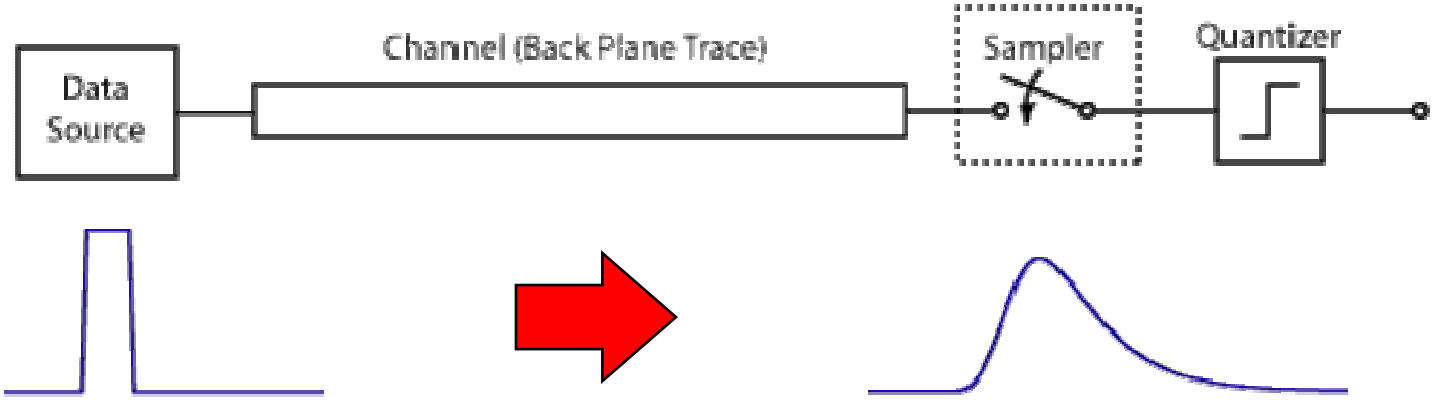
→ Goal: More complex equalization at low power

I/O Standards Roadmaps versus Data Rate

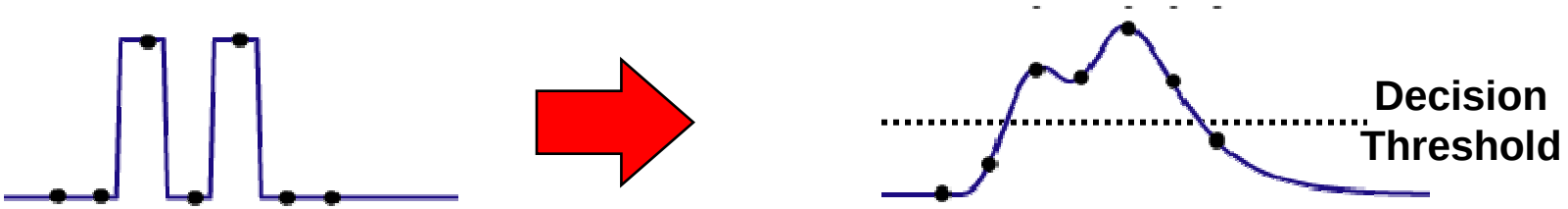


- **Current standards mostly in the 10-14Gb/s range**
  - OIF CEI pushing aggressively to 25G, still in “early adoption” phase
- **Expect most “major” standards to move to 25Gb/s regime within the next 12-18 months**
  - Ethernet, InfiniBand, FibreChannel all in development at those speeds

Background— Limited Bandwidth Channels Create Inter-Symbol Inteference; Equalization Required to Support High Data Rates



- **Dispersive nature of channel causes significant spreading of data pulse**

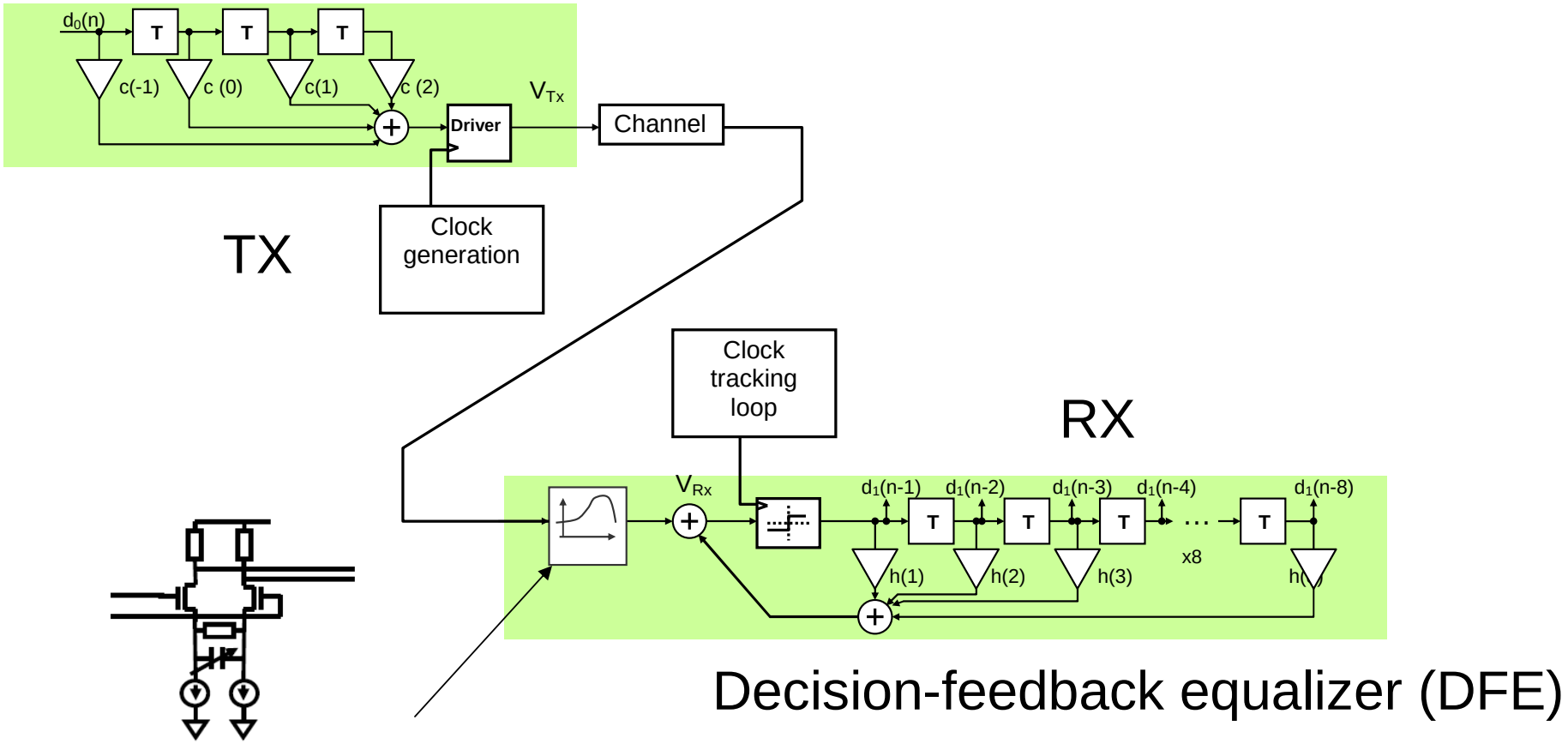


0 0 1 0 1 0 0 **0 0 1 1 1 1 0**

- **Adjacent symbols smear into each other, resulting in inter-symbol interference (ISI) and potential data errors**

Architecture of current high-speed I/Os

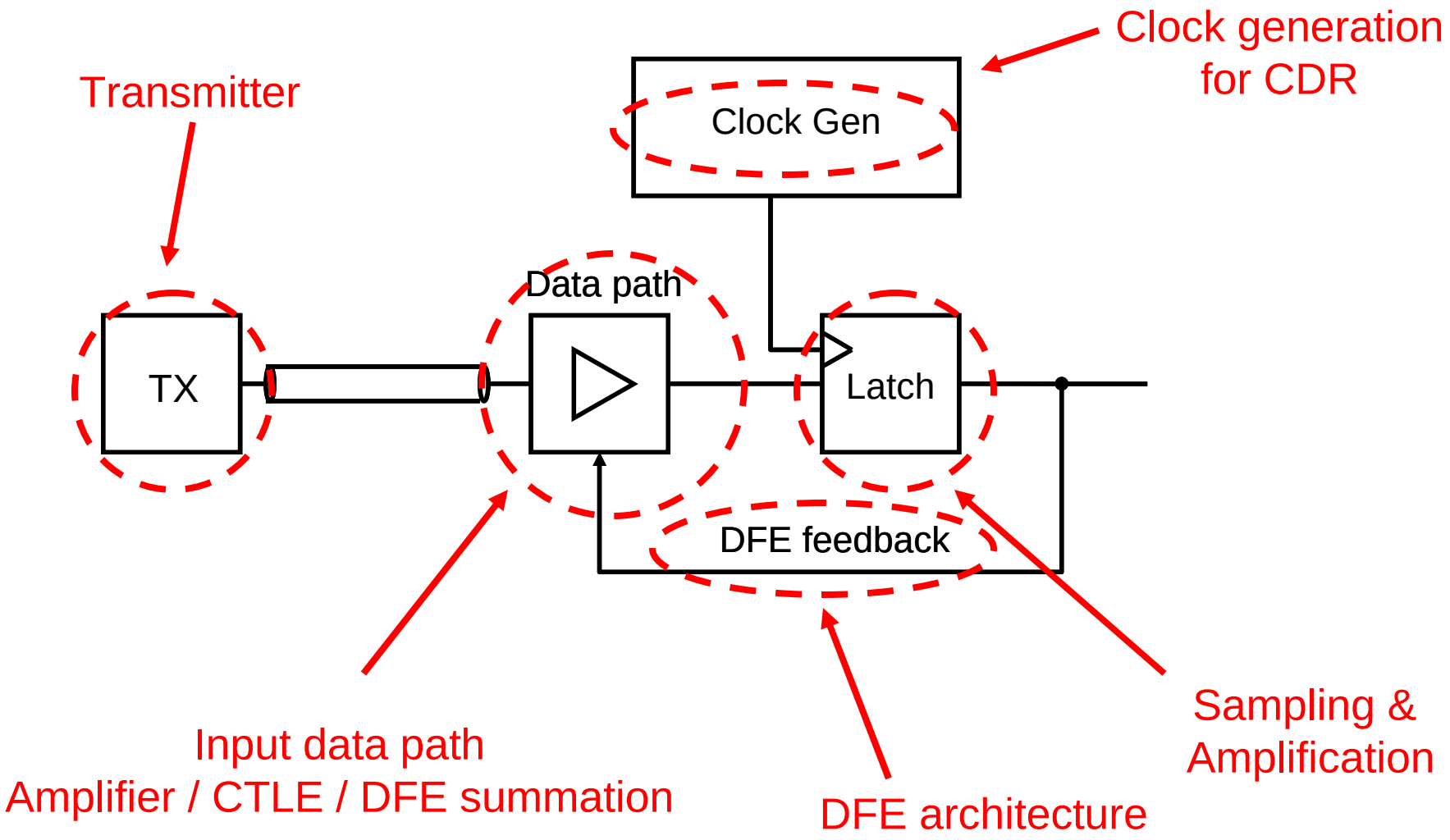
Feed-forward equalizer (FFE)



Decision-feedback equalizer (DFE)

Continuous-time linear equalizer (CTLE)

Low-power Design Areas



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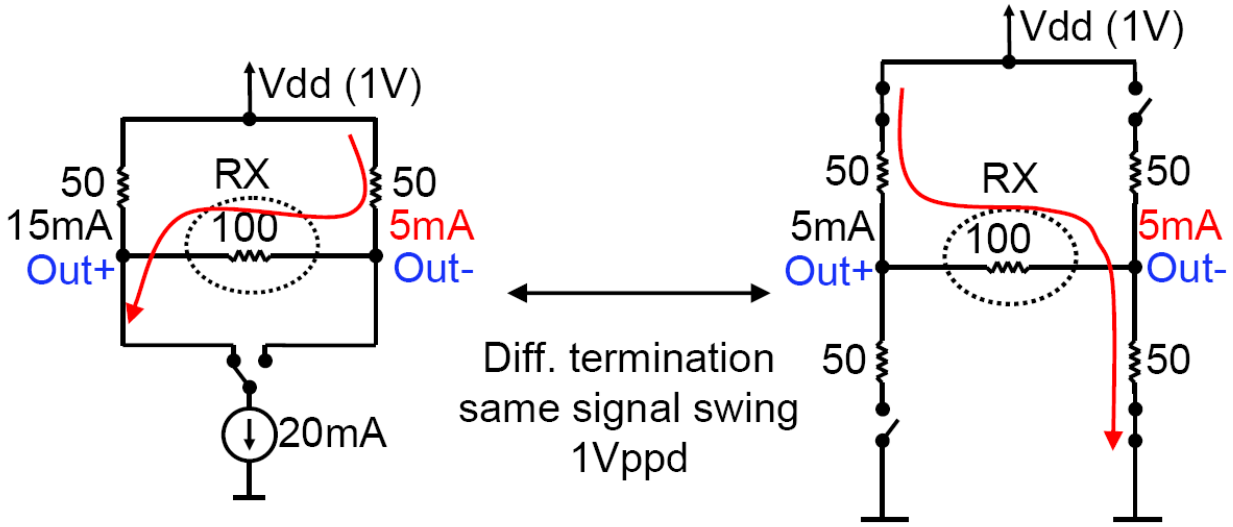
CML vs. voltage-mode (SST) driver



CML (Current mode logic)

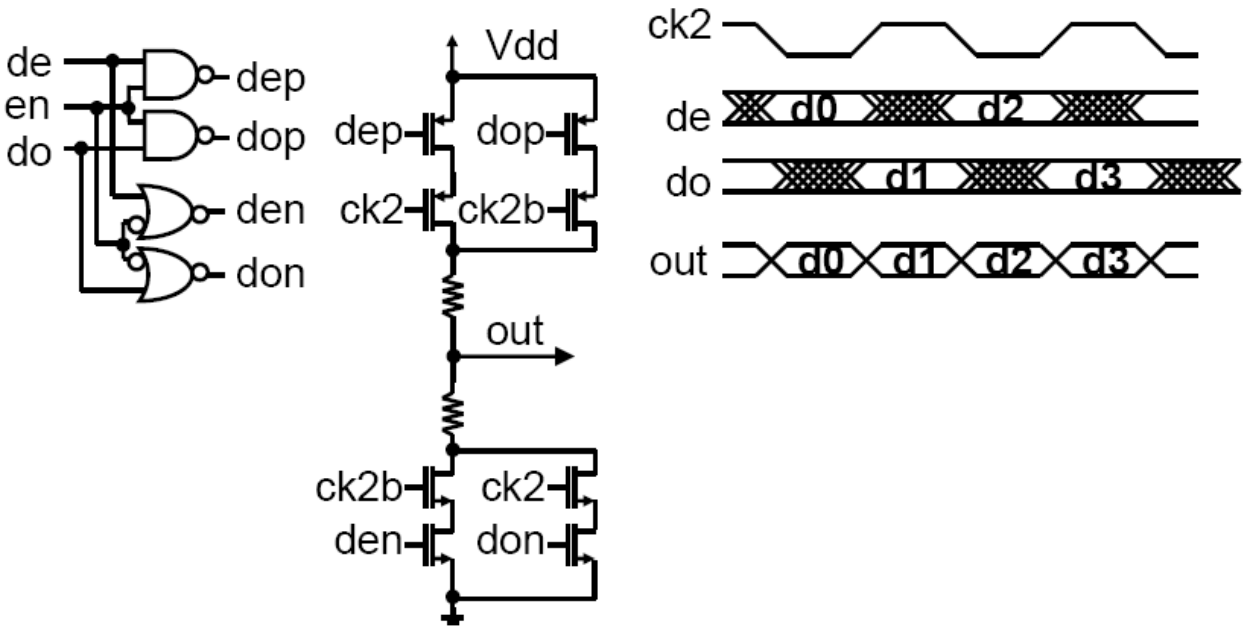
- **$1V_{ppd}$ swing**
- **Load current : +/- 5mA**
- **Total current: 20mA**

SST (Source-Series Terminated)

- **$1V_{ppd}$ swing**
- **Load current : +/- 5mA**
- **Total current: 5mA**

- Power is proportional to output swing in both cases
- SST driver allows different termination options (differential, to GND, to VDD)

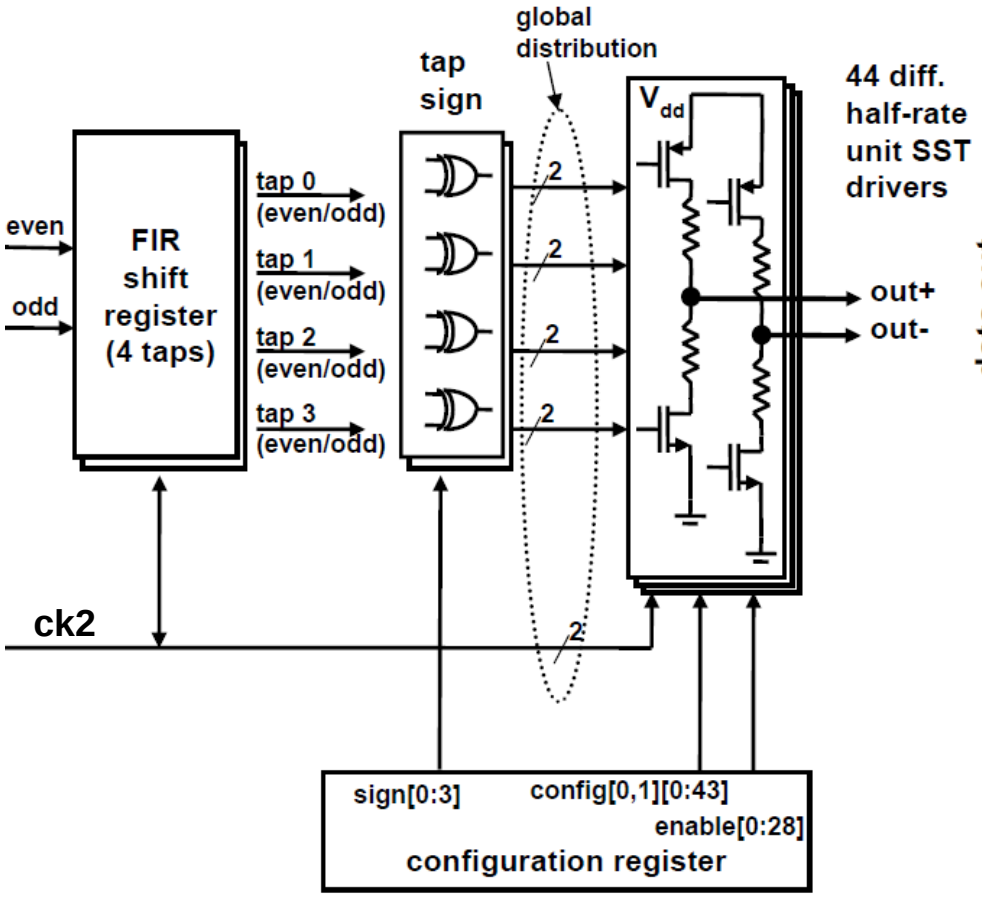
Half-rate SST Driver

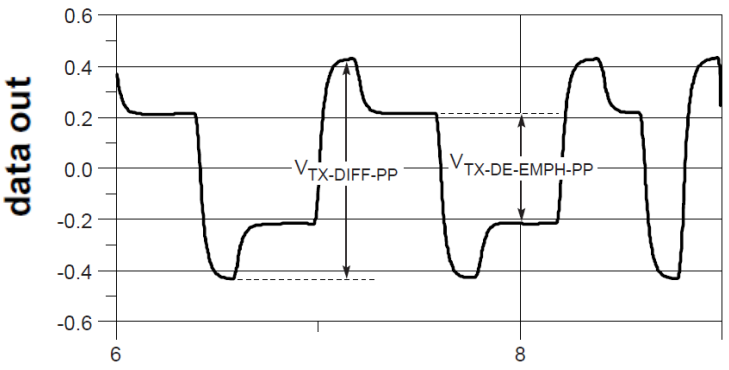


- Transistors are small due to large gate overdrive
- Small input capacitance → low power in pre-driver

C. Menolfi et al., "A 16Gb/s Source-Series Terminated Transmitter in 65nm SOI ," ISSC 2007.

TX with 4-tap Feed-forward equalizer (FFE)



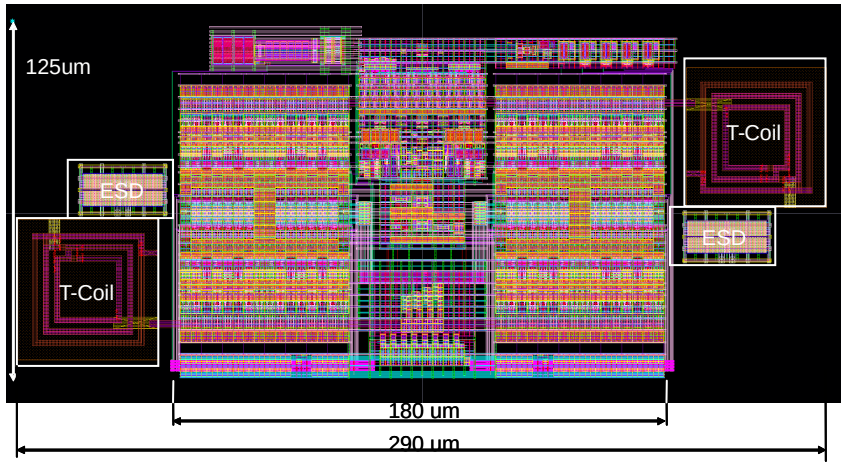


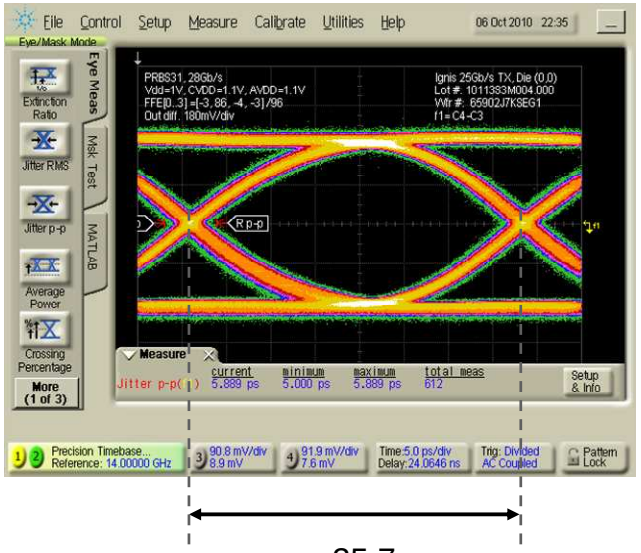
FFE waveform example

- 3.6 mW/Gbps @ 16 Gb/s and 1V swing

C. Menolfi et al., "A 16Gb/s Source-Series Terminated Transmitter in 65nm SOI ," ISSC 2007.

28 Gb/s SST-TX





- Operating speed: up to 28Gb/s at VDD_{min}=0.95V
- 4 tap bit-rate FIR feed-forward equalization (FFE)
- +/- 20ps programmable True/Comp. output skew (enabled by SST concept)
- +/- 5% Duty-cycle control
- Adjustable driver impedance
- Full ESD compliance: 2kV HBM, 100V MM, 250V CDM
- High-frequency impedance matching with on-chip T-Coils, <-10dB return loss
- Power consumption = 7mW/Gbps (175mW)

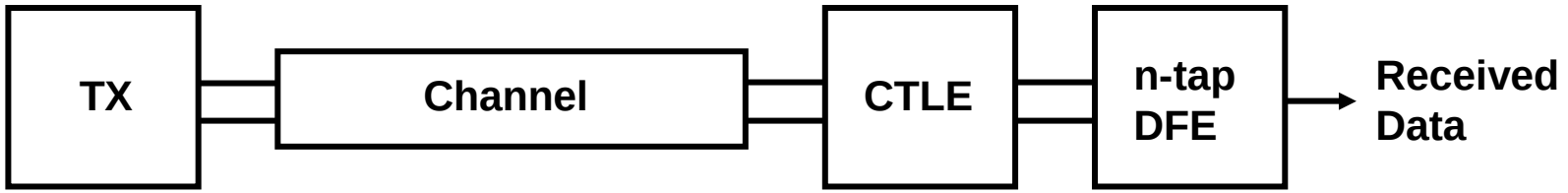
C. Menolfi et al., "A 28Gb/s Source-Series Terminated Transmitter in 32nm SOI“, ISSCC 2012.

Ultra-Low-power Transmitter Concept

- Equalization done on RX side only
- Avoid TX-FFE

  → (1) **Low power** (1mW/Gbps for TX for 1V swing)

  → (2) Less amplification of **TX clock jitter** (see next slides)

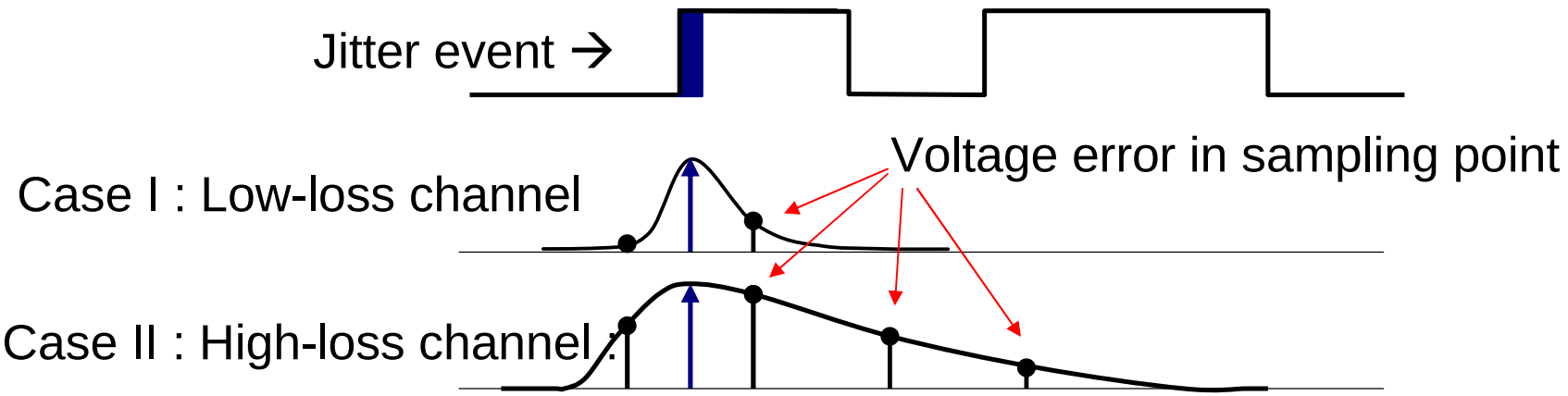


NO Feed-forward equalizer (FFE)

Continuous-Time Linear Equalizer (CTLE)

Decision-Feedback Equalizer (DFE)

Jitter Amplification in High-Loss Channels



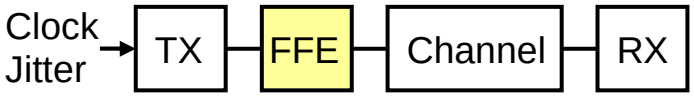
→Jitter is distributed along multiple UIs → Jitter amplification

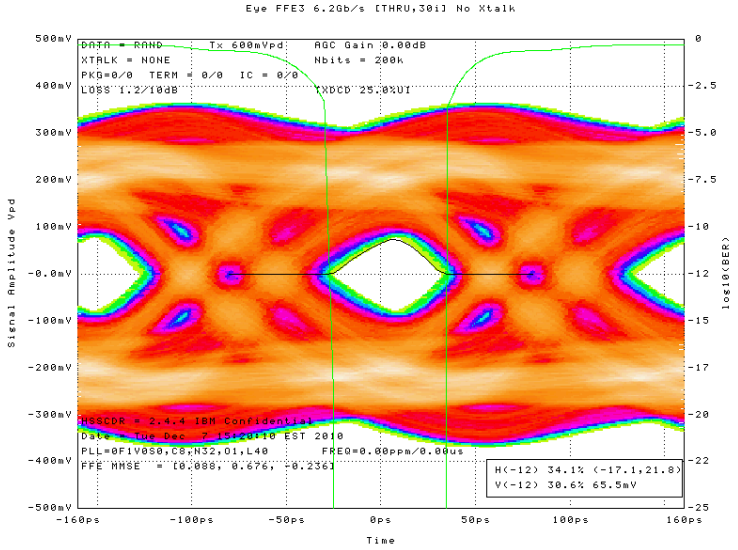
Case II can be converted to Case I by

(1) Continues time linear equalizer (CTLE) at RX side
(2) Continues time linear equalizer (CTLE) at TX side
(3) Discrete time RX FFE

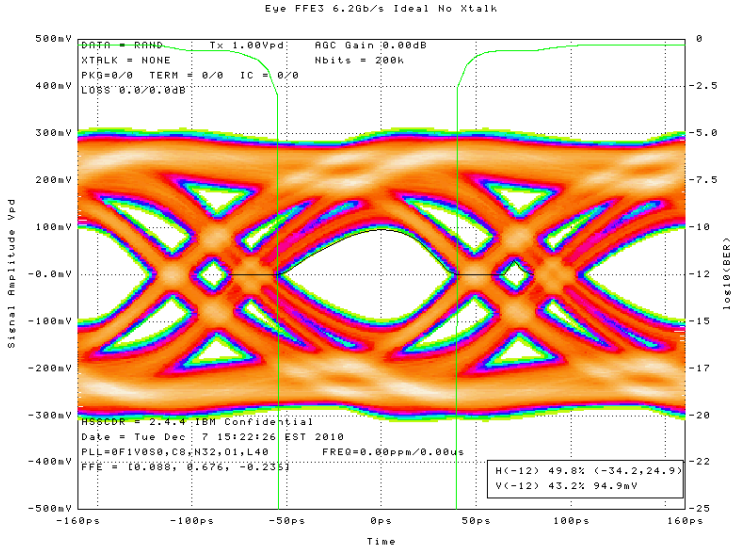
But not: TX FFE (since it is agnostic of actual jitter value)
→ TX FFE sub-optimal, should be replaced with (1)-(3) if possible

Jitter Amplification: Comparison TX FFE vs. RX FFE





TX-FFE



RX-FFE

Courtesy Troy Beukema

- 25% duty cycle variation applied = high frequency TX jitter at $f_b/2$
- Same equalizer coefficients for TX-FFE and RX-FFE

→RX-FFE suffers much less from TX jitter amplification than TX-FFE

→ Should make use of this fact in future standard definitions

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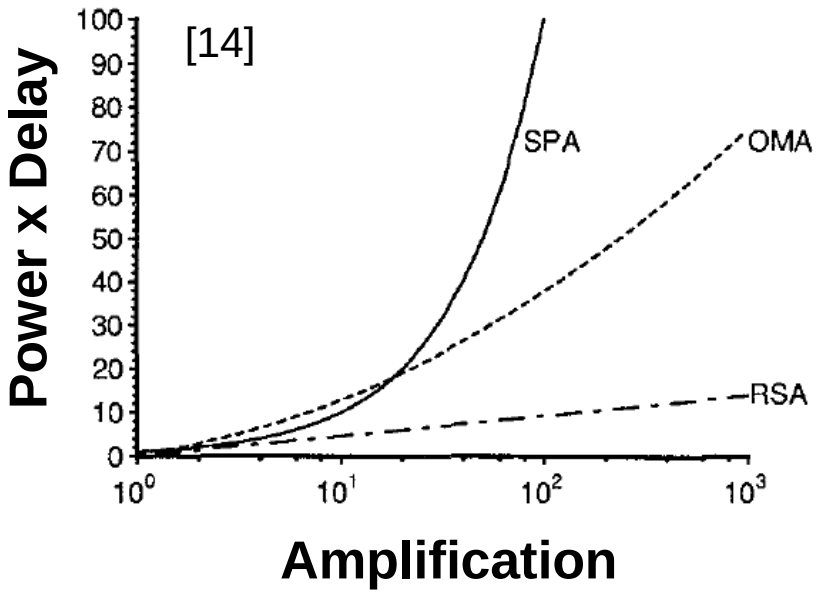
Power optimal Amplification



SPA = Single-Pole Amp

OMA = Optimized Multi-pole

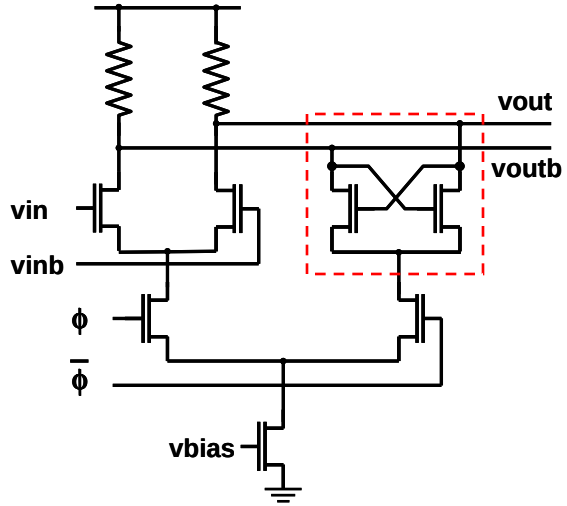
RSA = Regenerative Amp

- Energy/bit = Power * Delay

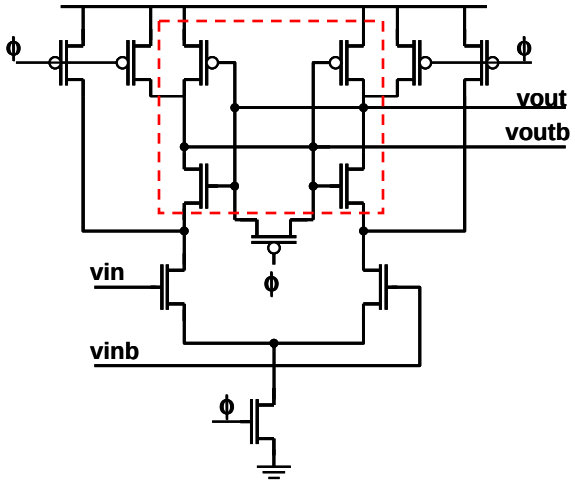
- Regenerative amplification most power efficient

J. Wu and B. Wooley, "A 100-MHz Pipelined CMOS Comparator," JSSC 1988.

CML vs. StrongARM (=DCVS) comparator latch



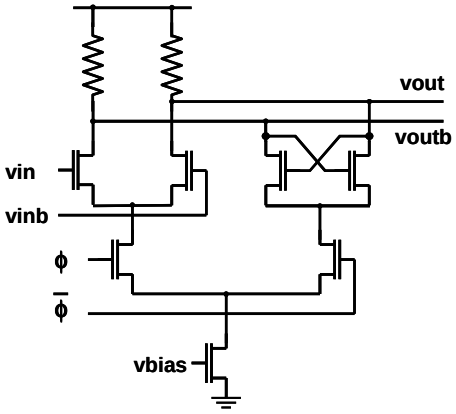
$$\tau_i = \frac{C_n}{gm_n - gds_n - 1/R} \cong \frac{2C_n}{0.9gm_n}$$



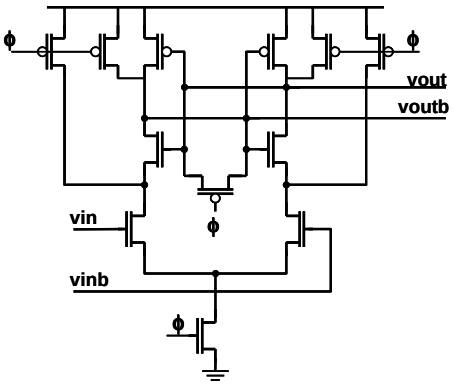
$$\tau_i = \frac{C_n + C_p}{gm_n + gm_p - gds_n - gds_p} \cong \frac{1.25C_n}{0.9gm_n}$$

- For V_{dd}=1V transistors are in similar operating point (V_{gs}=V_{ds}=0.5V)
- CML latch achieves smallest τ_i when $R=2/gm_n$
- StrongARM latch intrinsically faster
- P/N ratio was >2, now approaching 1 due to strain engineering

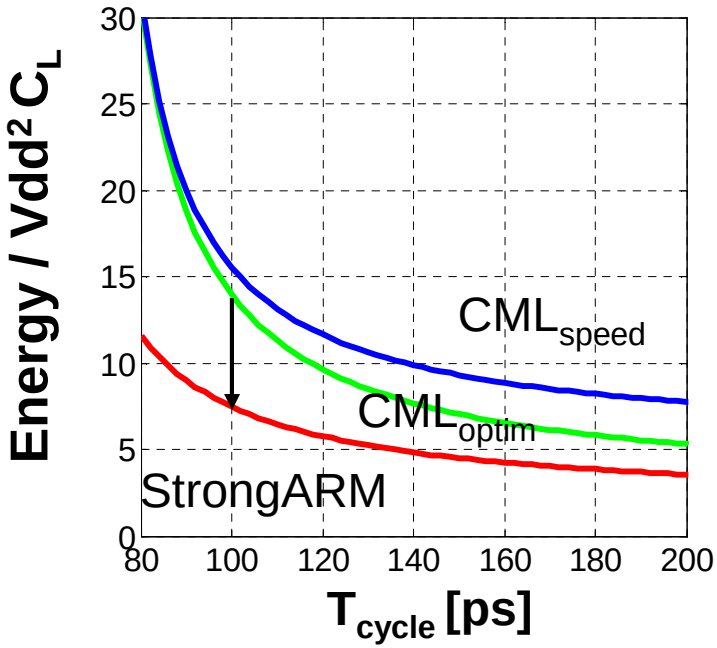
CML vs. StrongARM Latch Energy Consumption



CML-latch



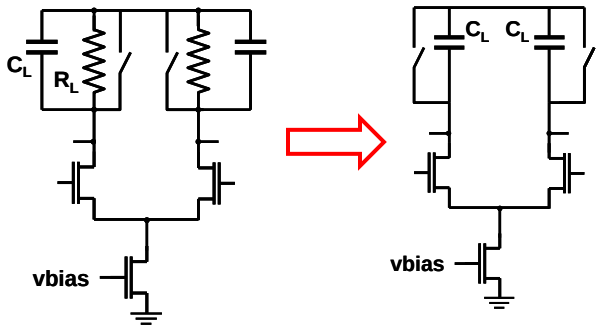
StrongARM-latch



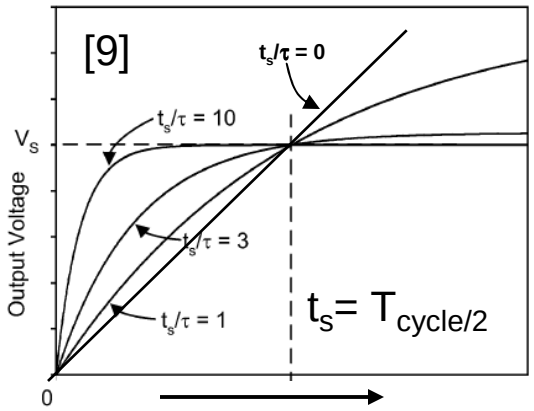
- CML latch optimized for speed or power
- Comparison for given T_{cycle} and amplification A = exp(5)

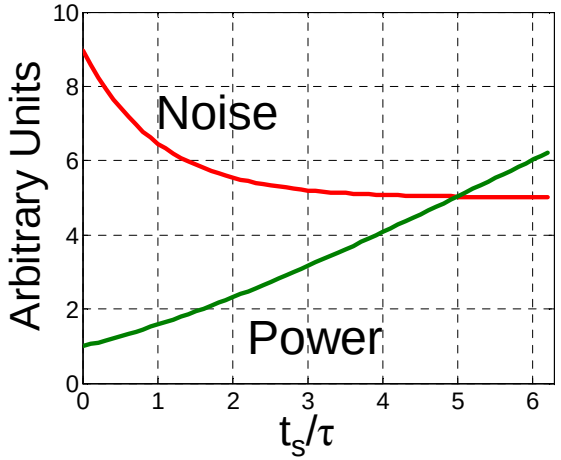
- **StrongARM latch ≈2x as power efficient at T_{cycle}=100ps**

Incomplete Settling → Integrating buffer



$\tau = R_L C_L$ $R_L \rightarrow \infty$, $t_s/\tau \rightarrow 0$





- First, introduce sampling & reset in data path
- For given C_L
  - $\tau = R_L C_L$ is varied by varying load resistance R_L
  - Power and noise are function of normalized settling time t_s/τ
  - Power can be reduced significantly for $R_L \rightarrow \infty$, ➔ integrator)
- But: Noise rises significantly when $t_s/\tau < 1.5$

➔ Can drive **higher load** at **same noise** with **lower power**

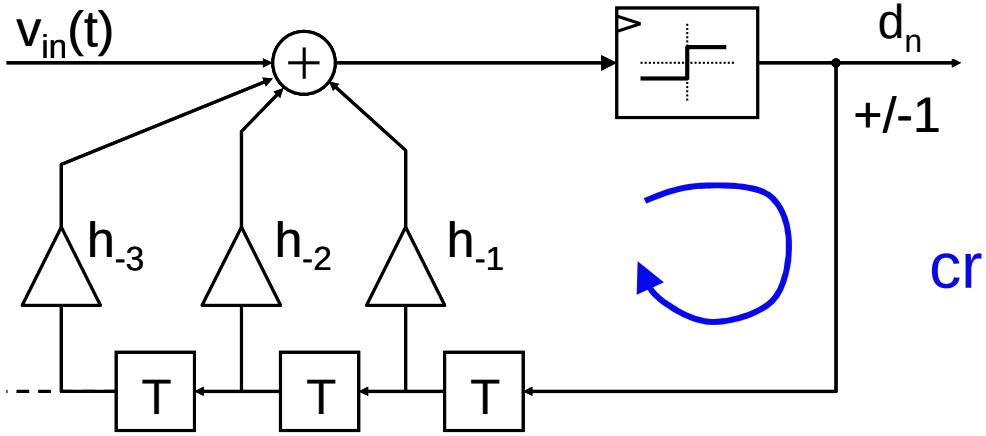
E. Iroaga and B. Murmann, "A 12-Bit 75-MS/s Pipelined ADC Using Incomplete Settling", JSSC 2007.

Low-Power Decision Feedback Equalizer (DFE)

- **DFE principle of operation**
  - **Direct DFE**
- **Low-power DFE**
  - **Speculative DFE**
  - **Integrating DFE**
  - **Switched-cap feedback**
- **Low-power DFE at high-speed (28 Gbps)**
  - **Integrating DFE with fast switched-cap path and 3-tap speculation**

Principle of DFE

Direct DFE



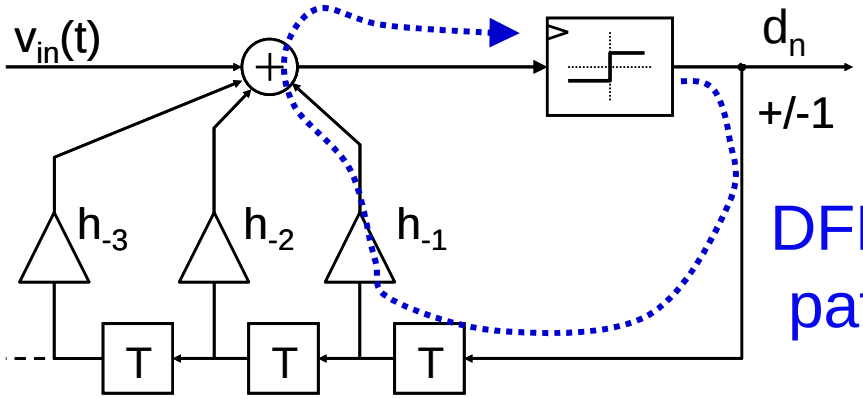
critical path
t=1UI

$$V_{int}=AV_{in}+d_{n-4}*h_4+\ldots+d_{n-15}*h_{15}$$

- **Fundamental problem**
  - **Have to close the to timing loop in the DFE in 1 UI**
- **Low-power solutions : Relax timing → lower supply voltage**
  - **Use speculative DFE (see next slide)**
  - **Improve speed of DFE feedback → switched-cap feedback**

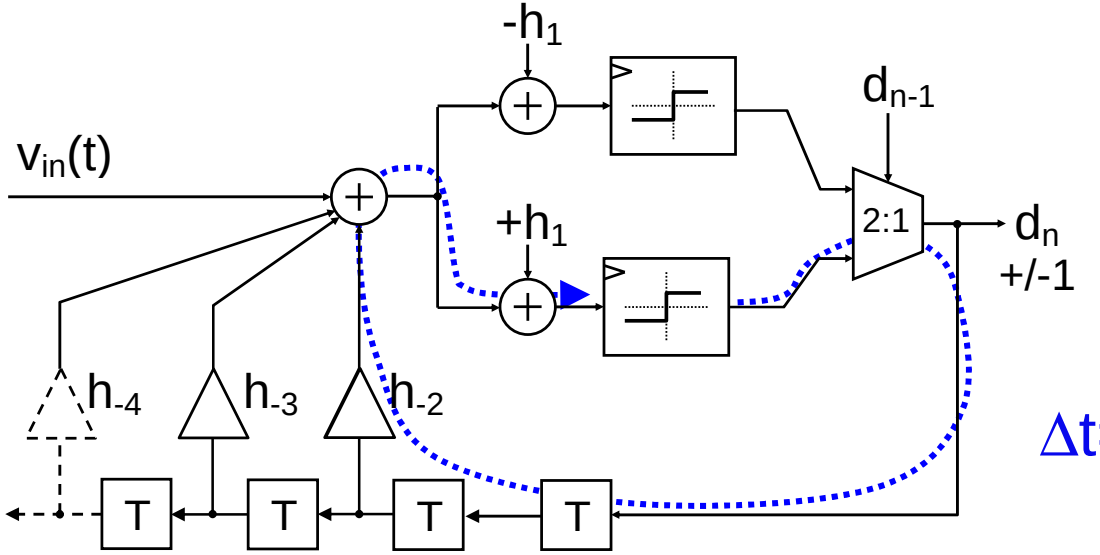
Speculation in DFE

Direct DFE



DFE feedback path Δt=1UI

DFE with **one** speculative tap



Δt=2UI

➔ **Timing relaxed by 1UI - t_{MUX}**

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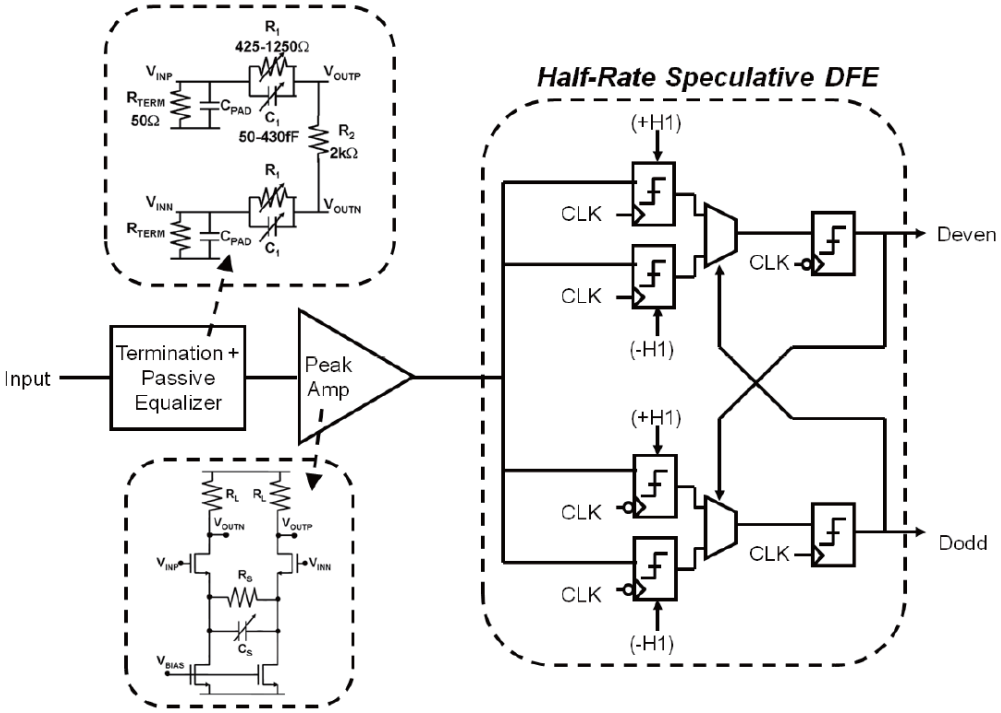
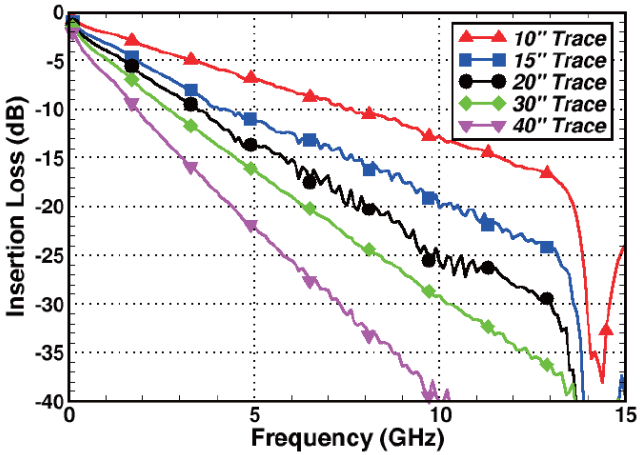
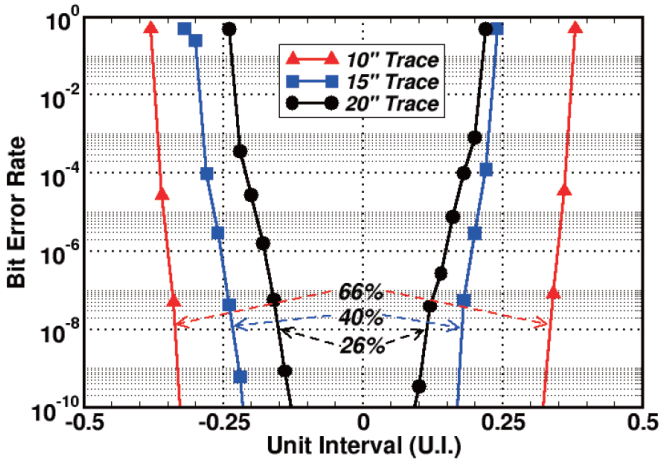
CTLE + 1-tap speculative DFE results in power-efficient solution



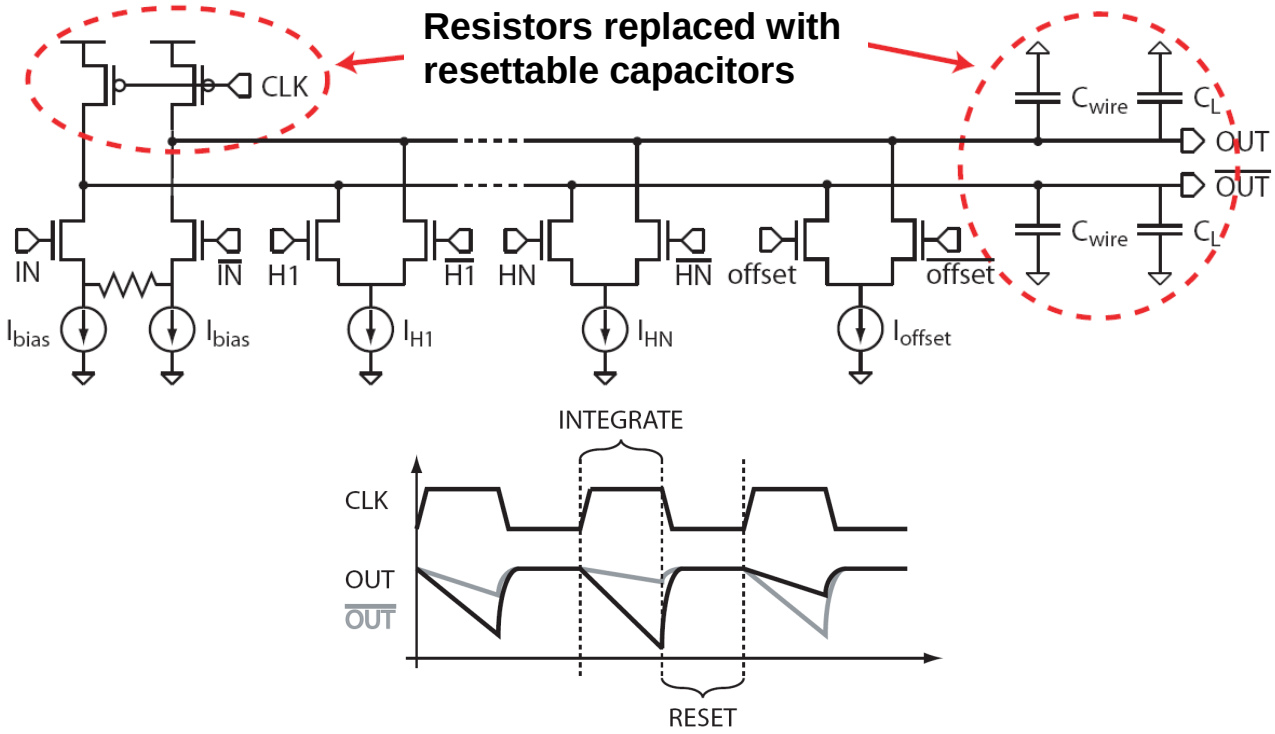




- Good solution for smooth channels
- Avoids analog DFE summation
- **Power = 0.7pJ/bit @ 20Gb/s**

J. Proesel et al., VLSI 2011

Summation node: Current-Integrating DFE



- **Integrating buffer** instead of **resistively loaded buffer**

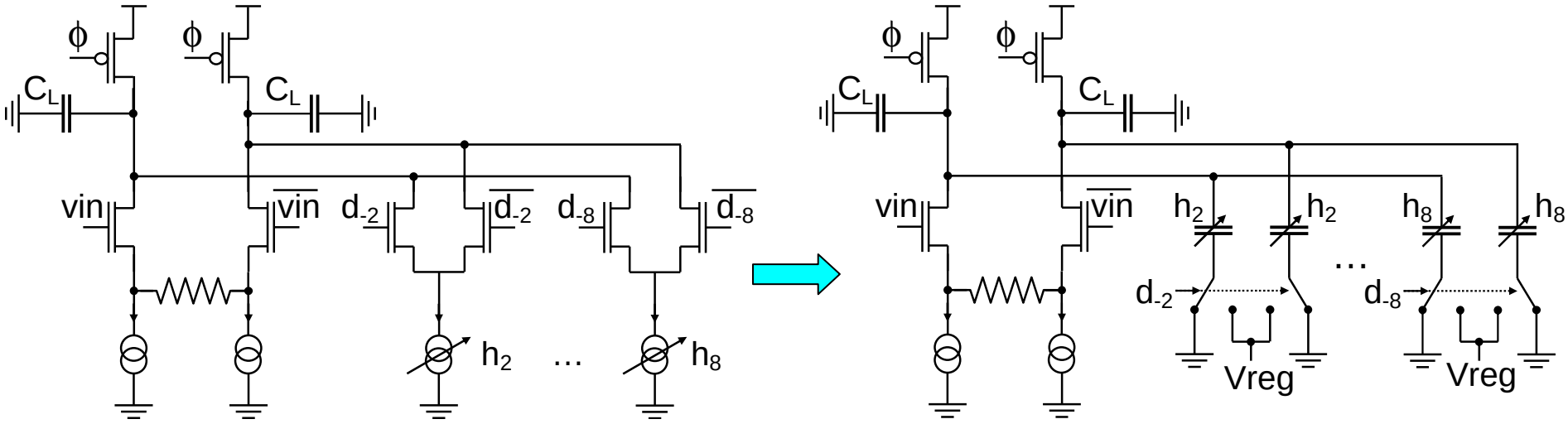
  → Lower power

- 1.4 pJ/bit for 2 taps, 90nm CMOS

M. Park, et al., "A 7 Gb/s 9.3 mW 2-Tap Current Integrating DFE Receiver", ISSCC 2007.

Integrating DFE with I-feedback or switched-cap feedback

$$V_{int}=AV_{in}+d_{n-4}*h_4+\ldots+d_{n-15}*h_{15}$$



I- feedback
[Parks and Bulzacchelli, ISSCC 2007]

Switched-cap feedback
SC-DFE (VLSI 2011)

- I-feedback is replaced with charge feedback → SC-DFE
- Enables **faster feedback loop** (see next slide)

T. Toifl et al. “A 2.6mW/Gbps 12.5Gbps RX with 8-tap Switched-Cap DFE in 32nm CMOS”, VLSI 2012

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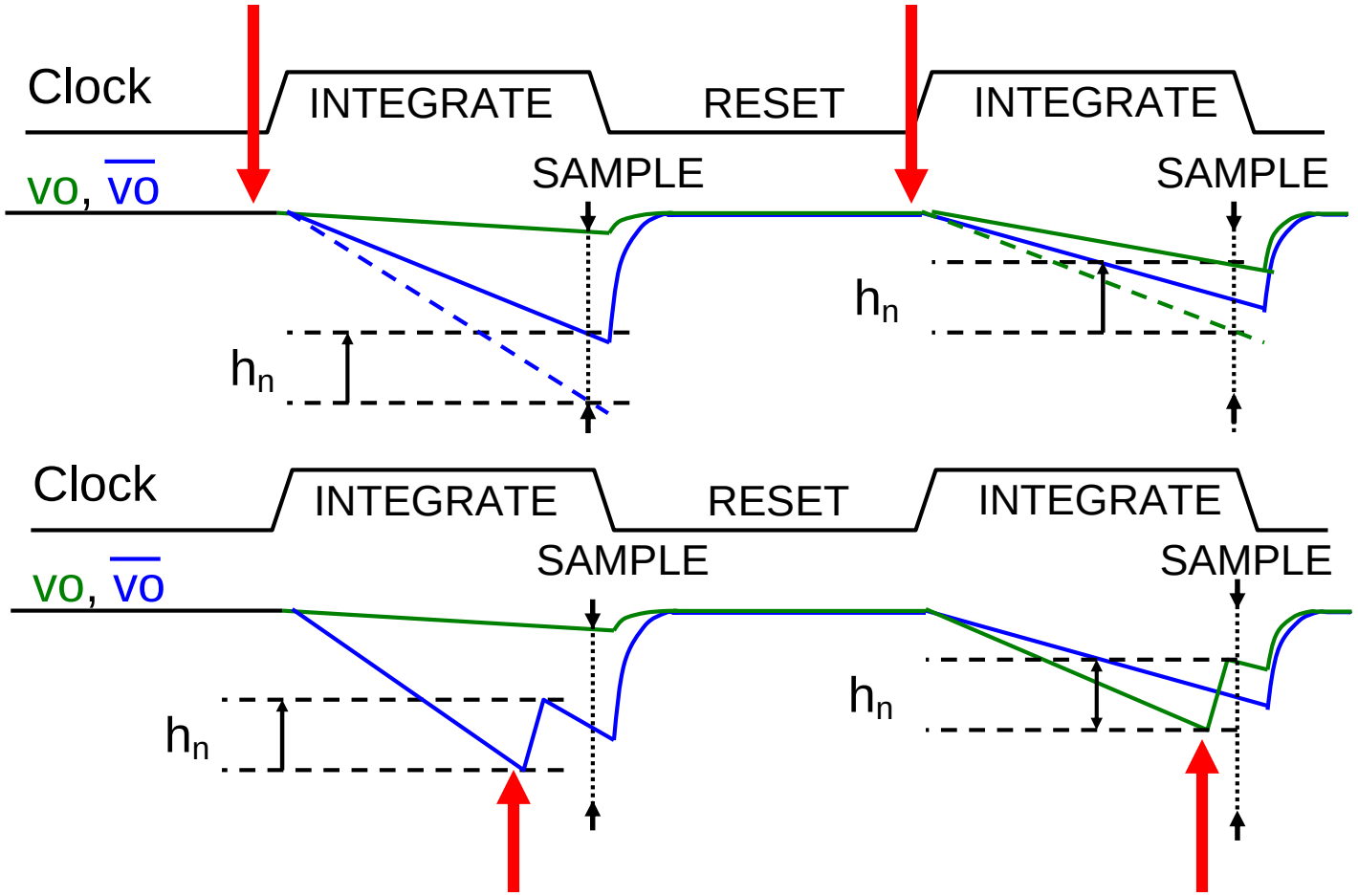
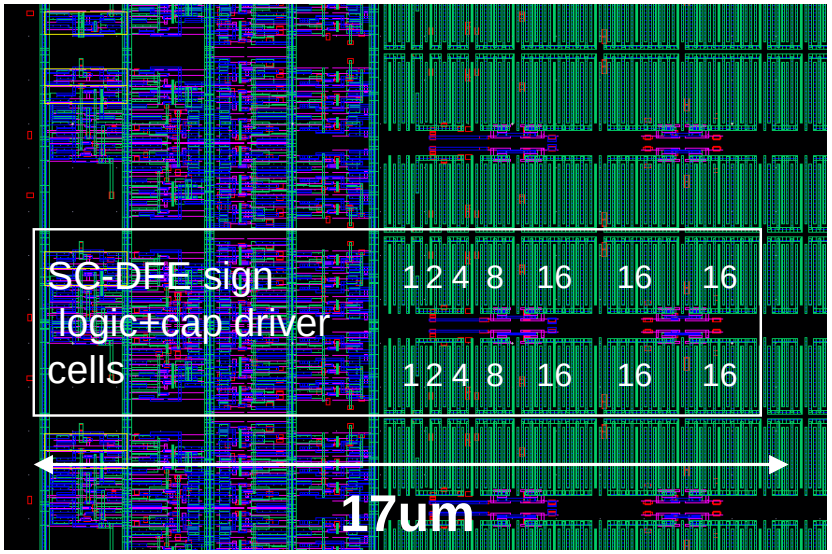
DFE: Current feedback vs. switched-cap feedback

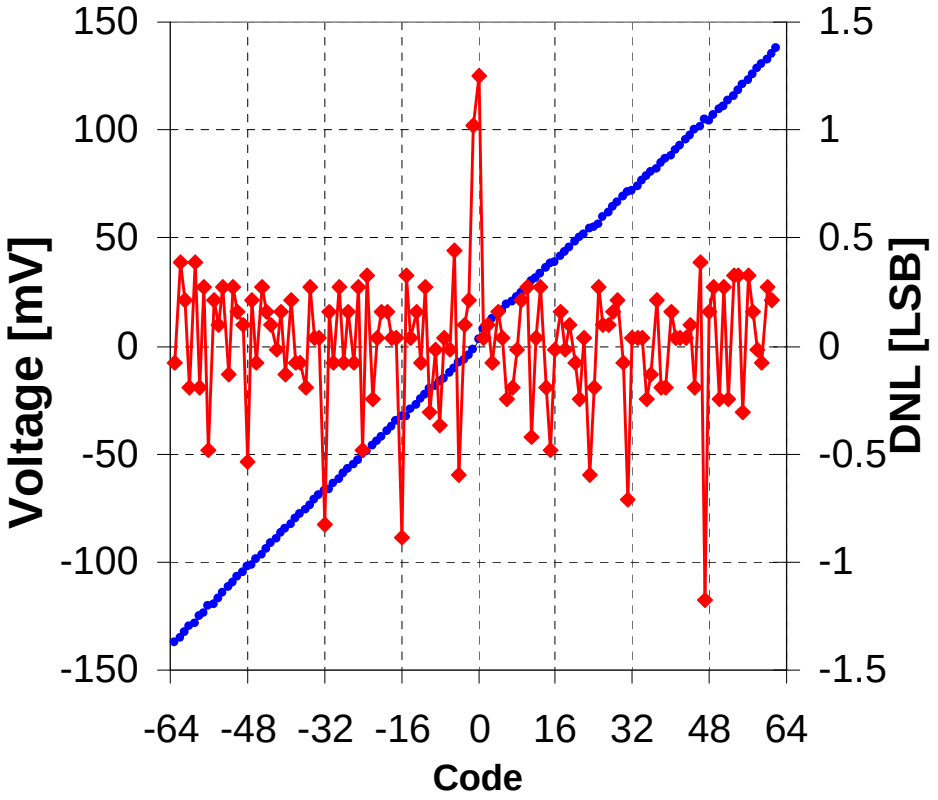
Current feedback: previous symbol decision must arrive **before** integration



SC-feedback: previous symbol decision may arrive **later** → **more margin**

SC-DFE DAC Implementation and Measurement





- ±63 steps (6bit+sign) for taps 2-8
- 1 LSB = 250aF
- Excellent linearity
- Very Small area (no I-DAC needed)

- Caps made of min finger M1+M2
- Size of entire SC-DFE tap < 70um^2 in 32nm (including DAC)

Low-power DFE at 28 Gbit/s

- **28 Gbps : 1UI = 35ps**
  - **Half-rate** receiver reaches limit
    - Hard to achieve required amplification in integrator
    - 14GHz CMOS clocking difficult
      - Duty cycle hard to control, need small FO
      - Electromigration requires to add lots of metal in the layout

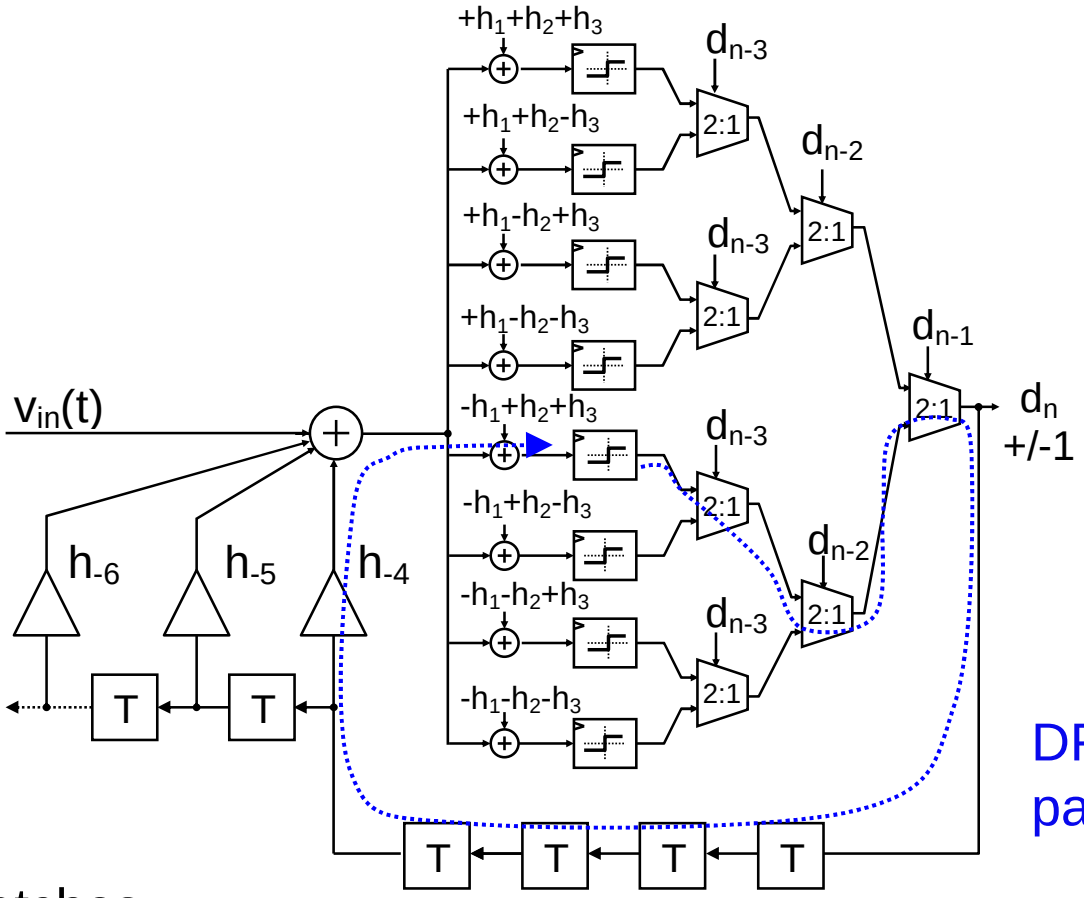
  → **Quarter-rate** receiver more power-efficient

  - **Single-tap** speculative DFE **too slow**
    - Feedback time only t_{fb}=70ps

  → **Three-tap speculation** relaxes timing (t_{fb}=210ps)

  → **Can reduce supply voltage and use higher fan-out**

3 Tap Speculation



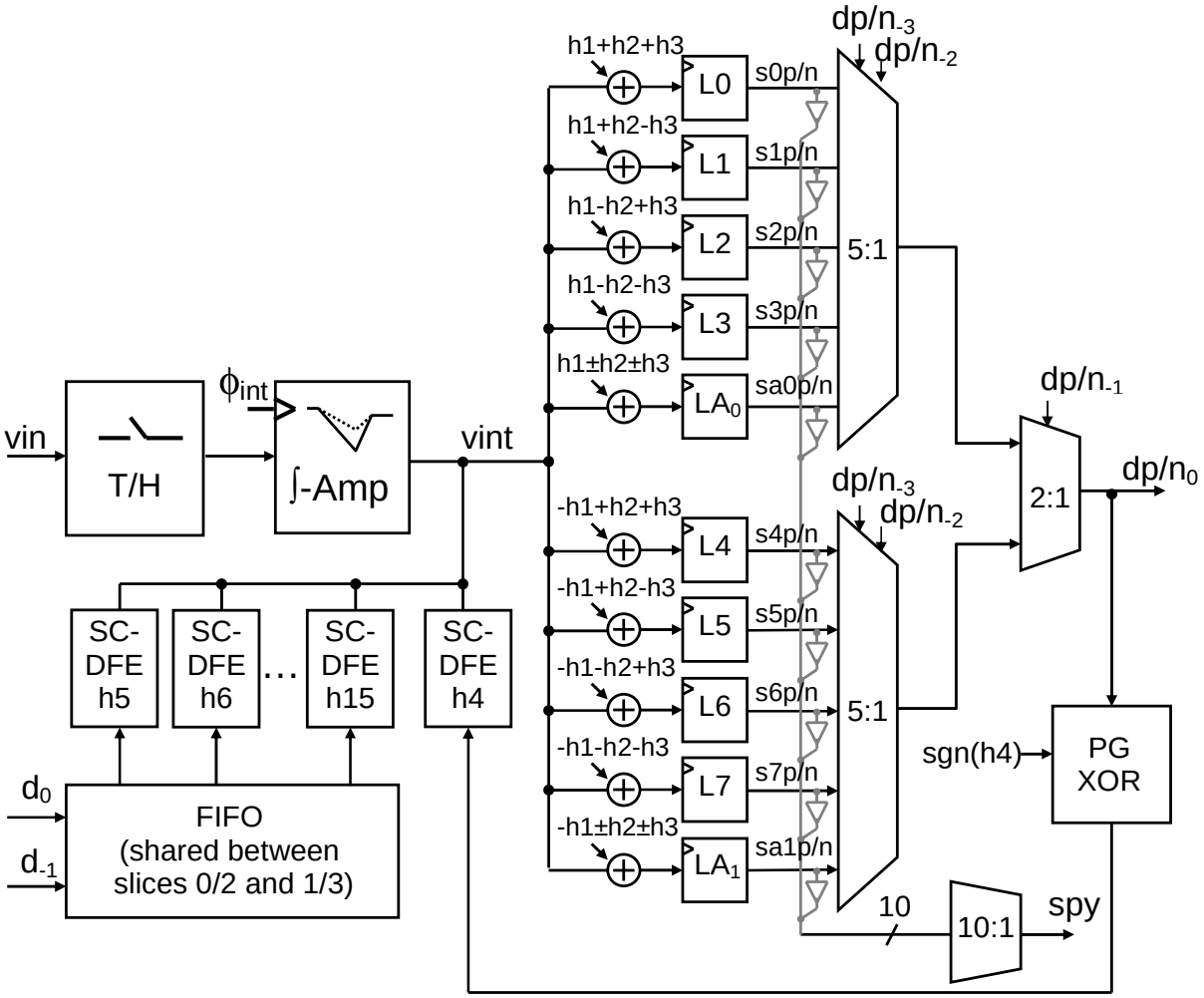
DFE feedback path $\Delta t=4UI$

- Now 8 latches
- Power ~ 150fJ/bit per latch → moderate penalty
- Critical path now 4UIs

➔ Timing relaxed by 3UI - $3t_{MUX}$

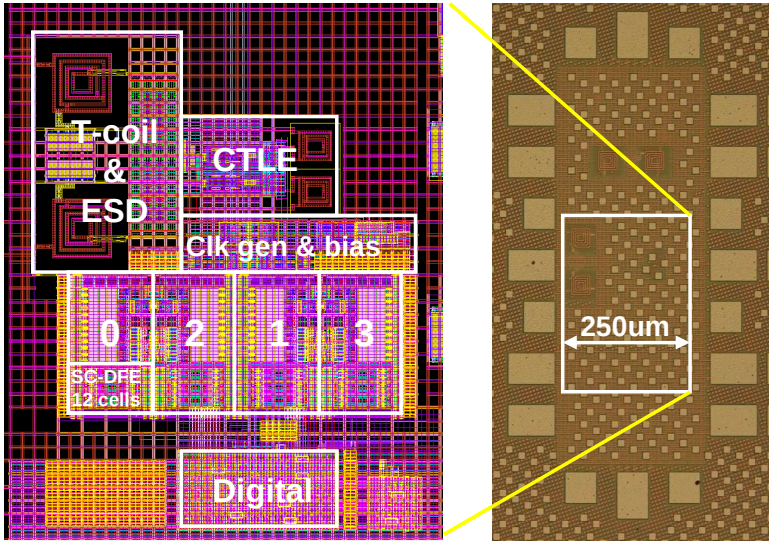
32

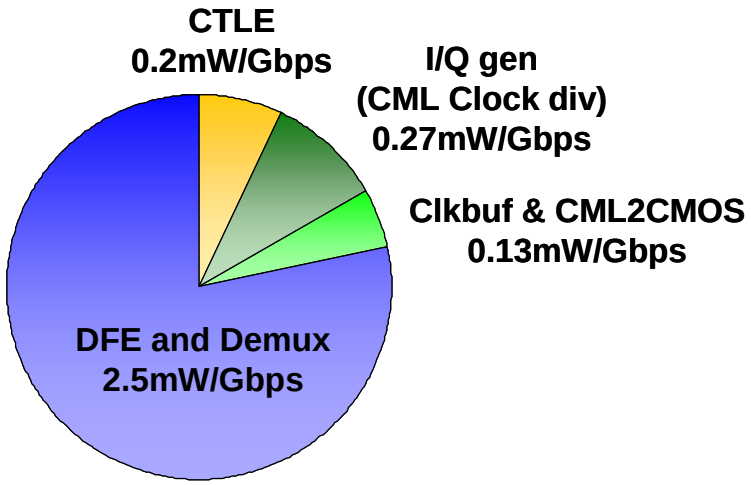
DFE + Demux slice (1 slice of 4 total)



Actually **10** comparator latches per slice : 8 active + 2 used for calibration

Layout and power breakout @ 30Gb/s



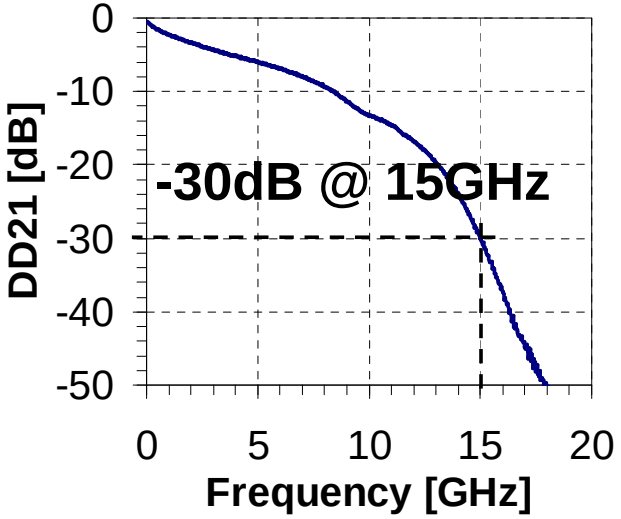


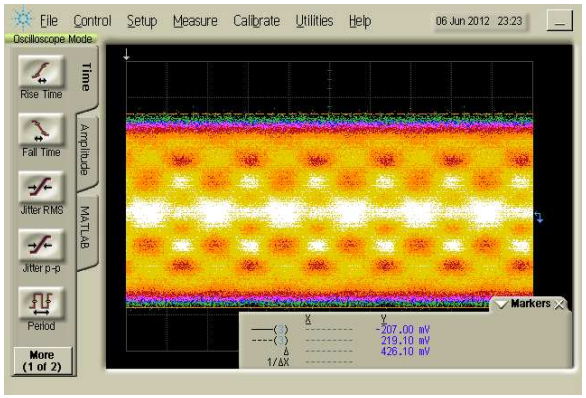
Total: 92mW = 3.1mW/Gbps

- **Core DFE size = 200x90µm**
- **Need to calibrate 40 comparator offsets and 48 DFE taps**

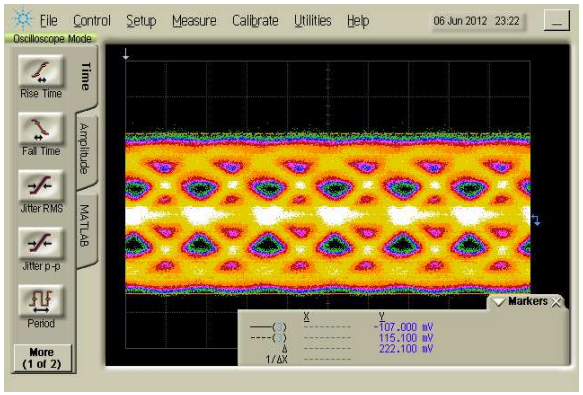
T. Toifl, et al., "A 3.1mW/Gbps 30Gbps Quarter-Rate Triple-Speculation 15-tap SC-DFE RX Data Path in 32nm CMOS", VLSI 2012.

30Gb/s

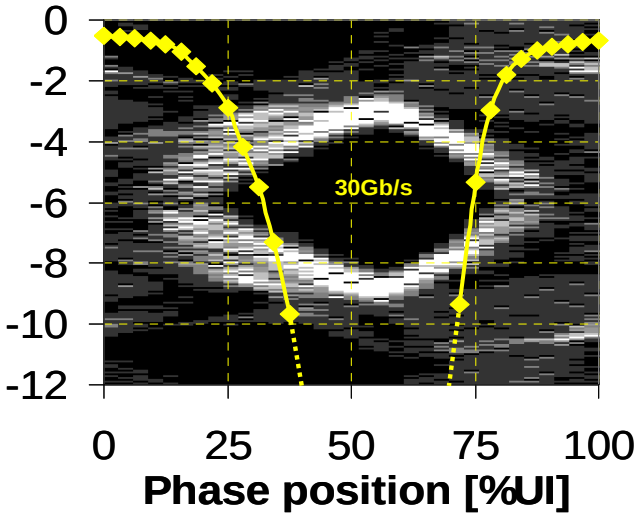




PRBS 31, No TX FFE



TX FFE = [0 67 -29]

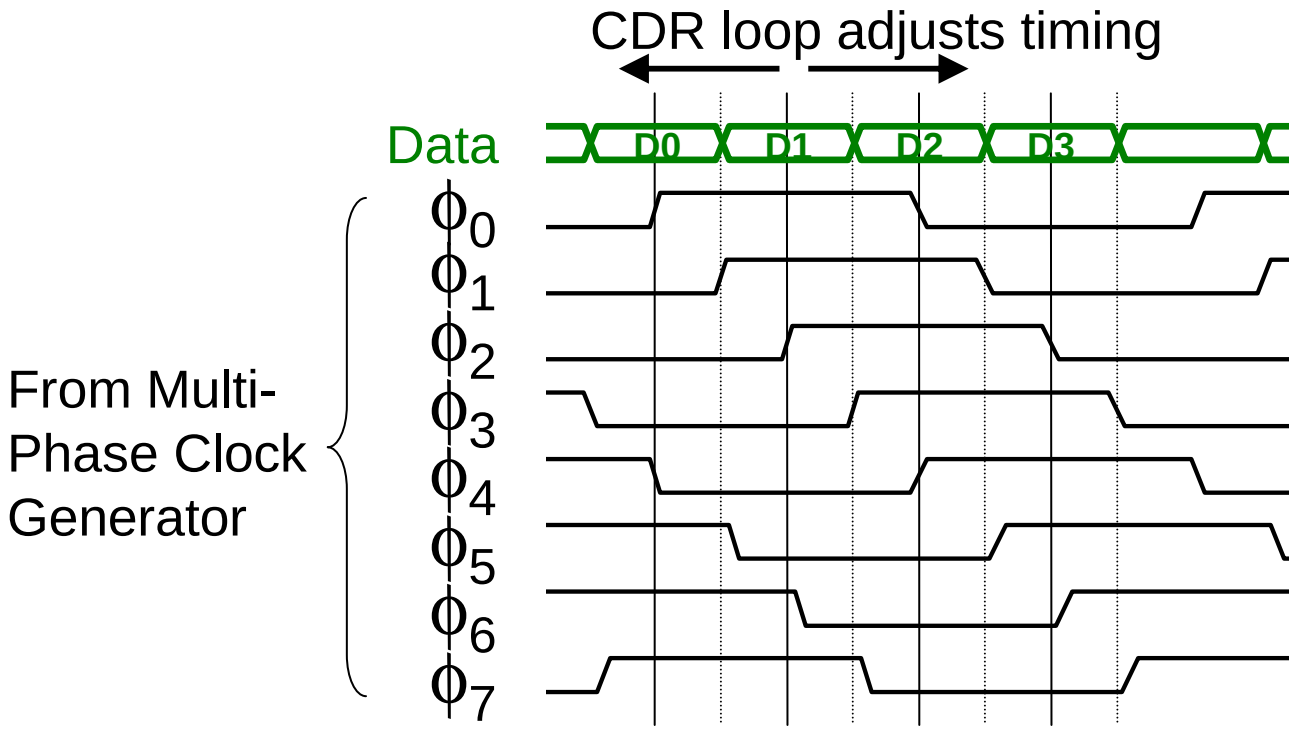


Power =92mW @ V_{DD}=1.15V = 3.1pJ/bit

Low-power RX clock generation

- **Clock generation for quarter-rate CDR system**
  - **Phase-programmable PLL (P-PLL)**
  - **Design example:**
    - 40Gb/s RX using P-PLL

Quarter-rate Clock and Data Recovery



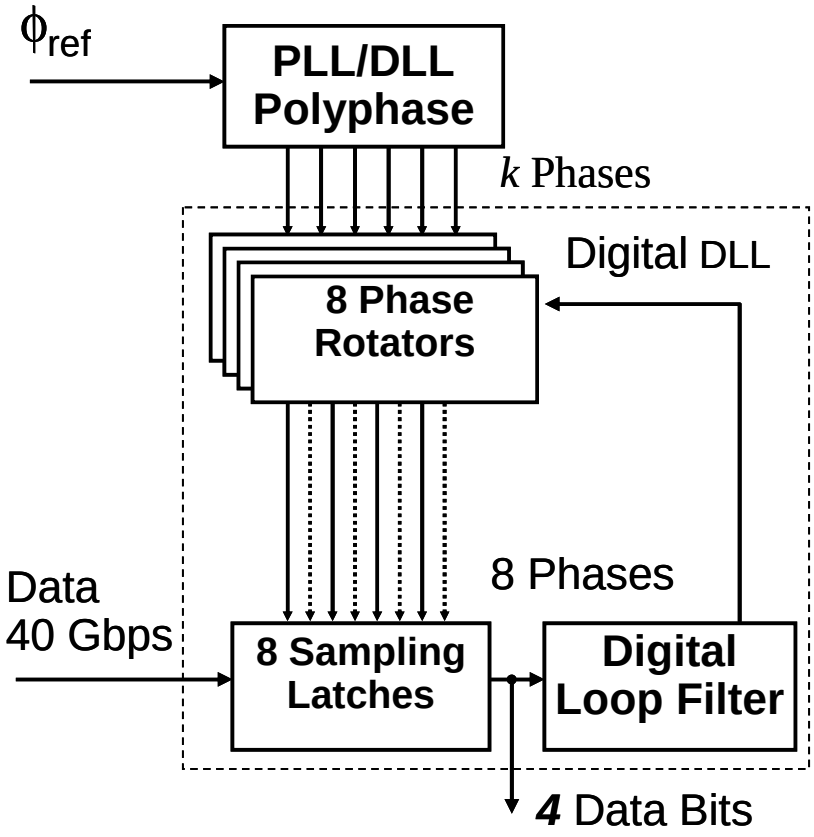
4 Received bits per clock cycle

2 Sample bits/symbol (data, edge)

→ Need 4x2 clock phases

→ Need to shift 8 clocks simultaneously

Quarter-rate Dual-loop architecture

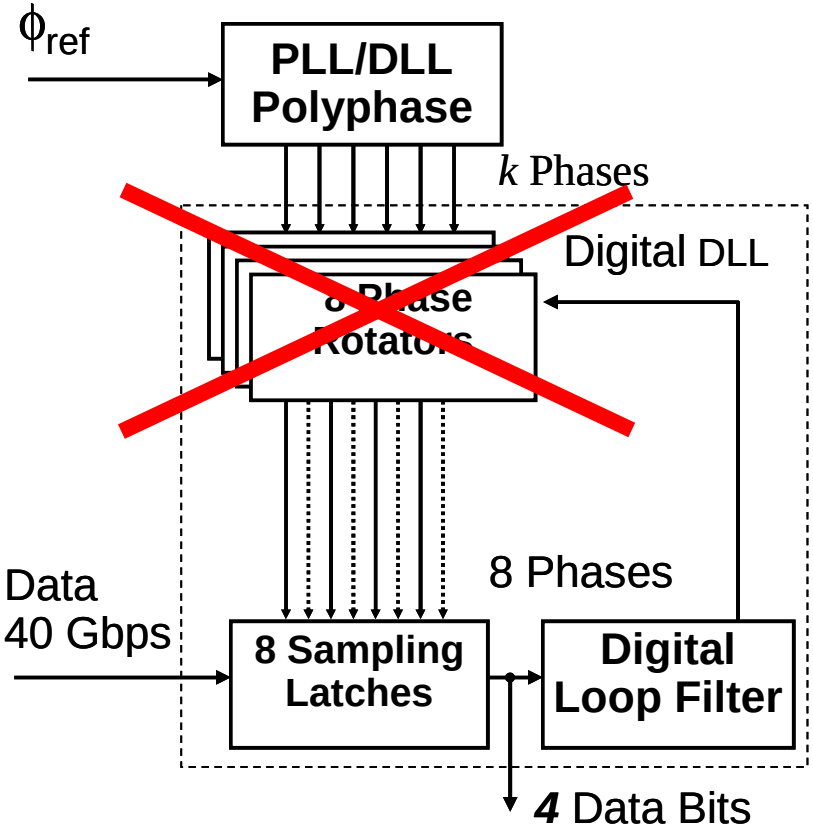


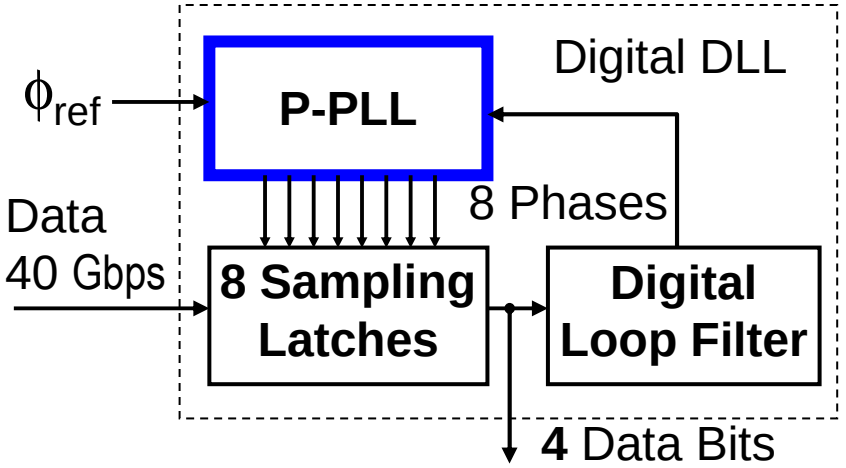
Previous solution

Phase rotators:

- Area
- Power
- Mismatch
- Need at least 2 ref phases

Quarter-rate Dual-loop architecture

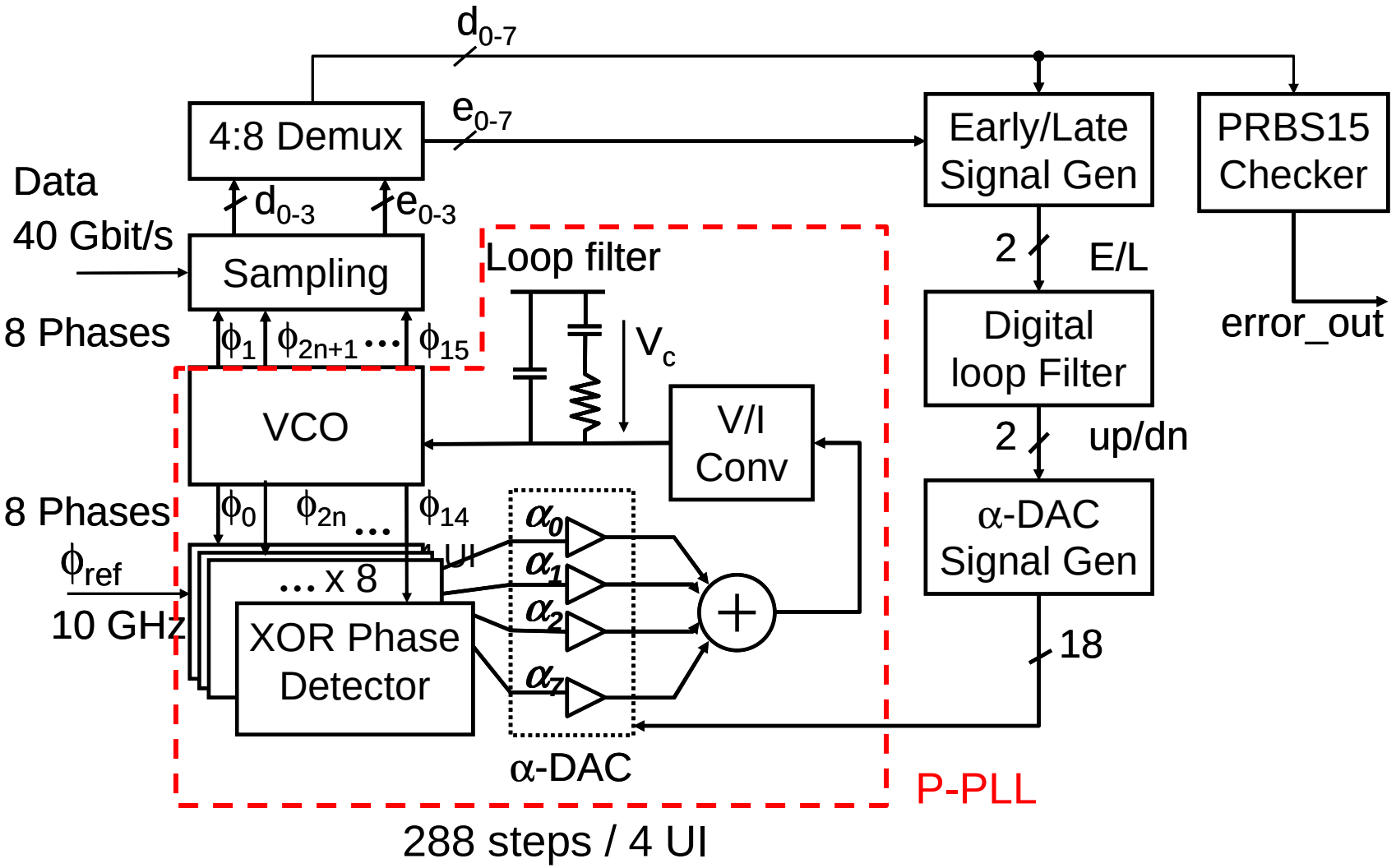




⇒ **Phase-Programmable PLL (P-PLL)**

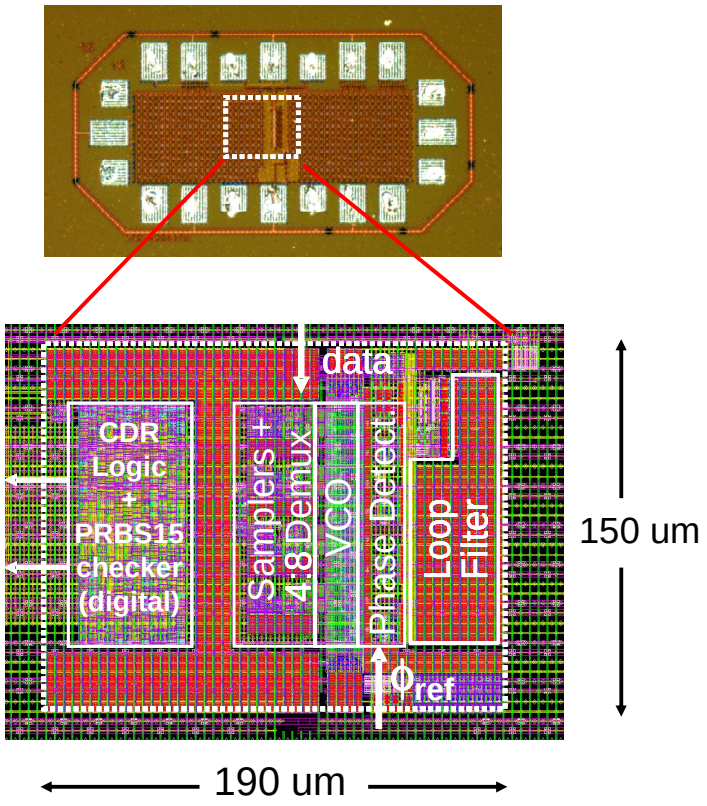
- Phases can be programmed by digital value → Enables digital CDR loop
- Provides tight lock to high-reference frequency → low jitter

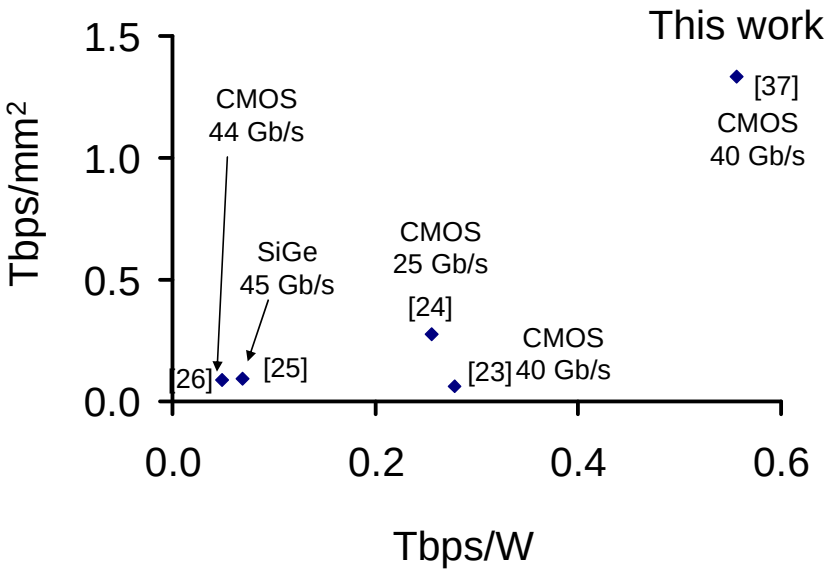
40 Gb/s CDR Architecture using P-PLL



[37] T. Toifl et al., "A 72 mW 0.03 mm^2 inductorless 40 Gb/s CDR in 65 nm SOI CMOS," ISSCC 2007.

Chip Photograph and Layout of 40Gb/s RX





- Power : 1.8pJ/bit @ 40 Gbps
- Area: <0.03mm² in 65nm CMOS, **no inductors uses**

Outline

- **Introduction**
  - High-Speed I/Os in the wireline link space
  - Equalization techniques
- **Low-power Transmitter**
  - SST vs. CML driver
  - Ultra-low power TX → Avoid TX-FFE
- **Low-power Receiver**
  - Power-optimal amplification
  - Incomplete Settling / Integrating Buffer
  - Low-power DFE Architecture
- **Digital approaches**
  - **ADC**
  - **DFE implementations**
  - **Analog vs. Digital**

ADC-based I/Os

- New standards emerging operating with PAM-4
  - IEEE 802.3bj (100Gb Ethernet over backplane)
    - PAM-4 mode for high channel loss (>40dB)

- Requirements for ADC
  - Rather low resolution (<5bits)
  - Low latency (for closing CDR loop)

  → Flash ADC

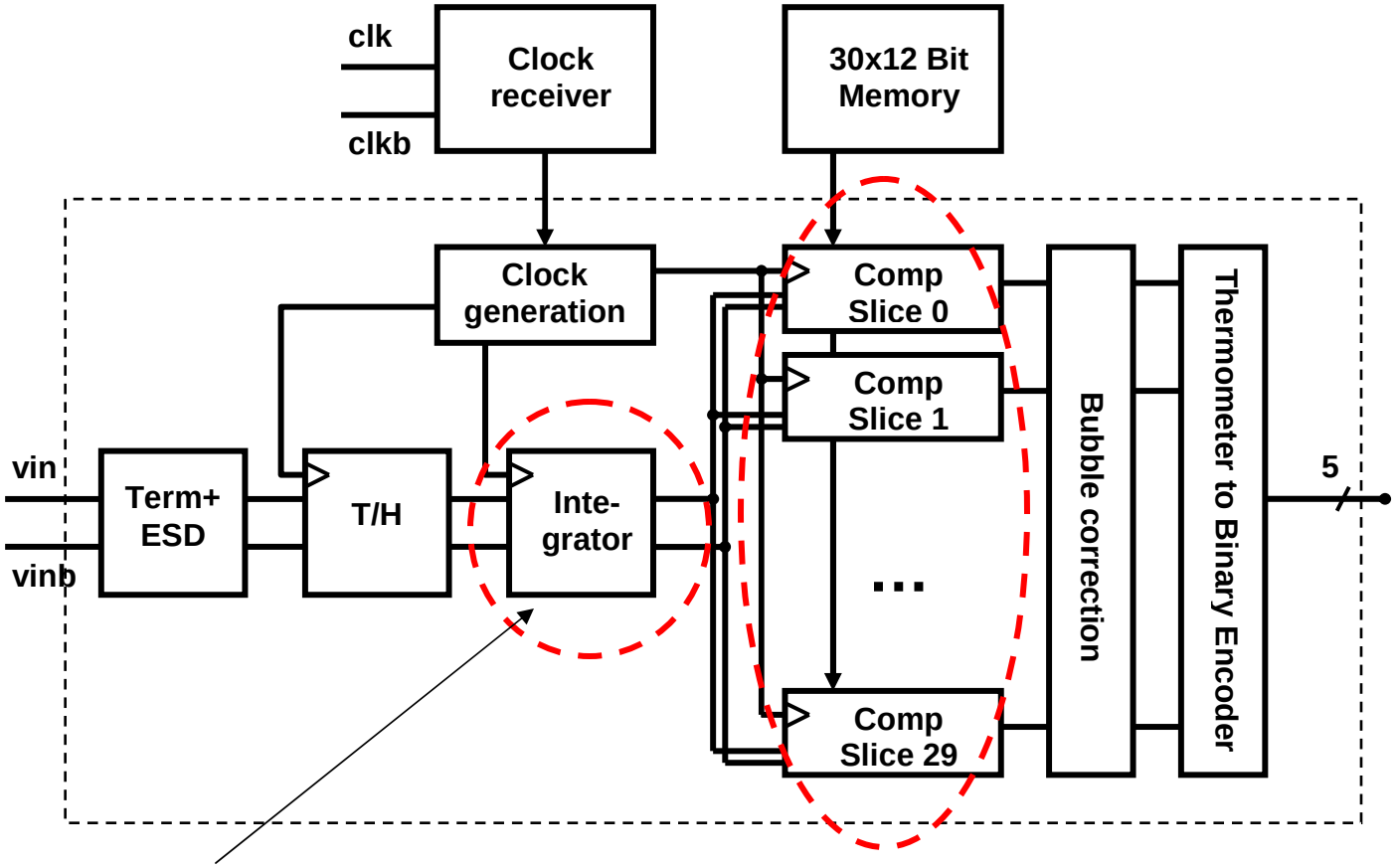
  - High conversion rates

  → Interleave Flash ADC

  → Low input capacitance required

Example: Low-power flash ADC with small input cap

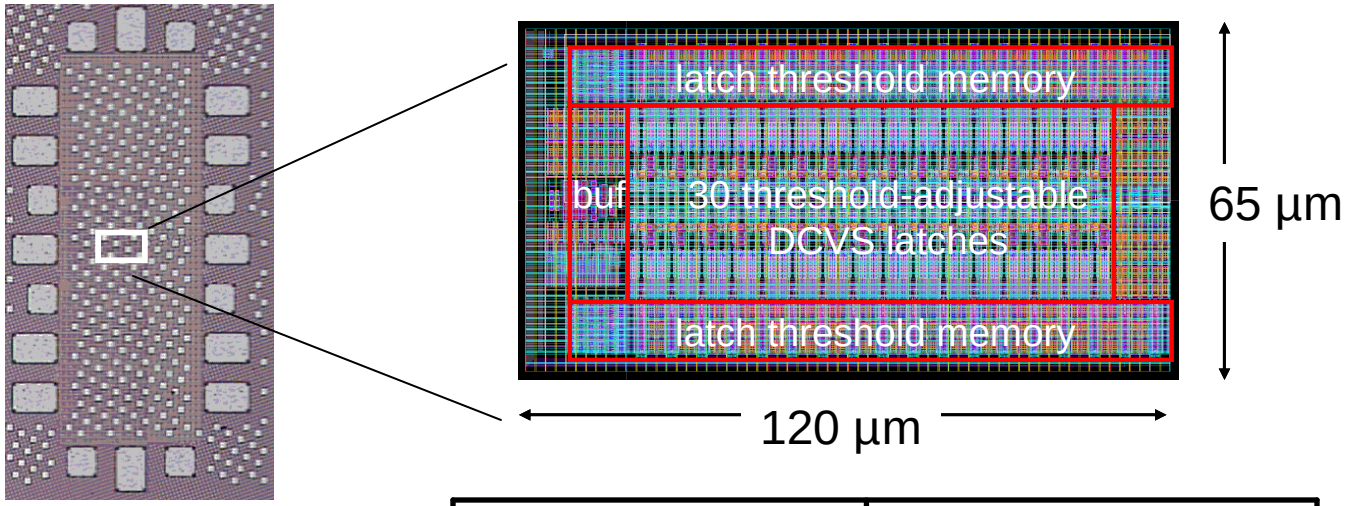
Low-power flash ADC with small input cap



- Integrating buffer drives big load with small input capacitance

- Comparator slice consists of offset-adjustable SenseAmp latch (no reference ladder required)

Low-power flash ADC results

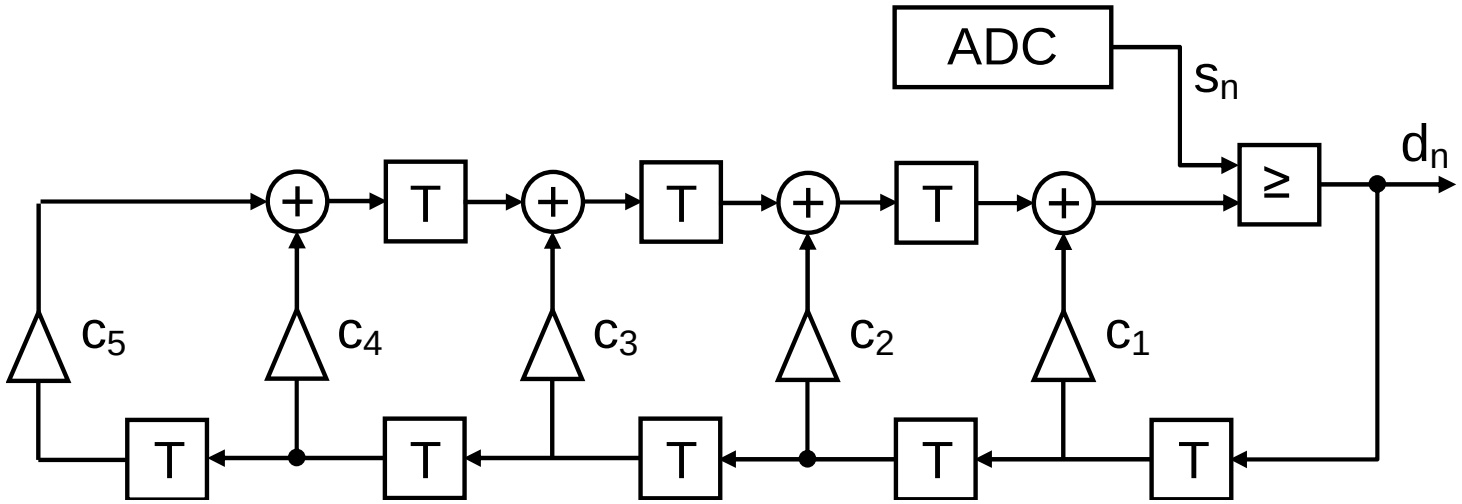


Technology	**32nm CMOS SOI**
Sampling frequency	**5GHz**
ENOB @ DC	**4.4**
ENOB @ fs/2	**4.1**
DNL, INL	**<0.3 LSB, <0.3 LSB**
Power consumption	**19mW @ 1V supply**
FOM	**230fJ/conversion step**
Input cap	**50fF**

→ ADC cell can be time-interleaved to achieve higher conversion rates

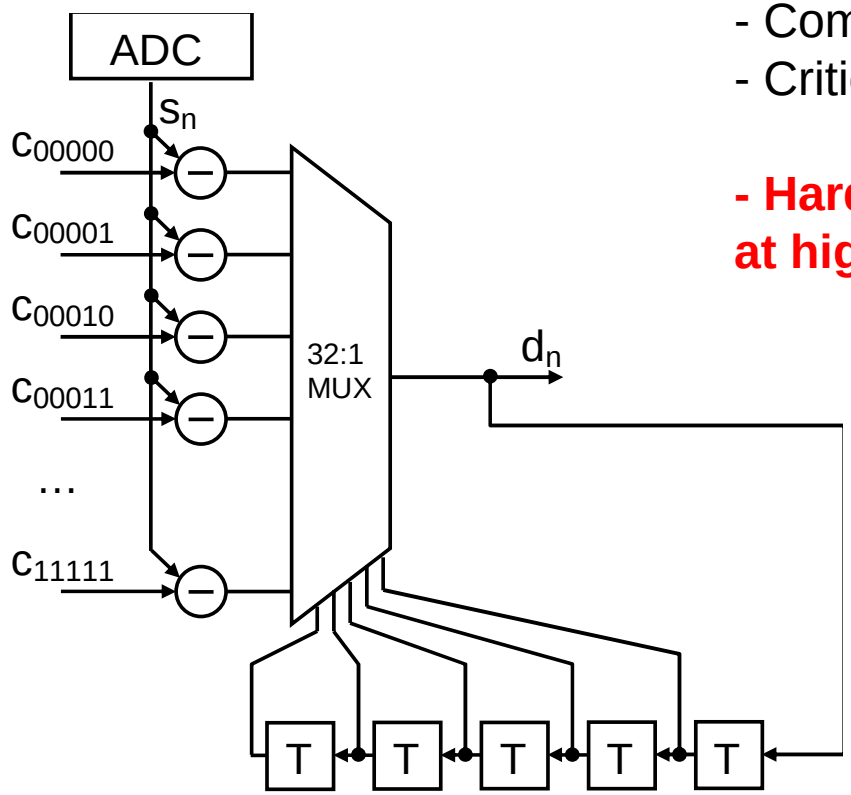
Digital DFE

- Relatively simple and low-power
  - **Case I : low speed (<5Gbit/s)**
    - DFE loop can be implemented by digital adder
    - Critical path is adder and comparator
    - Taps can also be combined in LUT



Digital DFE

- Relatively simple and low-power
  - **Case II : small number of DFE taps (n ≤ 5)**
    - Digital loop unrolling requires 2^n comparators



- Comparator power: <100uW/Gbps
- Critical path: 2:1 MUX

- Hard problem is long DFE (eg 15 taps) at high speed (eg 28Gb/s)

Analog vs. Digital: RX power comparison

- Power: **Optimized Analog RX** with 15-tap DFE
  - Clock path: 2mW/Gbps
  - Linear equalizer (CTLE): 1.5mW/Gbps
  - DFE: **3mW/Gbps** for 15-tap DFE @ 25Gb/s
  - **Total: 6.5 mW/Gbps**

- Power: **ADC based RX** with 15-tap digital DFE
  - Clock path: **1mW/Gbps** (no edge samples required with Mueller-Müller CDR)
  - Linear equalizer (CTLE): 1.5mW/Gbps
  - ADC: 4mW/Gbps
  - DSP: FFE: 3mW/Gbps + DFE: 3mW/Gbps
  - **Total: 12.5mW/Gbps**

→ADC power alone is ≥ DFE power

→ **Analog will stay lowest power solution for DFE equalization**

Why ? Analog well suited for DFE: **fast summation with moderate accuracy**

BUT: gap will shrink as technology scales

Summary

- **Low-power TX techniques**
  - SST drivers: low-power, multi-standard
  - Avoid TX-FFE: Low power, less jitter amplification
- **Low-power RX Techniques**
  - Regenerative amplification, StrongARM (DCVS) latch
  - Integrating DFE using switched-cap feedback
  - P-PLL phase generation
- **Digital (ADC-based) I/O approaches**
  - ADC : Flash ADC <4mW/Gbps
  - Analog is lower power solution for long DFE at high speeds
  - High-speed I/Os will follow route of Gb Ethernet over UTP

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IBM

- Christian Menolfi
- Peter Buchmann
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Miromico

- Robert Reutemann
- Michael Ruegg
- Daniele Gardellini
- Andrea Prati
- Giovanni Cervelli

Thank you for your attention!

Additional Slides

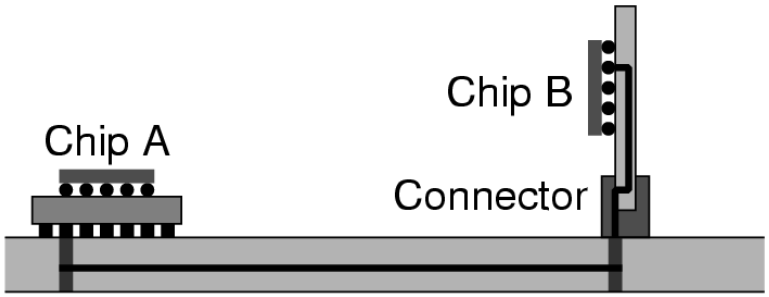
Summary of Equalization Techniques

- **Feed-forward Equalization (FFE)**
  - FIR filter, usually implemented at TX side
- **Continuous-Time Linear Equalizers (CTLE)**
  - Increase high-frequency gain and/or decrease low-frequency gain to compensate for low-pass channel characteristics.
- **Decision Feedback Equalization (DFE)**
  - Feed back previous bit decisions to cancel postcursor ISI caused by those bits.

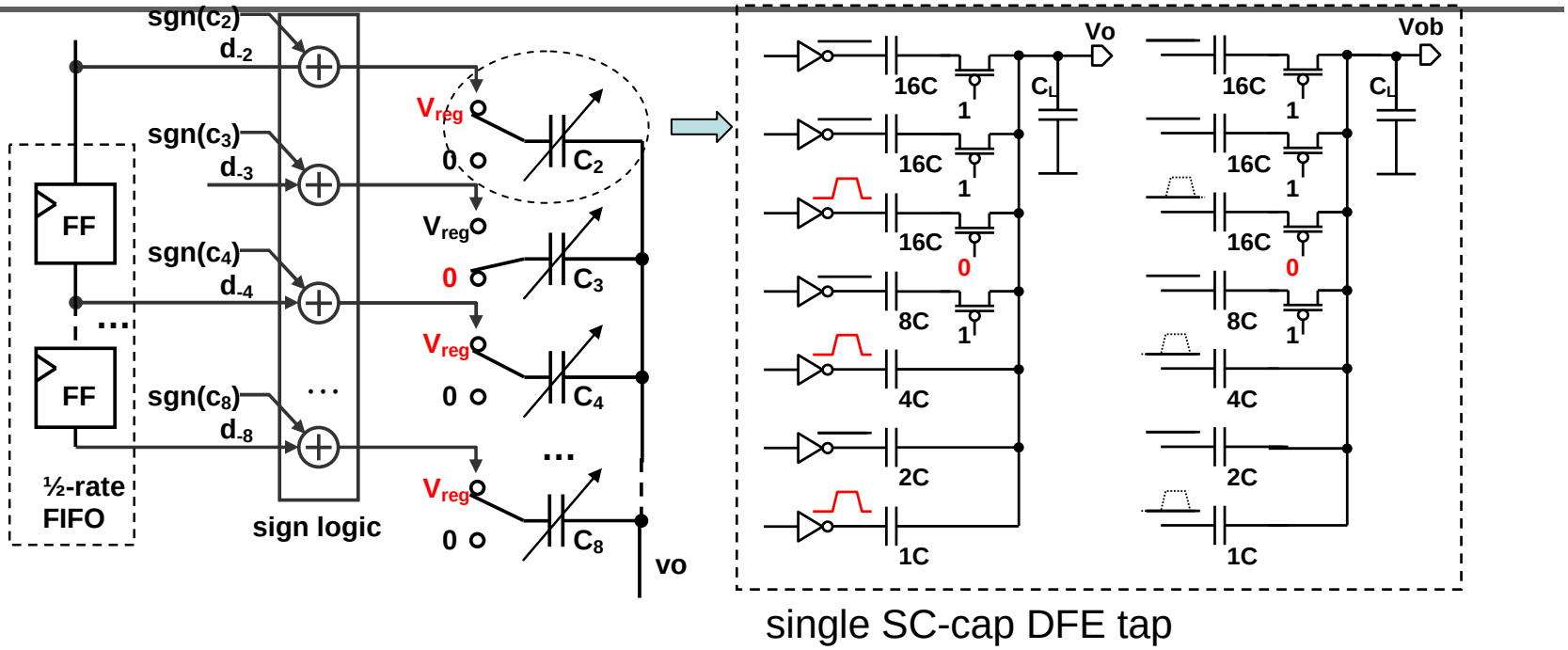
Source-synchronous Links Application Area

Important parameters:

- throughput (Gb/s per pin)
- power (mW per Gb/s or equivalently pJ per bit)
- limited die area (μm^2 per Gb/s, fit beneath C4 balls)
- Latency (memory links, SMP links)



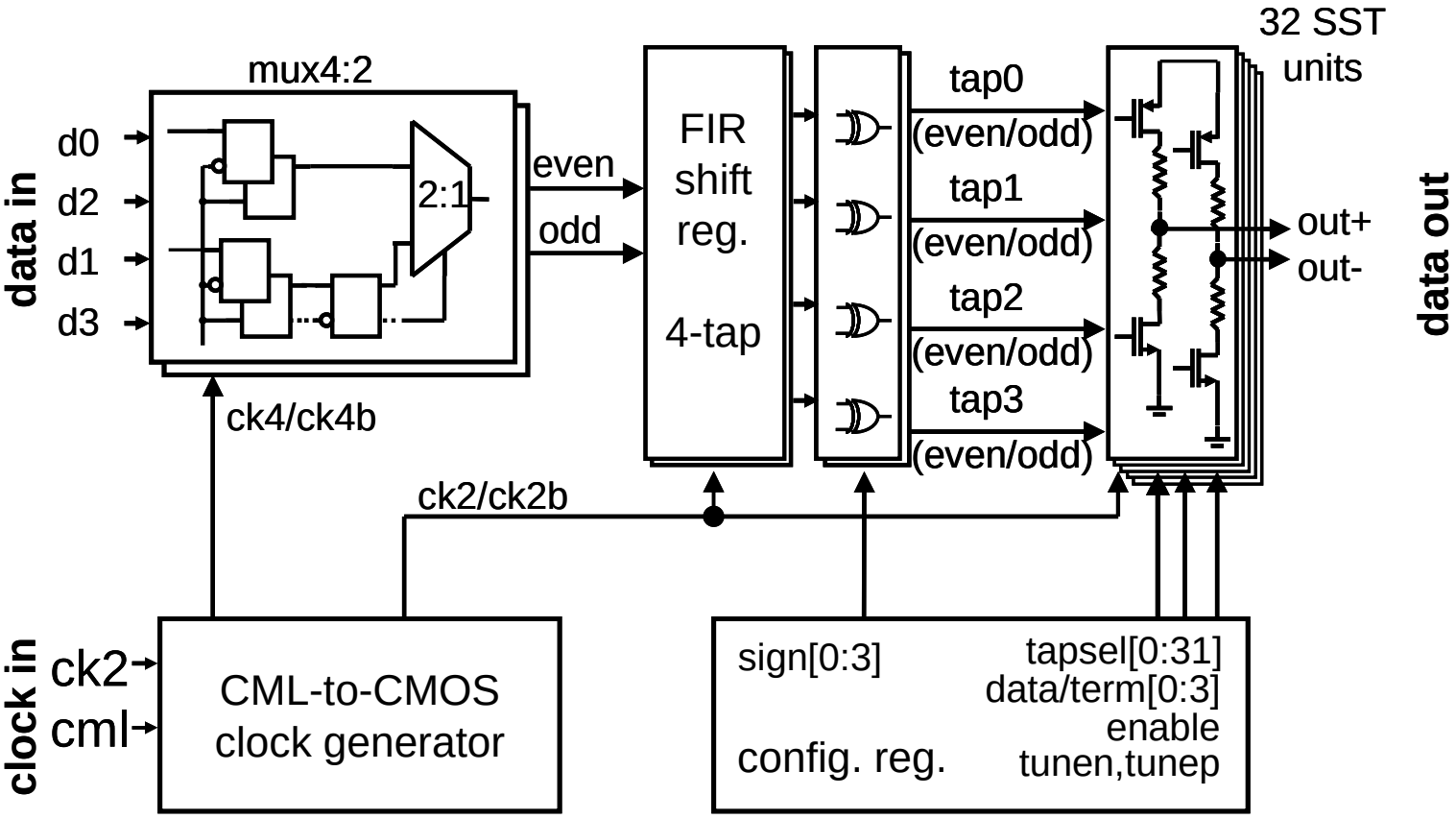
Switched-cap DFE principle



single SC-cap DFE tap

- Current feedback replaced by charge feedback
- Capacitive DAC (6 bits+sign, +/-0..63): 4 binary (1,2,4,8) + 3 bits therm-coded (16,16,16)
- unused caps disconnected by PFET pass transistors (reduced cap loading)
- Transistors used as switches (digital design style, don't care about 'analog' parms like gm, gds)
- DFE timing margin is improved wrt to integrating DFE with current feedback
- Addition of charges is highly linear: needed for large number (e.g. 20) DFE or X-talk cancellation

TX Architecture



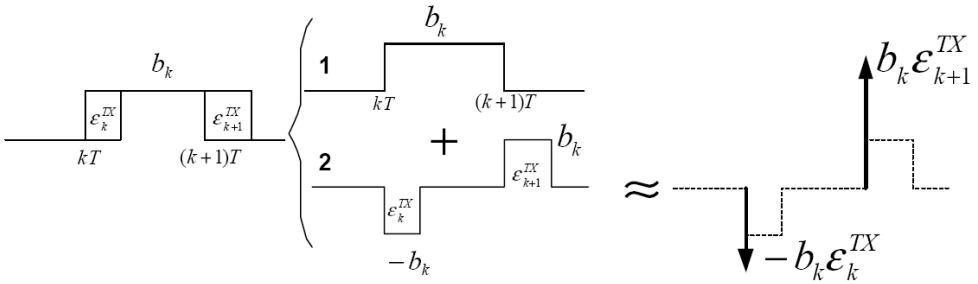
courtesy Christian Menolfi

[1],[5]

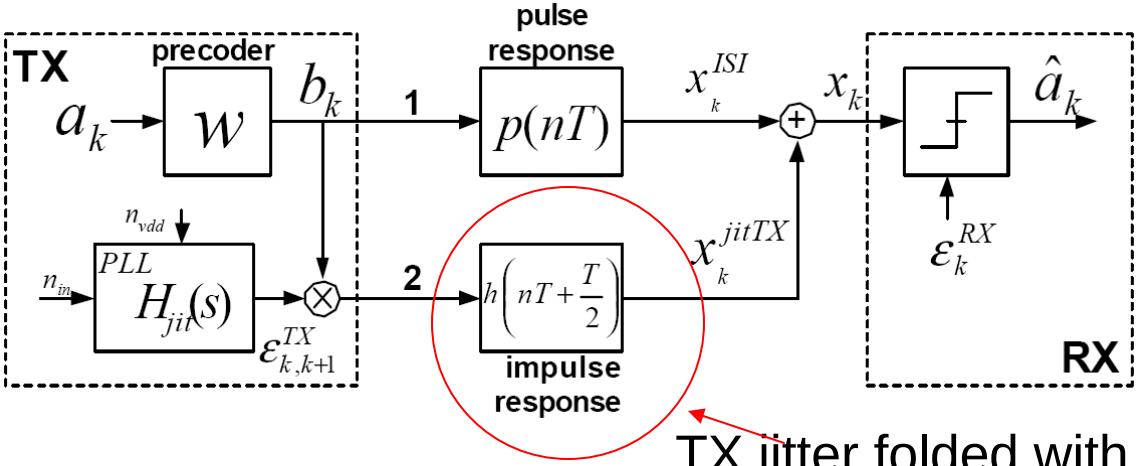
- Half-rate architecture
- 4-tap feed-forward equalizer (FFE)
- Programmable output impedance

Jitter Amplification in High-Loss Channels

- Jitter can be approximated by Dirac impulse at edge position [1]



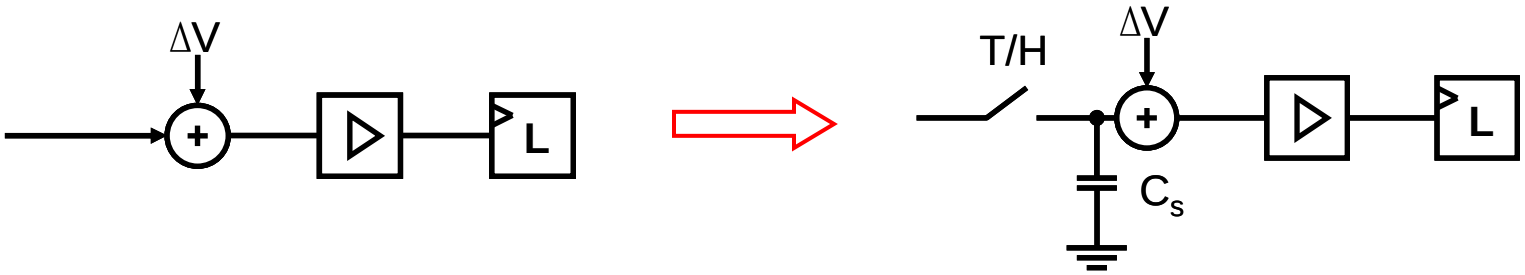
- Jitter is then converted to **voltage noise** in the sampling point



TX jitter folded with channel response

[1] V. Stojanović et al., "Optimal Linear Precoding with Theoretical and Practical Data Rates in High-Speed Serial-Link Backplane Communication", ICC 2004

Sampling in Data Path vs. continuous time data path



- Sampling is done by **T/H** at the input
- Total input capacitance is $N \cdot C_s/2$
- Advantages

  - Signal processing now in **discrete time domain**

    -> Reduced bandwidth requirements due to

    -> Sub-rate

    -> Can use **reset** to erase history

    -> Buffers can use **incomplete settling** or **integration**

P-PLL – Key points:

- Advantages
  - Clocks from VCO go directly into the latches
  - No need for phase rotators
  - Clock path is very short
  - Phase-rotation with XOR phase detectors is inherently linear
  - High-frequency noise on input clock signal is filtered out

- Disadvantages
  - Phase noise is accumulated due to PLL operation

    But: PLL bandwidth is extremely high (>1 GHz for 10GHz clock)

    → Noise is attenuated to large extent
  - Phase-rotation now in feedback-path

    But: No influence on CDR due to high PLL bandwidth

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SST- Transmitter

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[2] M. Kossel, C. Menolfi, J. Weiss, P. Buchmann, G. von Bueren, L. Rodoni, T. Morf, T. Toifl, M. Schmatz, "A T-Coil-Enhanced 8.5Gb/s High-Swing source-Series-Terminated Transmitter in 65nm Bulk CMOS", IEEE Journal of Solid-State Circuits, Vol. 43, pp. 2905-2920, Dec. 2008.

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[13] M. Jeeradit, J. Kim, B. Leibowitz, P. Nikaeen, V. Wang, B. Garlepp, C. Werner, "Characterizing Sampling Aperture of Clocked Comparators", pp 68-69, IEEE Symposium on VLSI Circuits, June 2008.

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Acronyms

ASST	At-Speed Structural Test
BER	Bit Error Rate
CDR	Clock and Data recovery
CML	Current Mode Logic
CTLE	Continuous Time Linear Equalizer
DCVS	Differential Cascode Voltage Switch (circuit)
DFE	Decision Feedback Equalizer
DLL	Delay Locked Loop
FFE	Feed-forward Equalizer
FFT	Fast Fourier Transform
FS-CMOS	Full-swing CMOS (=inverter based clocking)
INL	Integral Non-Linearity
ISI	Intersymbol Interference
LSSD	Level Sensitive Scan Design
PLL	Phase-Locked Loop
P-PLL	Phase Programmable PLL
PPF	Poly-phase filter
RX	Receiver
SC-DFE	Switched-Cap DFE
S.E.	Single-Ended
SOI	Silicon On Insulator
SST	Source-Series Terminated
VCO	Voltage Controlled Oscillator
T/H	Track and Hold
TX	Transmitter