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Low-power High-Speed CMOS I/Os: Design Challenges and Solutions

Thursday, 20 September 2012 14:00 (45 minutes)

Due to the ever-increasing number of transistors on a processor chip, I/Os are more and more becoming the limiting factor on system performance. This presentation will describe the challenges for implementing the physical layer of high-speed wireline I/Os in CMOS in order to achieve both high data throughput and low power consumption. We will discuss how these goals can be met by proper choice of the system architecture, circuit topologies and equalization techniques such as the feed-forward equalizer (FFE), continuous time linear equalizer (CTLE), and decision-feedback equalizer (DFE). We will show examples of recent low-power implementations of transmitter and receiver circuits in CMOS operating at and above 28Gb/s. Looking further ahead, future ADC-based I/Os using digital equalizers will be discussed and compared to currently used analogue implementations.

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