Pulsed power poster introduction

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2008-2011 -> CERN DCDC converters group with F. Faccio and G. Blanchot

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Outline

Vertex barrel detector at CLIC

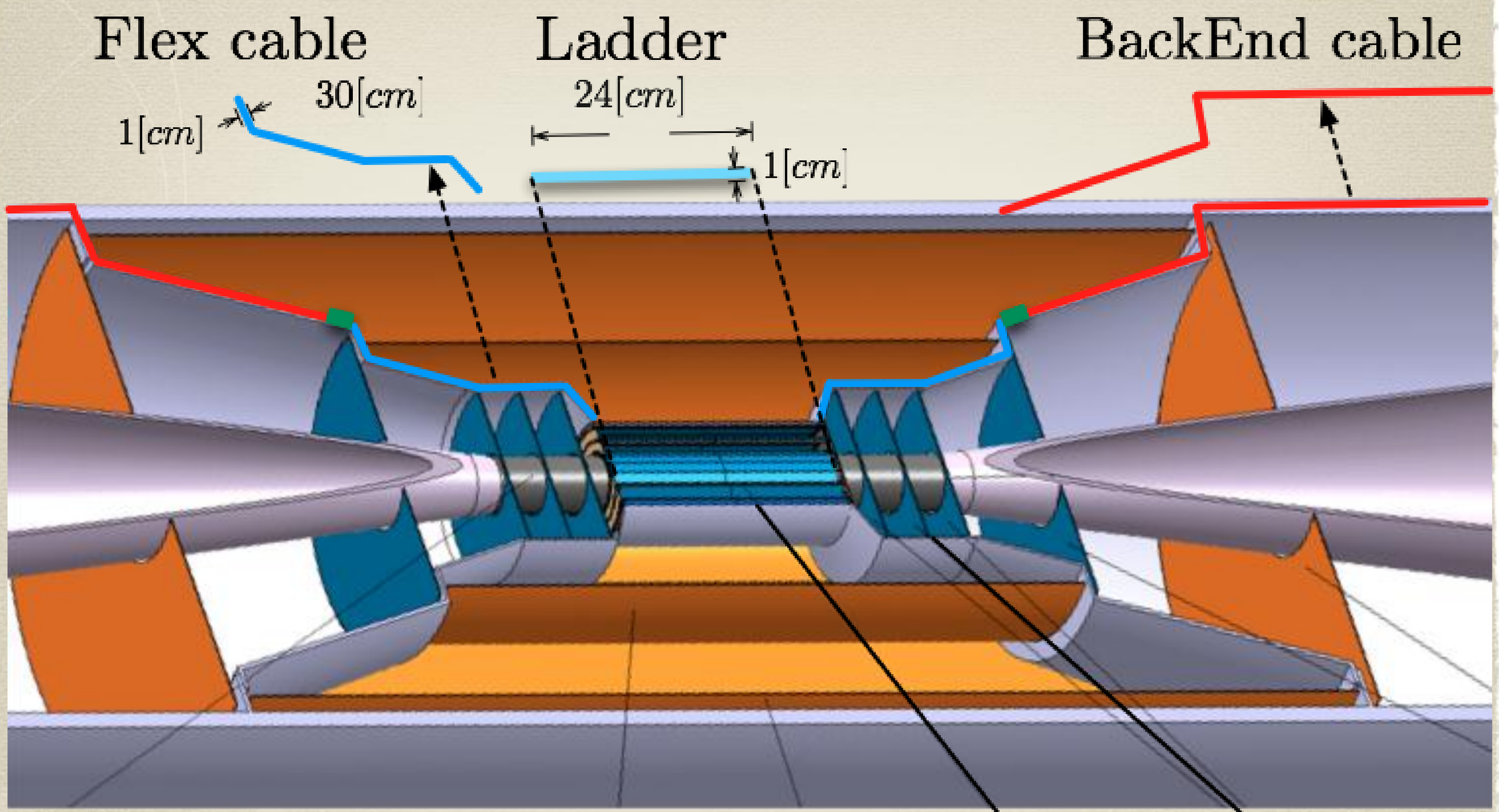
Introduction to the challenges

Analog: Regulation and Material Budget constrains

Proposed scheme + implementation

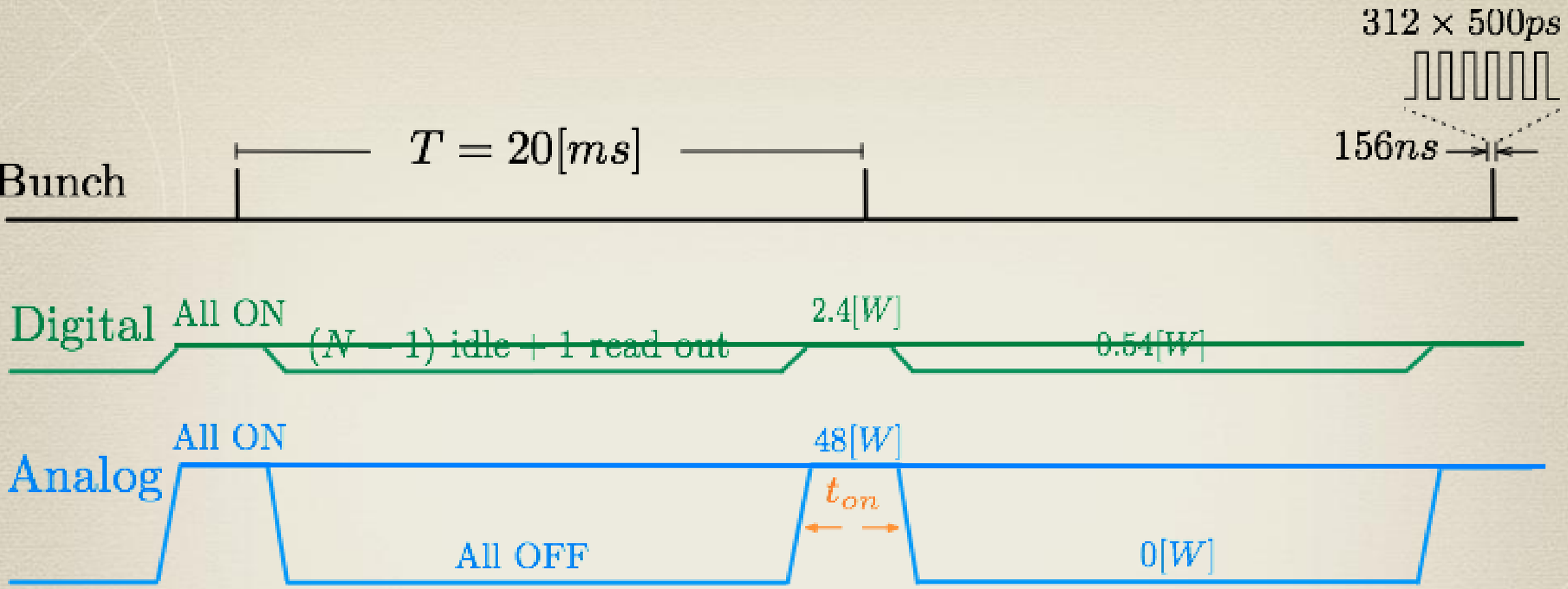
Invitation to my poster

Vertex Barrel detector at CLIC



Ladder: 24 CLICPIX ASICs of 1cm^2 area

Why to power-pulse it?



Values from CLICPIX design specifications

Take advantage of the small duty cycle (or to power-pulse) to reduce the average power.

..but why is it important to reduce average power?

Challenges

1) Low losses: < 50 mW/cm^2 in the sensor area, as the heat-removal solution is based on air-cooling to reduce mass. (must be shared among analog and digital electronics)

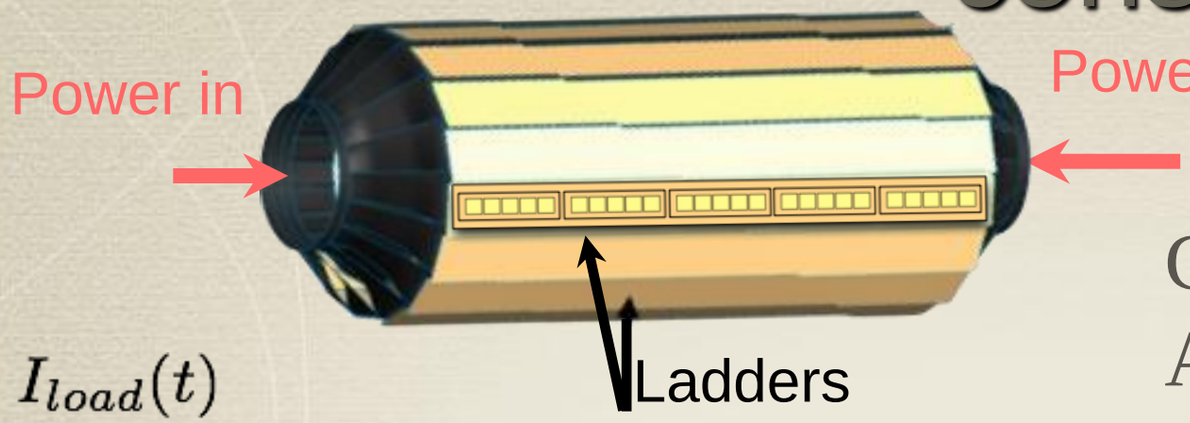
2) High magnetic Field: > 4 [Tesla] restricting the use of ferromagnetic material.

3) Material Budget: < 0.2%Xo for a detection layer, leaving less than 0.1%Xo for cooling and services.

extra challenge for analog electronics

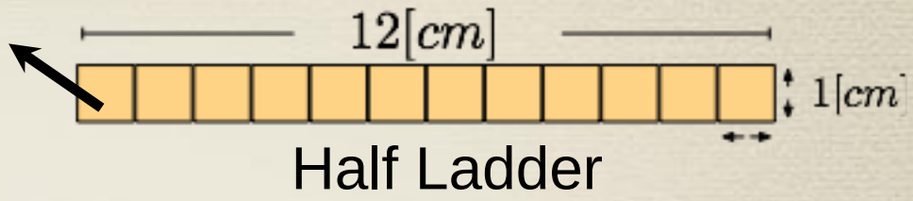
4) Regulation: within 5% (60 mV) on the ASIC during the acquisition time, expected to be close to 15 µs (CLICPIX specifications).

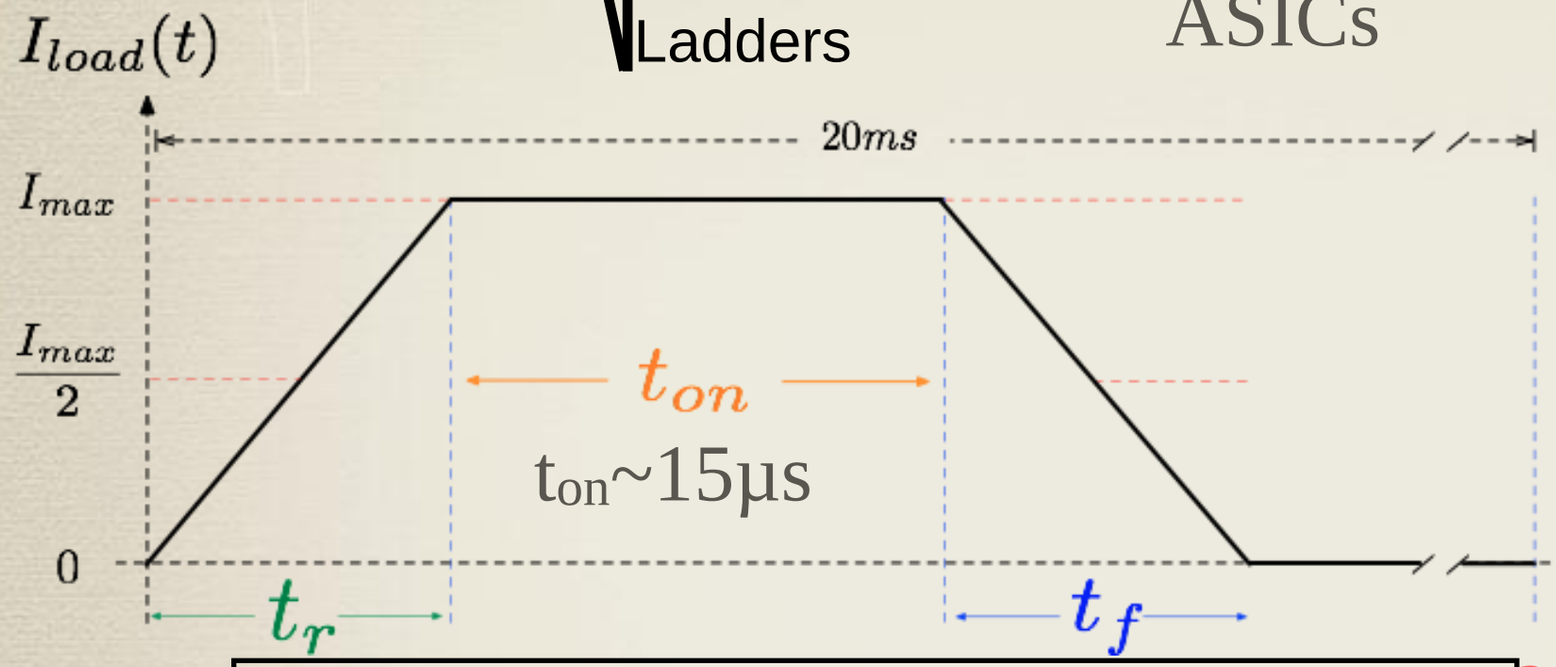
Analog: Regulation and Material Budget constrains



We power half a ladder,
it means 12 chips of 1x1cm^2 area

CLICPIX ASICs





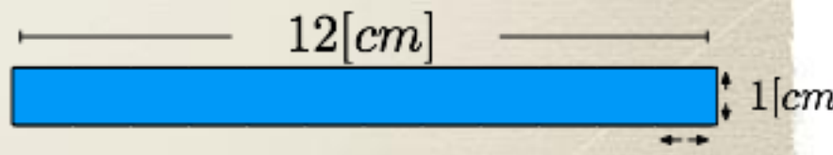
I_{max}=20 A for half ladder

t_{on}~15µs

t_r and t_f : few µs range

Power outside with regulated 1st ASIC

20 A



100µm PCB flex cable for regulation at the last ASIC. (2 copper layers)

Part Name	Material	X0 (mm)	length (mm)	width(mm)	thick (mm)	Number	factor	h eq (mm)	% X0
PCB (copper)	Copper	14,3	120	10	0,1	2	1	0,2	1,40

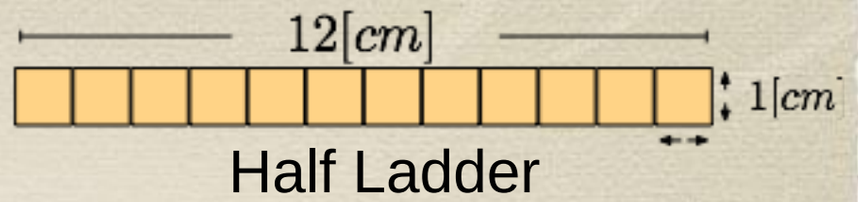
14 times higher than target!!

35µm PCB flex cable. (2 copper layers)

Part Name	Material	X0 (mm)	length (mm)	width(mm)	thick (mm)	Number	factor	h eq (mm)	% X0
PCB (copper)	Copper	14,3	120	10	0,035	2	1	0,07	0,49

Still 5 times higher than target!!

Analog: Regulation and Material Budget constrains



Half Ladder

Lets imagine we want a really low mass cable:

Lets say 8 µm PCB flex cable. (2 copper layers)

Part Name	Material	X0 (mm)	length (mm)	width(mm)	thick (mm)	Number	factor	h eq (mm)	% X0
PCB (copper)	Copper	14,3	120	10	0,008	2	1	0,016	0,11

Still (but slightly) over the target!!

Nevertheless, in order to compensate a so resistive cable (50mOhms) we may need local regulation and/or capacitor storage (remember: 20A required).

Lets add 1 ceramic SMD 1206 capacitor per chip (12 ceramic cap in total)

Part Name	Material	X0 (mm)	length (mm)	width(mm)	thick (mm)	Number	factor	h eq (mm)	% X0
Ceramic Caps 1206	86% $BaTiO_3$, 8% Ni, 6% Sn	18,4	3,2	1,6	1,78	12	1	0,0911	0,50

5 times over target!

Lets just add 1 ceramic SMD 1206 capacitor every four chips (3 cap in total)

Part Name	Material	X0 (mm)	length (mm)	width(mm)	thick (mm)	Number	factor	h eq (mm)	% X0
Ceramic Caps 1206	86% $BaTiO_3$, 8% Ni, 6% Sn	18,4	3,2	1,6	1,78	3	1	0,0228	0,12

Still (but slightly) over the target!!

NOTE: the material of the cable and capacitors must be added.

Proposed scheme + implementation

So what can we use for?

Aluminum flex cables:

For the same resistance of a cable, aluminum has 4 times lower %Xo than copper. Example: For the same resistance than 35µm of copper.

Part Name	Material	X0 (mm)	length (mm)	width(mm)	thick (mm)	Number	factor	h eq (mm)	% X0
PCB (copper)	Copper	14,3	120	10	0,035	2	1	0,07	0,49
PCB (Al)	Aluminium	88,9	120	10	0,054	2	1,00	0,11	0,12

0.49 vs 0.12-> 4 times better!

Silicon capacitors:

Silicon capacitors is another technology that helps to reduce Xo. We can find capacitors with a density of 25uF per cm^2 in a thickness of 100µm.

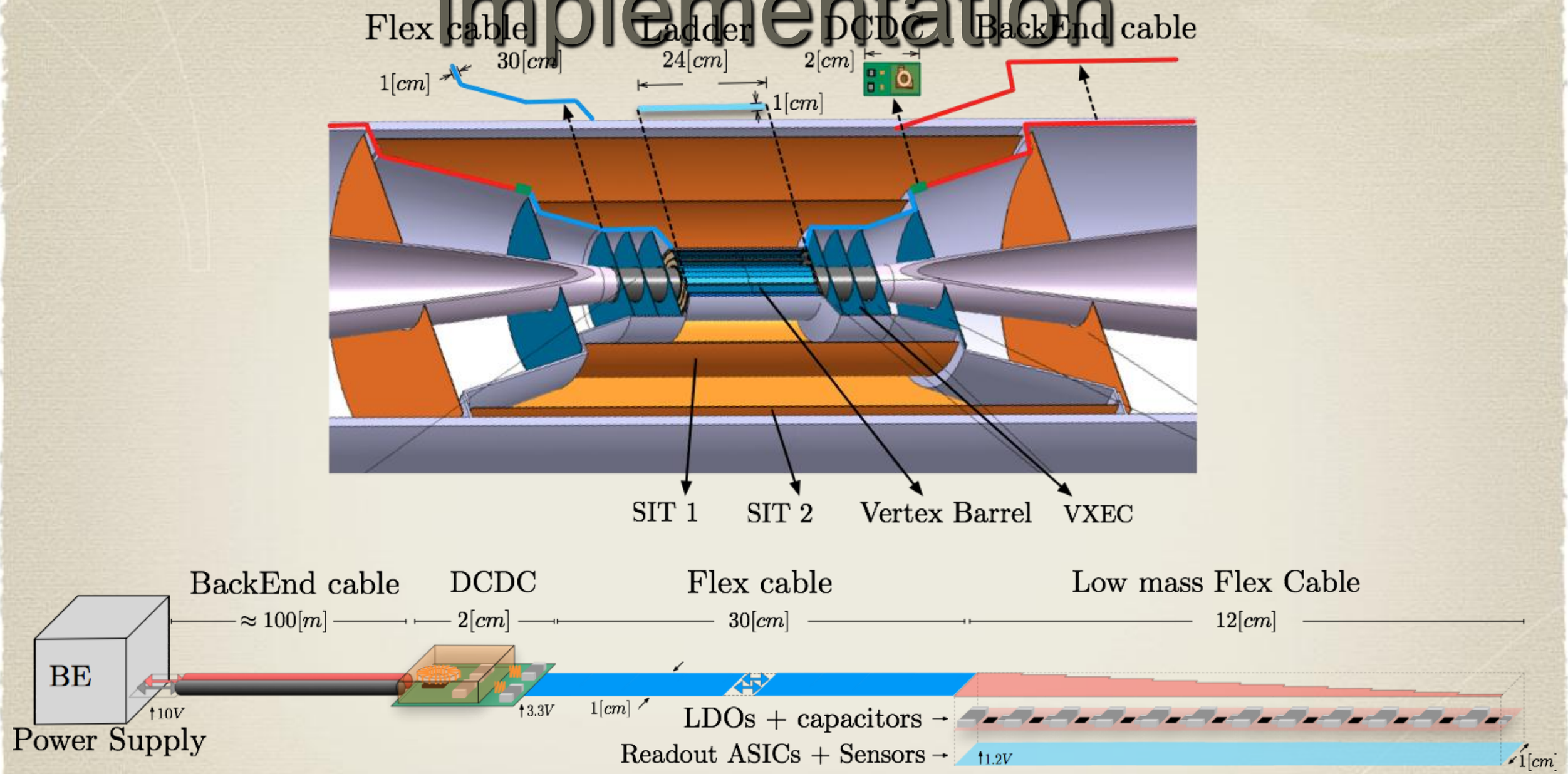
Example: For the same capacitance than 12 smd 1206 capacitors of 10µF.

Part Name	Material	X0 (mm)	length (mm)	width(mm)	thick (mm)	Number	factor	h eq (mm)	% X0
Ceramic Caps 1206	86% $BaTiO_3$, 8% Ni, 6% Sn	18,4	3,2	1,6	1,78	12	1	0,0911	0,50
Input LDO Capacitors	Silicon	93,6	3,2	1,6	0,1	120	1,00	0,0512	0,055

0.5 vs 0.055-> almost 10 times better!

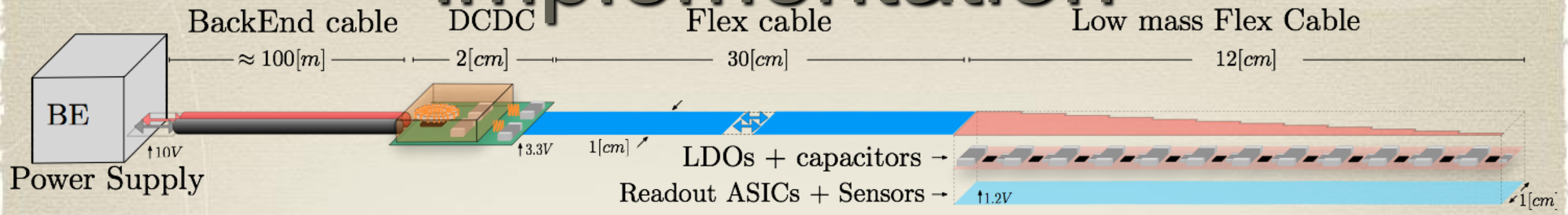
NOTE: Silicon capacitors have higher ESR than ceramic capacitors. In the order of 100-400 mOhms

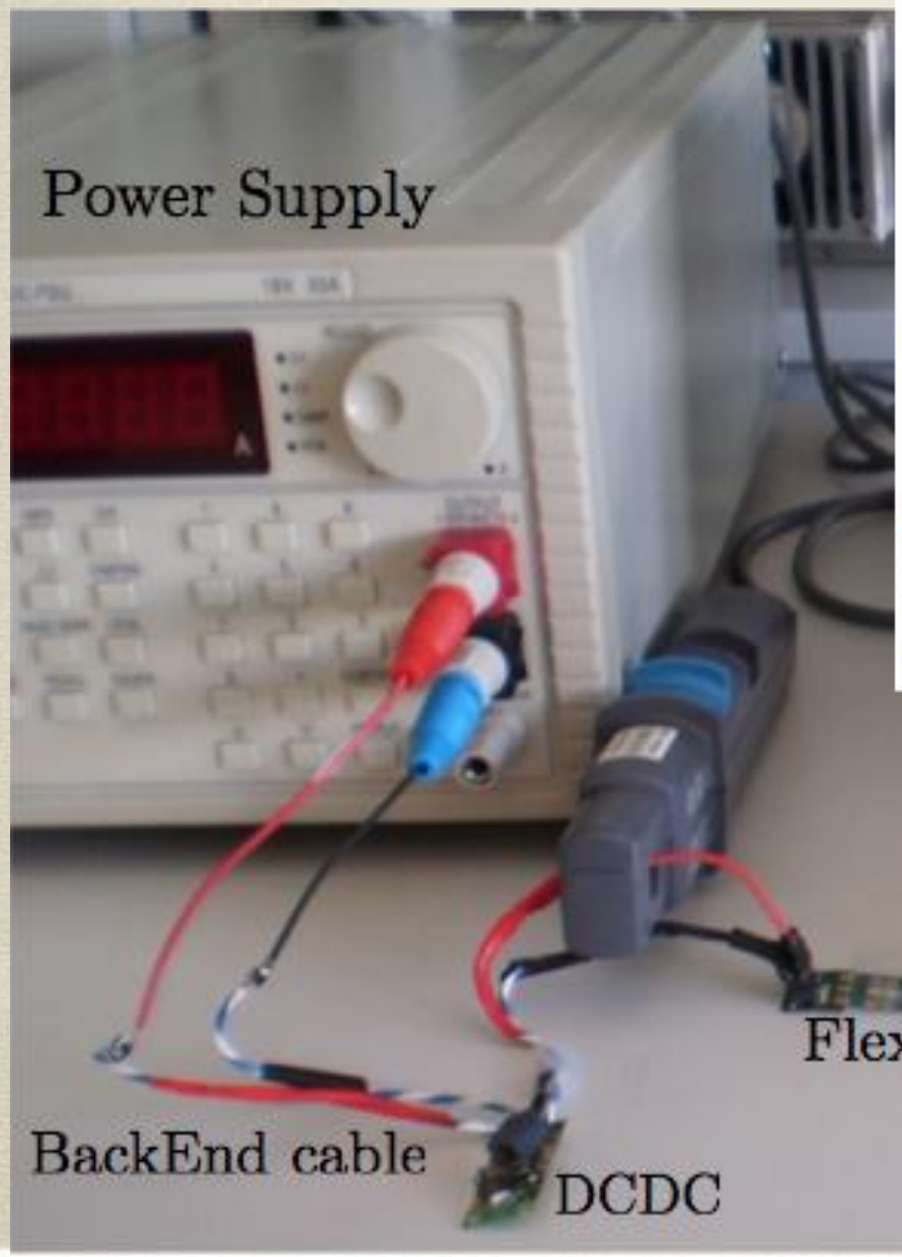
Proposed scheme + implementation

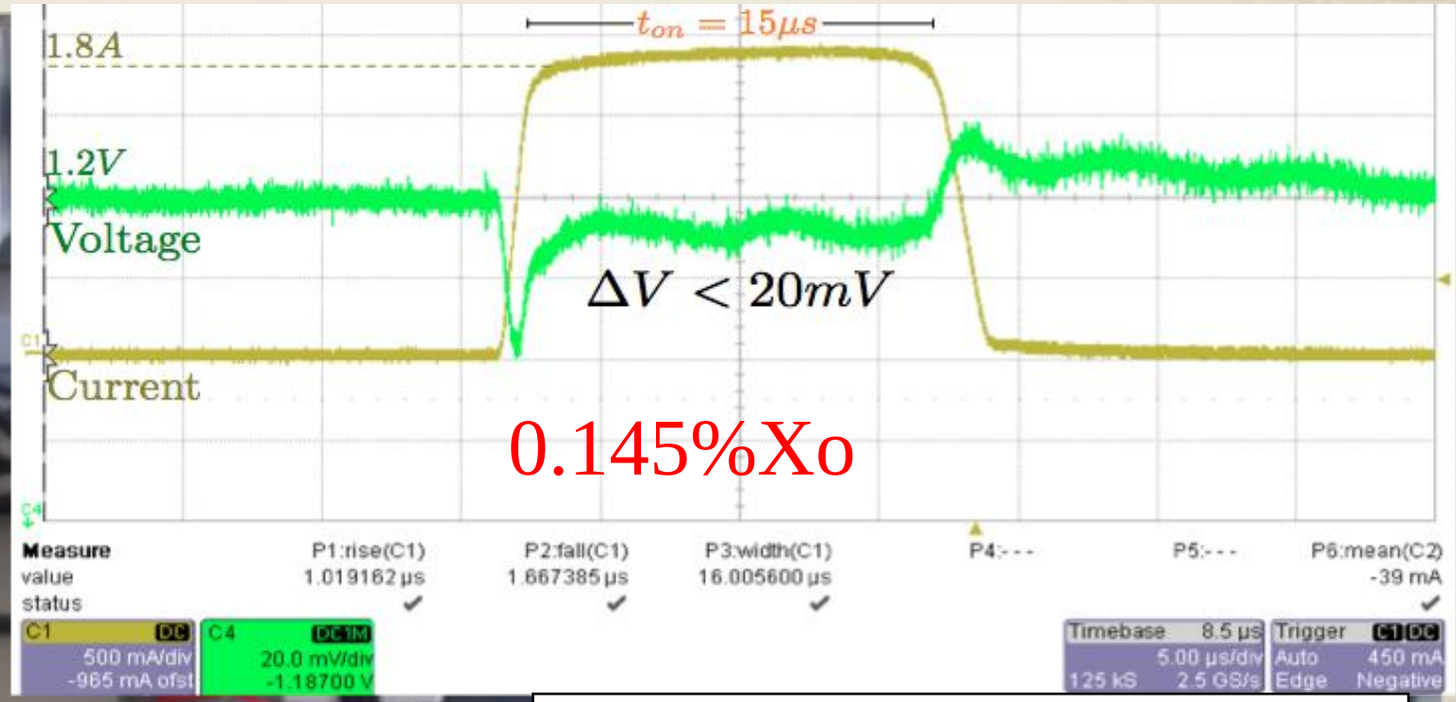


The front end readout ASICs are now under development. In order to test the proposed pulsed-powered scheme, their behavior was emulated using a PCB.

Proposed scheme + implementation







0.145%Xo

With future work we expect to reduce it below 0.1%Xo

Invitation to the poster...

So if you are interested in:

-further details of the proposed power scheme

-the currently obtained results

-how they will be improve with future work

-Share your knowledge and ideas with me

-Or just to make my thursday afternoon funnier :)

you are most welcome to see my poster tomorrow, located at B10