xTCA developments for the LHCb Readout

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Outline

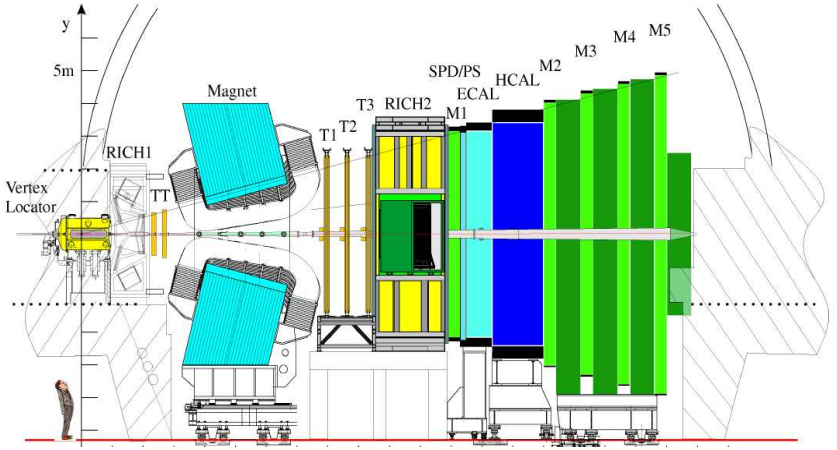
- Readout architecture
- Generic readout board
- Data paths
- Compatibility with xTCA for Physics
- Current prototype
- Early test setup
- Possible development sharings
- Next steps

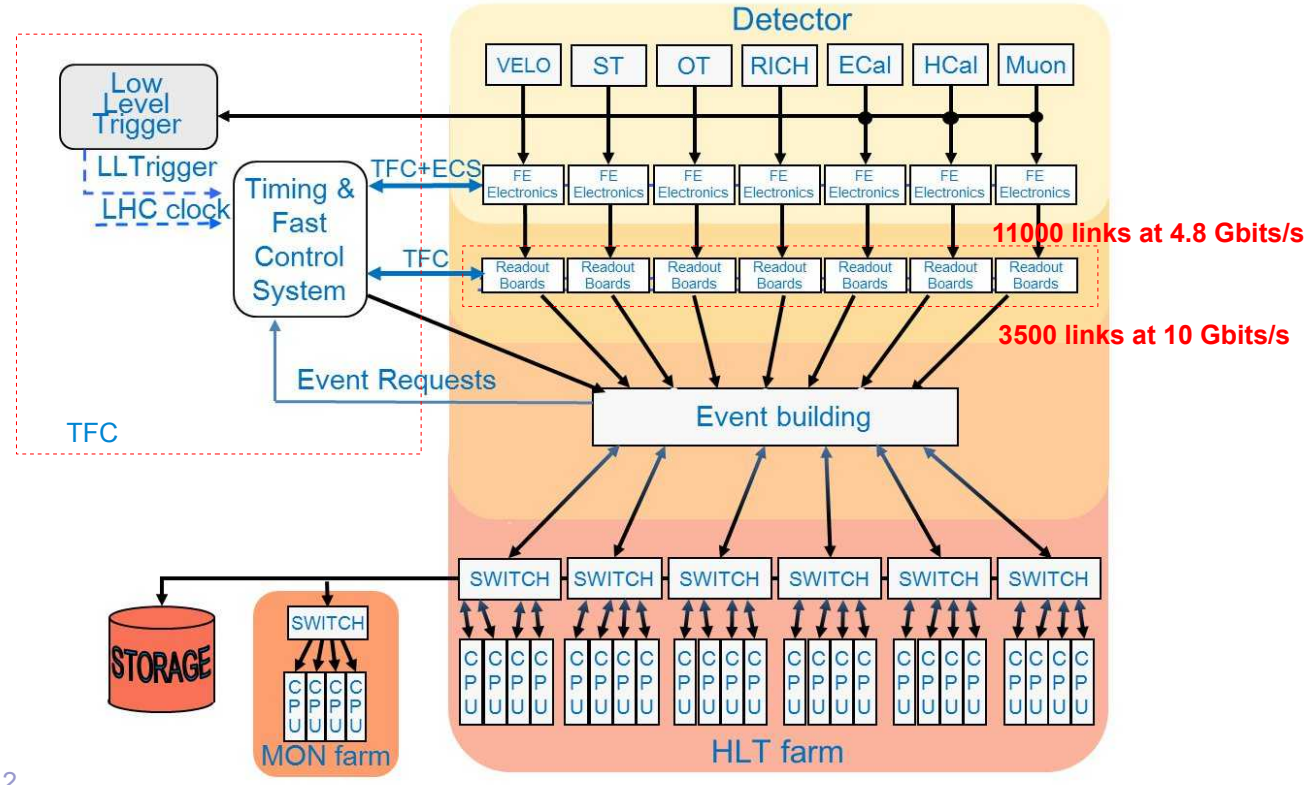
General architecture

LHCb Readout system

5 main blocks :

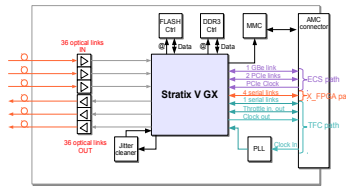
- FE
- Readout boards
- TFC system
- Online network
- HLT Farm





Generic readout board

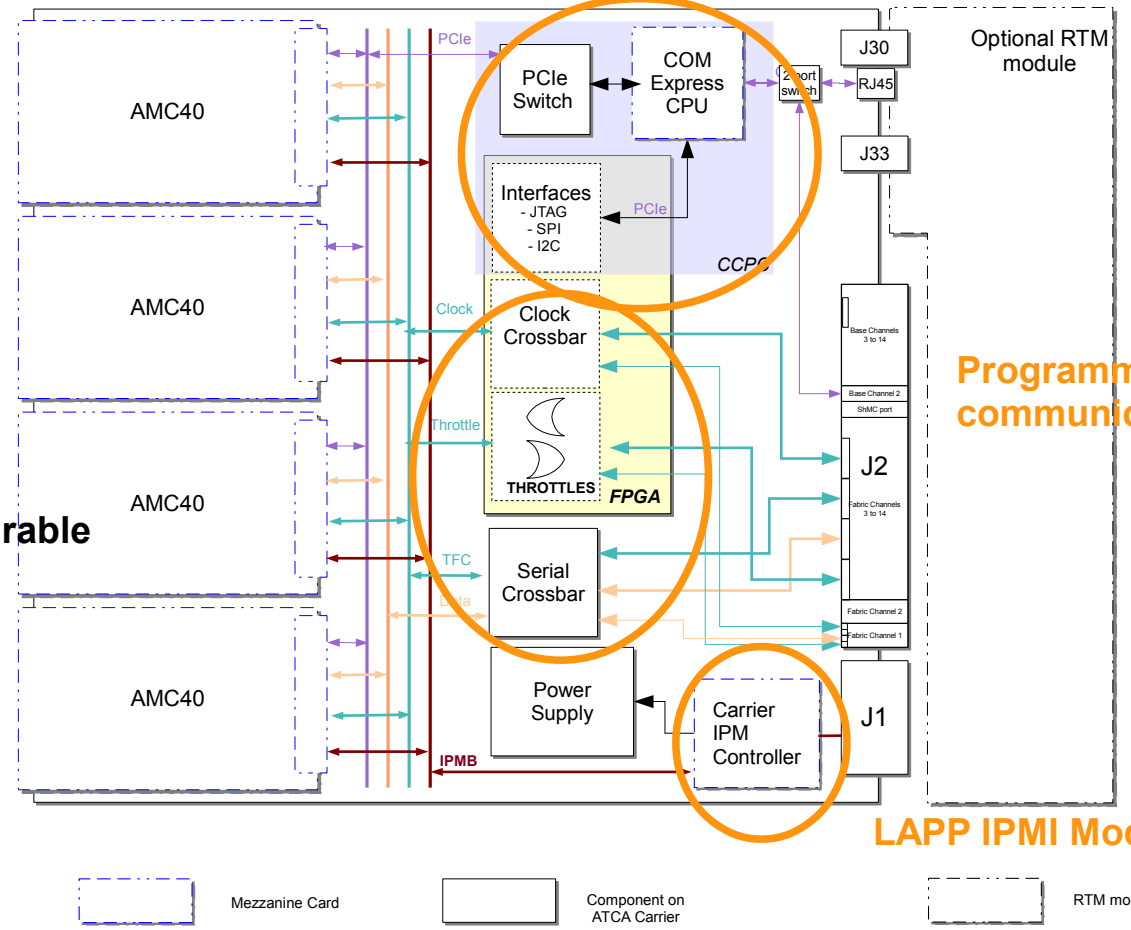
AMC40



Flexible and reconfigurable carrier board

144 optical links :
- **96** GBT links
- **48** 10GbE links

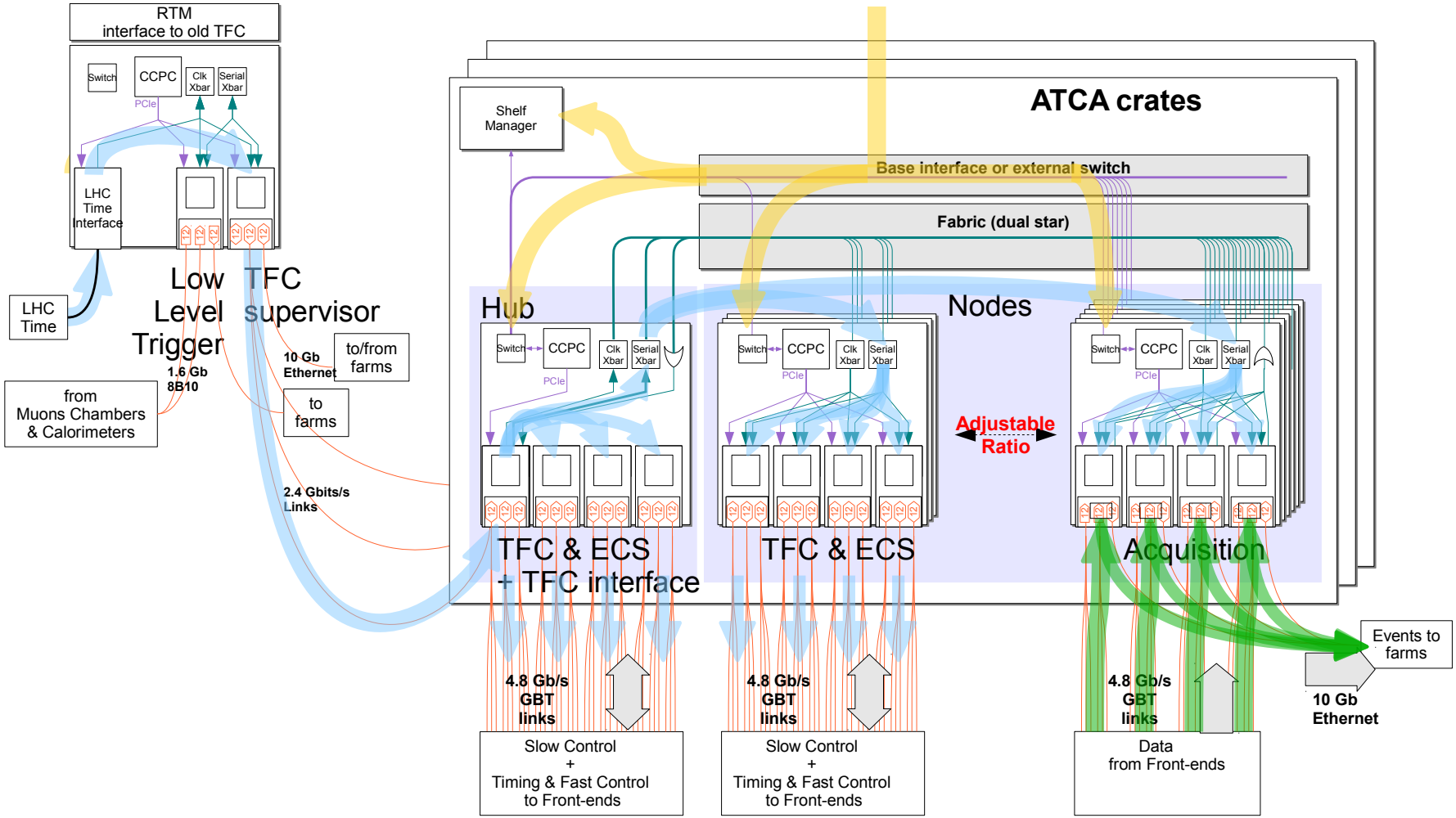
ATCA40



Different firmwares to implement readout, time distribution, slow control, trigger interface

Data paths
&
Compatibility with xTCA for Physics

Data paths : Acquisition
Timing and Fast Trigger
Slow control



Timing distribution

Implemented on fabric

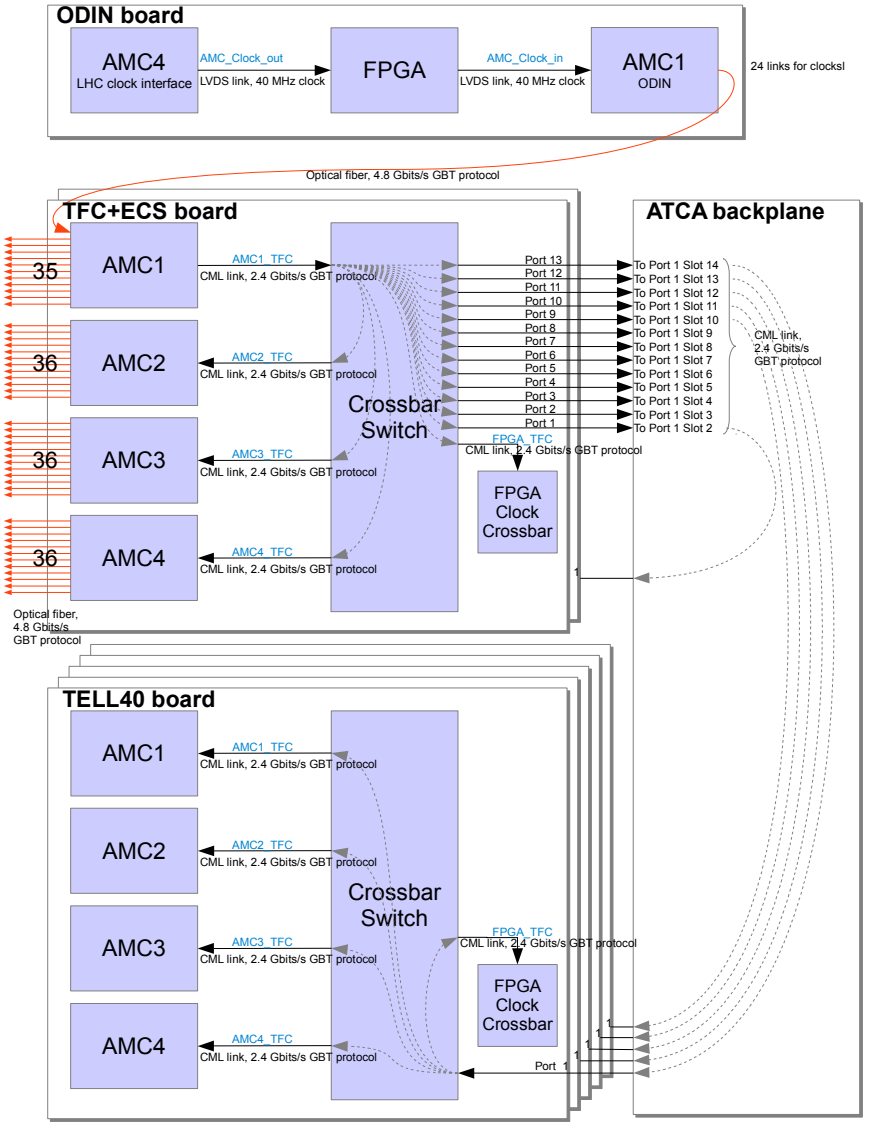
- Dual star topology
  - not used for redundancy
  - Possibility to feed 2 clocks and triggers to different boards : 2 groups working on side A and side B

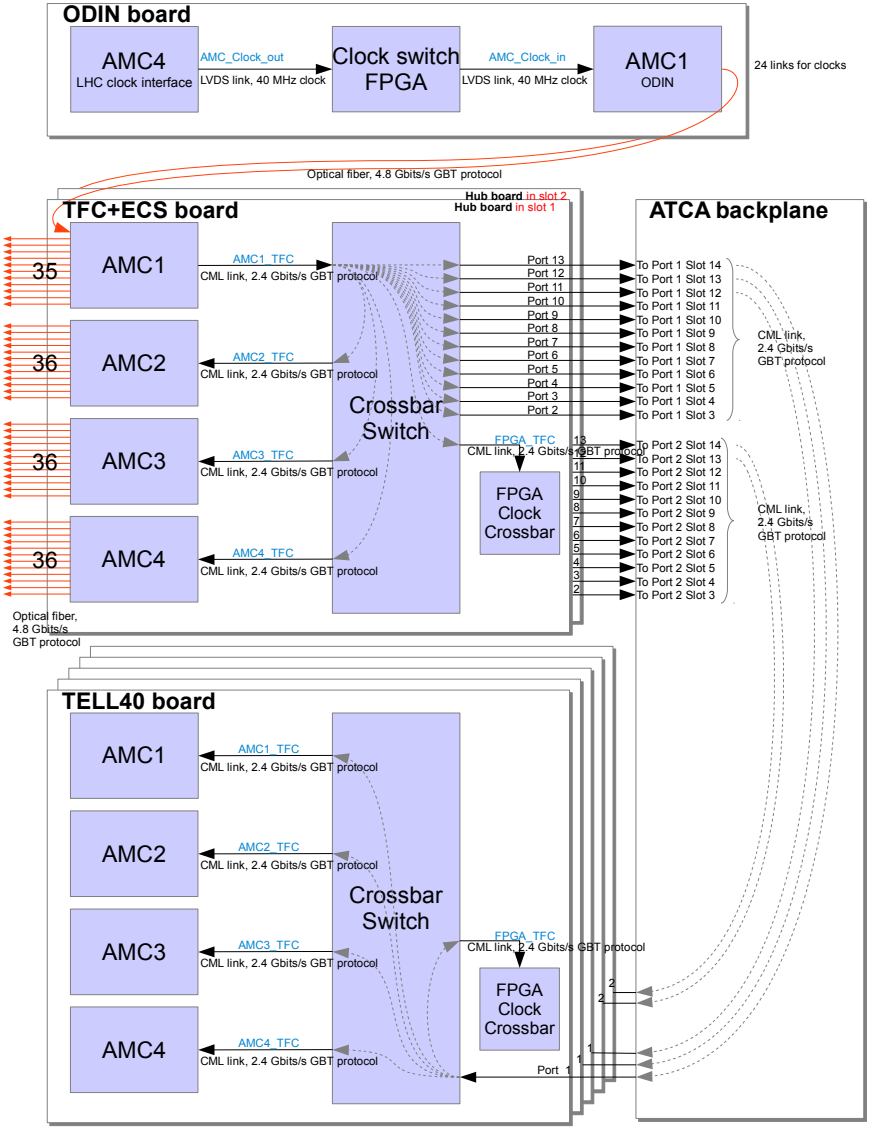
Signals used on the fabric

- **TFC**: CML for clock + trigger (not interleaved 2.4 Gbits/s GBT protocol)
- **Throttle** : LVDS (800 Mbits/s)
- *Optional :*
  - *LVDS Clock*
  - *2 bidirectional 8B10B CML links for board communication*

		Hub Channel i (2 to 14)		Backplane Links	Node i (2 to 14) Channel 1		Signal type
Row	Column (+/-)	*Connector name*	*Board Name*		*Connector name*	*Board Name*	
n	ab	**TX0_i**	X_FPGA_TX0_i		**TX0_1**	X_FPGA_TX0_1	**CML**
	cd	**RX0_i**	X_FPGA_RX0_i		**RX0_1**	X_FPGA_RX0_1	**CML**
	ef	**TX1_i**	X_FPGA_TX1_i		**TX1_1**	X_FPGA_RX1_1	**CML**
	gh	**RX1_i**	X_FPGA_TX1_i		**RX1_1**	X_FPGA_RX1_1	**CML**
n-1	ab	**TX2_i**	TFC_TX_i		**TX2_1**	TFC_TX_1	**CML**
	cd	**RX2_i**	TFC_RX_i		**RX2_1**	TFC_RX_1	**CML**
	ef	**TX3_i**	Clock_i_OUT		**TX3_1**	Throttle_OUT	**LVDS**
	gh	**RX3_i**	Throttle_i_IN		**RX3_1**	Clock_IN	**LVDS**

Clocks and trigger: two possible schemes

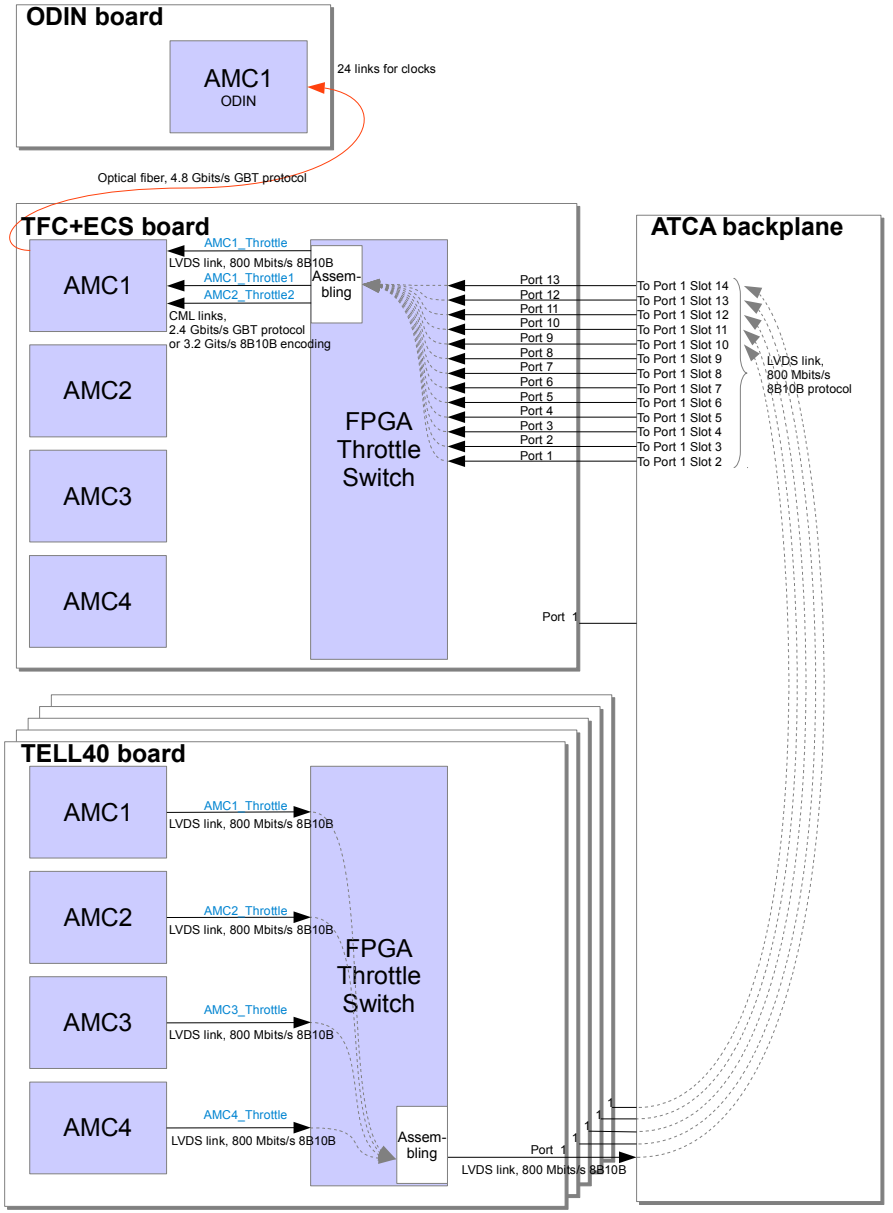




Throttles

Implemented on fabric

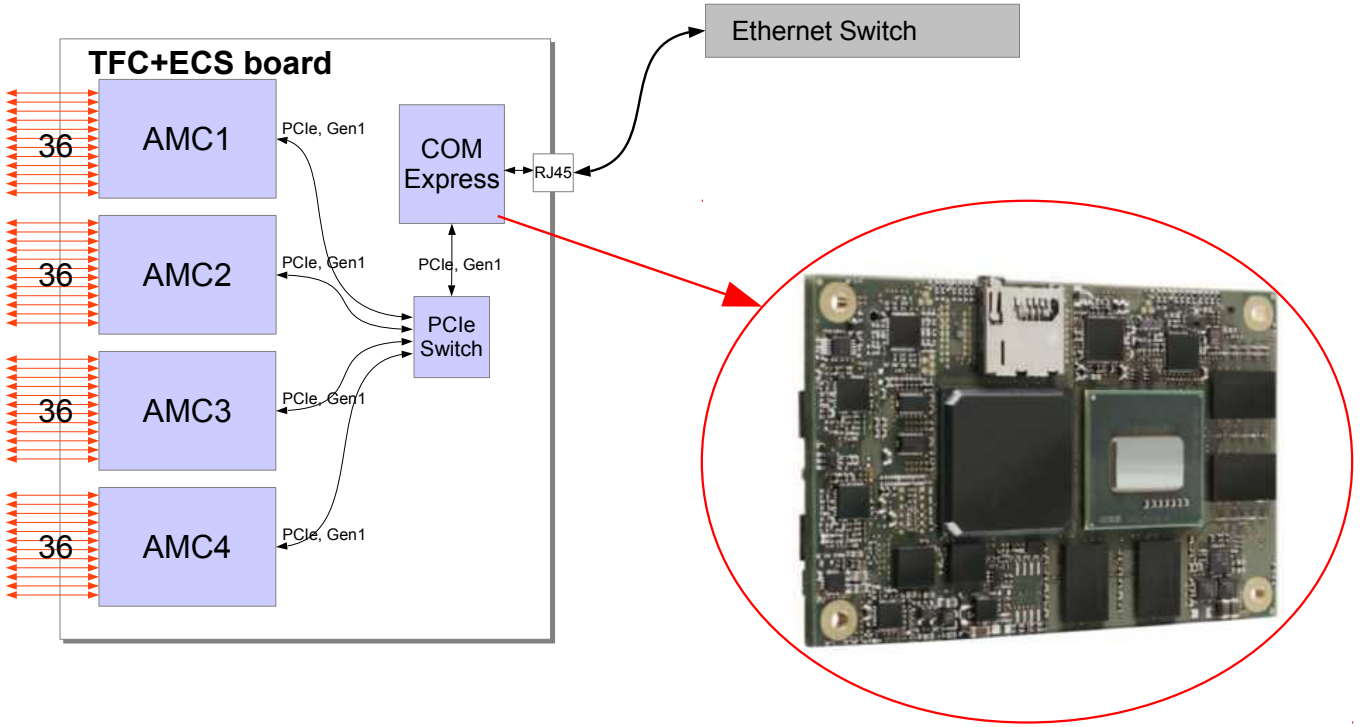
- *8B10B 800 Mbits/s LVDS link*
- *12 Bxld bits + 1 throttle bit per AMC card*



ECS path

Main features

- COM Exporess module type 10
- 1 GbE link per card connected to external switch
- Local control : PCIe

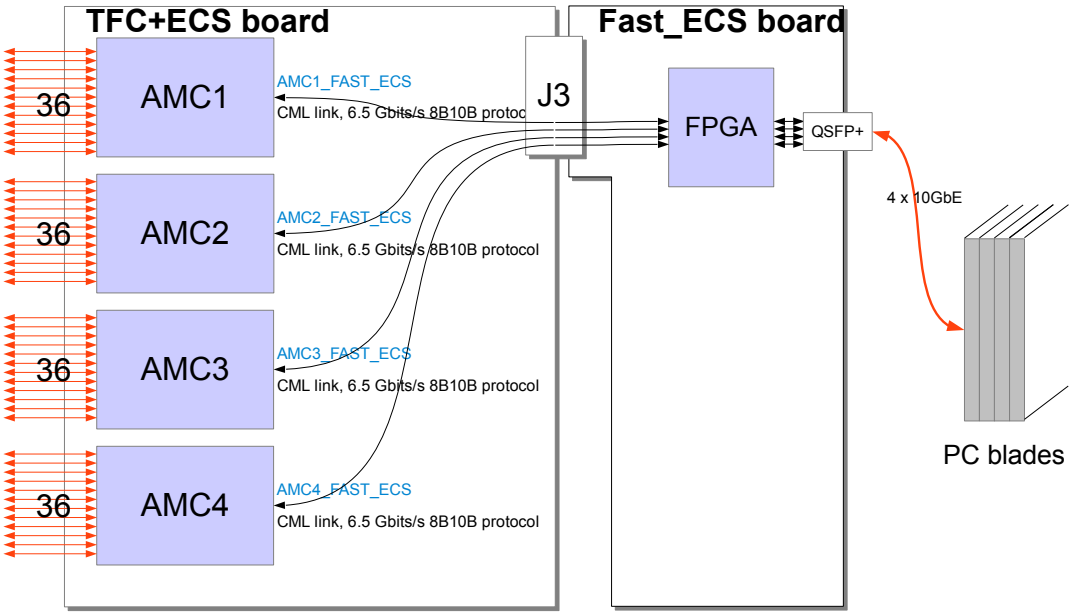


Possible drawback : GbE = bottleneck when many FE

ECS path

Fallback solution

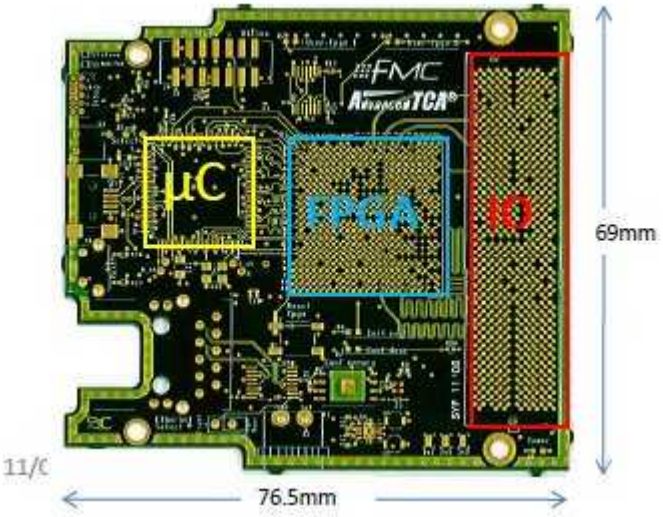
- Use of a Fast_ECS board
  - Up to 20 Gbits/s bandwidth



IPMI chain

Use of already tested solutions

- DESY/CPPM/CERN MMC module (integrated in AMC board)
- CIPMC validated by LAPP with 2 modifications
  - Smaller form factor to better fit an ATCA carrier
  - AMC management currently being added



Version 1

Version 2
(ARM Cortex M4)

Compatibility with xTCA for Physics

Reference document for clock distribution in elaboration by WG1 Timing and Synchronization

- CGT guidelines document: Clock Gate and Timings
  - Not released yet
  - Not a specification
- Several authorized schemes
- **Fabric interface** scheme chosen
  - But Tell40 does not follow recommendation to distribute clock from slot 3
    Slot 1 prefered for density reasons
    → allowed configuration (see below)

Timing interface	Ports	Lines available	Performance	Compatibility
Synchronization Clock Interface	CLK1, CLK2 re-assigned. CLK3 user definable.	6 bussed diff pairs	Fair 100 MHz	Compatible
Shared Fabric Interface	Clock and Data lines share a fabric port.	All nodes receive/send up to 6 distinct clock signals	Good ~3 GHz radial <100 ps jitter	Changes to PICMG 3.x required. Lowers the data rate.
Fabric Interface (Clock hub)	Timing hub in slot 3;4 Ports 3;4 on node cards	All nodes receive/send up to 8 distinct clock signals	Good [1] ~3 GHz radial <100 ps jitter	New e-Keying type may be required.
RTM Zone 3 Backplane Clock Interface	Full-mesh of clock ports on J33 of Zone 3 (RTM).	Full-mesh of two P2P lines; 14 bused lines.	Excellent [2] Low skew Low jitter	Compatible.
Update Channel Interface	Update channel ports redefined for timing.	Up to 10 additional, equal length, low crosstalk diff pairs.	Excellent [2] Low skew Low jitter	Not compatible if update channels are used. Requires new backplane.
Base interface (encoded time)	Ethernet hub in Slot 1 (and 2).	IEEE-1588 time encoded on Ethernet. Disciplined clock and time signals.	<50 ns rms time stamp jitter Very low clock jitter	Compatible.
Fabric Interface (encoded time)	Ethernet/PCIe/SRIO hub in slots 1 (and 2).	Time encoded on Ethernet/ PCIe/ SRIO. Disciplined clock and time signals.	Good [1] ~3 GHz, P2P <100 ps jitter	Compatible PCIe/ SRIO protocol unknown.

When no specific hub card is required on Slot 1(2), a Clock hub card can be inserted in Slot 1(2) to provide a (dual-)star of point-to-point clock ports to the 13[15] node boards (12[14] in redundant systems). This hub is non-standard (unlike Ethernet or PCIe hubs) but the approach is functional if all other node boards accept the clock interface in Port 1(2).

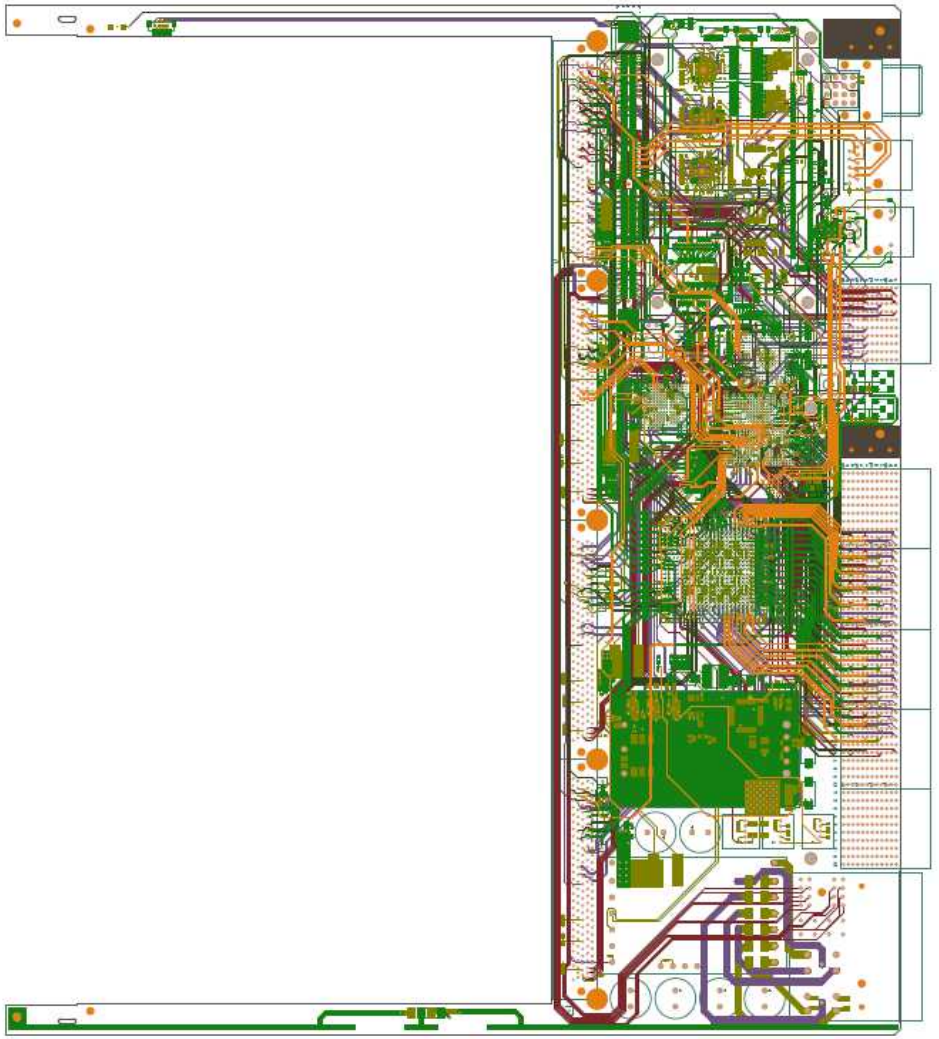
Full scale prototype

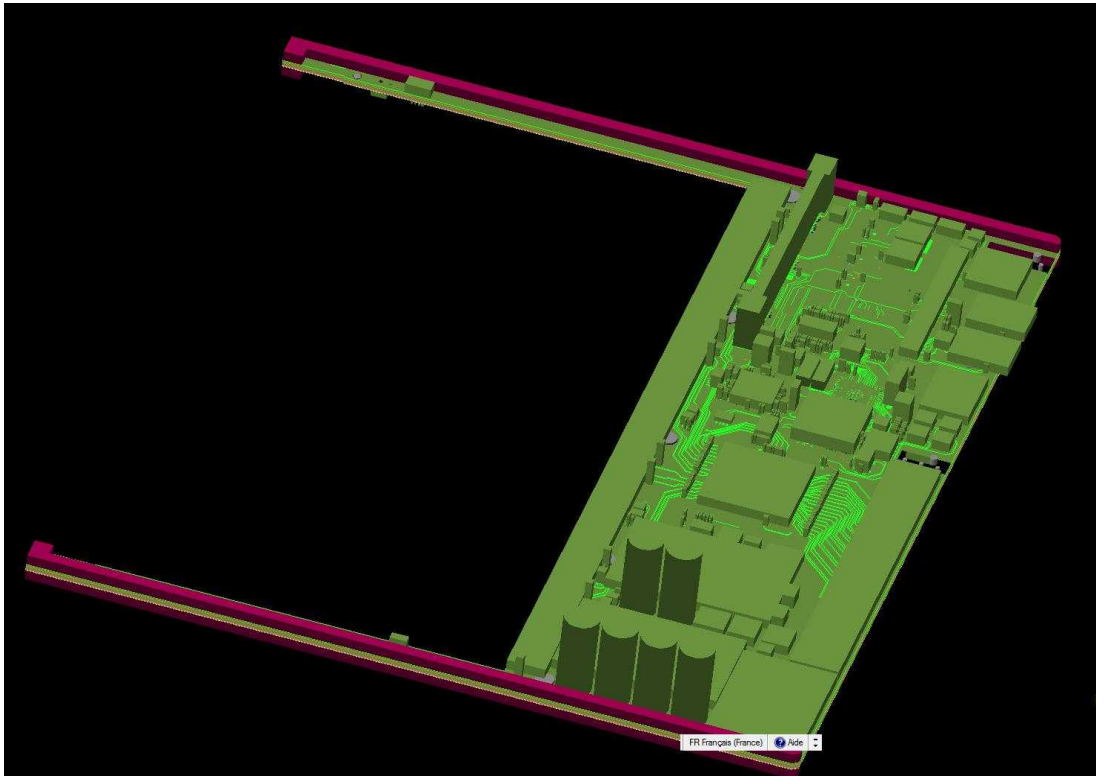
AMC40


AMC40
1 Stratix V GX
36 inputs and 36 outputs at 10 Gbits/s
Slow control through PCIe

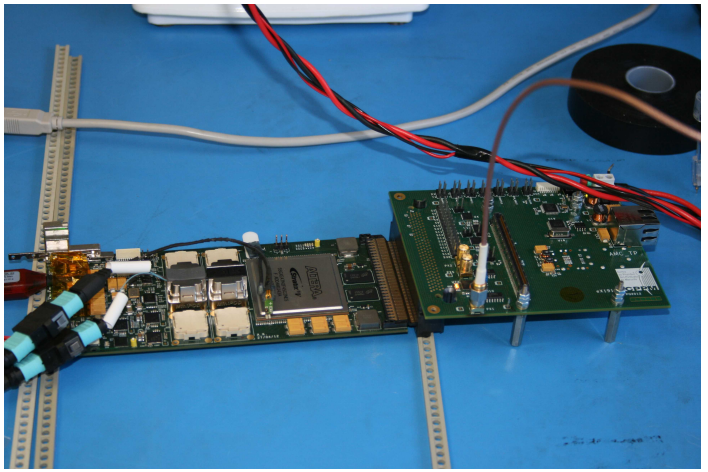
ATCA40

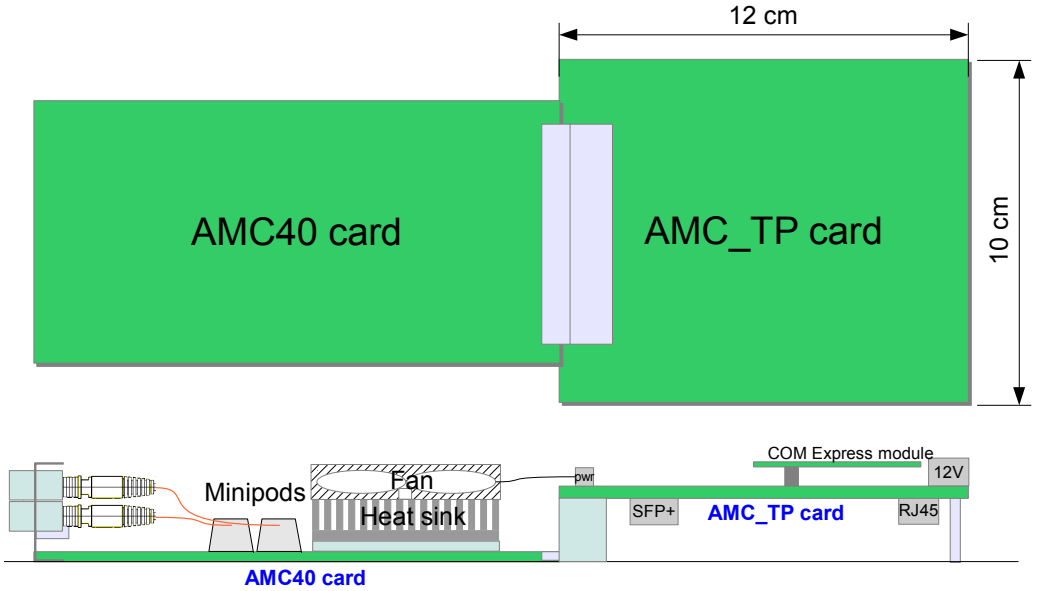
Routing nearly ended

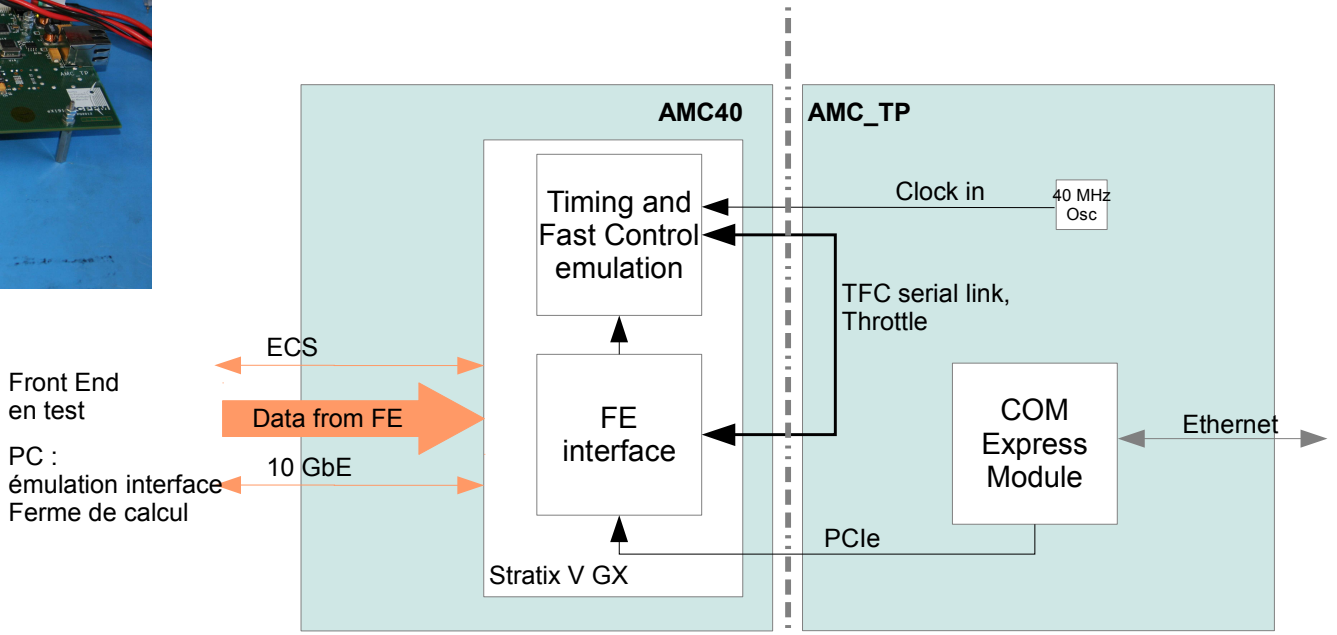




Early test setup AMC_TP card







AMC40 and AMC_TP connection

Possible shared developments

Several easily envisageable :

- Crate:
  - Common mechanics
  - Mechanics adaptation for vertical airflow
- IPMI:
  - Same hardware
  - Same supervision software
- Else ?

Synergy with ATLAS

Conclusion

ATCA chosen by LHCb for implementing first version of the readout system

- Feasibility has to be demonstrated end 2012

Many converging developments

- We should reach this goal

Large effort because xTCA is new

- Development sharing for common parts welcome

Full mesh and dual star ATCA fabric

	Logical Slot #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Connect or	Channel #															
P20	15	16-1	16-2	16-3	16-4	16-5	16-6	16-7	16-8	16-9	16-10	16-11	16-12	16-13	16-14	16-15
P20	14	15-1	15-2	15-3	15-4	15-5	15-6	15-7	15-8	15-9	15-10	15-11	15-12	15-13	15-14	14-14
P20	13	14-1	14-2	14-3	14-4	14-5	14-6	14-7	14-8	14-9	14-10	14-11	14-12	14-13	13-13	13-14
P21	12	13-1	13-2	13-3	13-4	13-5	13-6	13-7	13-8	13-9	13-10	13-11	13-12	12-12	12-13	12-14
P21	11	12-1	12-2	12-3	12-4	12-5	12-6	12-7	12-8	12-9	12-10	12-11	11-11	11-12	11-13	11-14
P21	10	11-1	11-2	11-3	11-4	11-5	11-6	11-7	11-8	11-9	11-10	10-10	10-11	10-12	10-13	10-14
P21	9	10-1	10-2	10-3	10-4	10-5	10-6	10-7	10-8	10-9	9-9	9-10	9-11	9-12	9-13	9-14
P21	8	9-1	9-2	9-3	9-4	9-5	9-6	9-7	9-8	8-8	8-9	8-10	8-11	8-12	8-13	8-14
P22	7	8-1	8-2	8-3	8-4	8-5	8-6	8-7	7-7	7-8	7-9	7-10	7-11	7-12	7-13	7-14
P22	6	7-1	7-2	7-3	7-4	7-5	7-6	6-6	6-7	6-8	6-9	6-10	6-11	6-12	6-13	6-14
P22	5	6-1	6-2	6-3	6-4	6-5	5-5	5-6	5-7	5-8	5-9	5-10	5-11	5-12	5-13	5-14
P22	4	5-1	5-2	5-3	5-4	4-4	4-5	4-6	4-7	4-8	4-9	4-10	4-11	4-12	4-13	4-14
P22	3	4-1	4-2	4-3	3-3	3-4	3-5	3-6	3-7	3-8	3-9	3-10	3-11	3-12	3-13	3-14
P23	2	3-1	3-2	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13	2-14
P23	1	2-1	1-1	1-2	1-3	1-4	1-5	1-6	1-7	1-8	1-9	1-10	1-11	1-12	1-13	1-14

Full mesh

Logical Slot #		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Connector	Fabric Channel #																
P20	15	16-1	16-2														
P20	14	15-1	15-2														
P20	13	14-1	14-2														
P21	12	13-1	13-2														
P21	11	12-1	12-2														
P21	10	11-1	11-2														
P21	9	10-1	10-2														
P21	8	9-1	9-2														
P22	7	8-1	8-2														
P22	6	7-1	7-2														
P22	5	6-1	6-2														
P22	4	5-1	5-2														
P22	3	4-1	4-2														
P23	2	3-1	3-2	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13	2-14	2-15
P23	1	2-1	1-1	1-2	1-3	1-4	1-5	1-6	1-7	1-8	1-9	1-10	1-11	1-12	1-13	1-14	1-15

Dual star