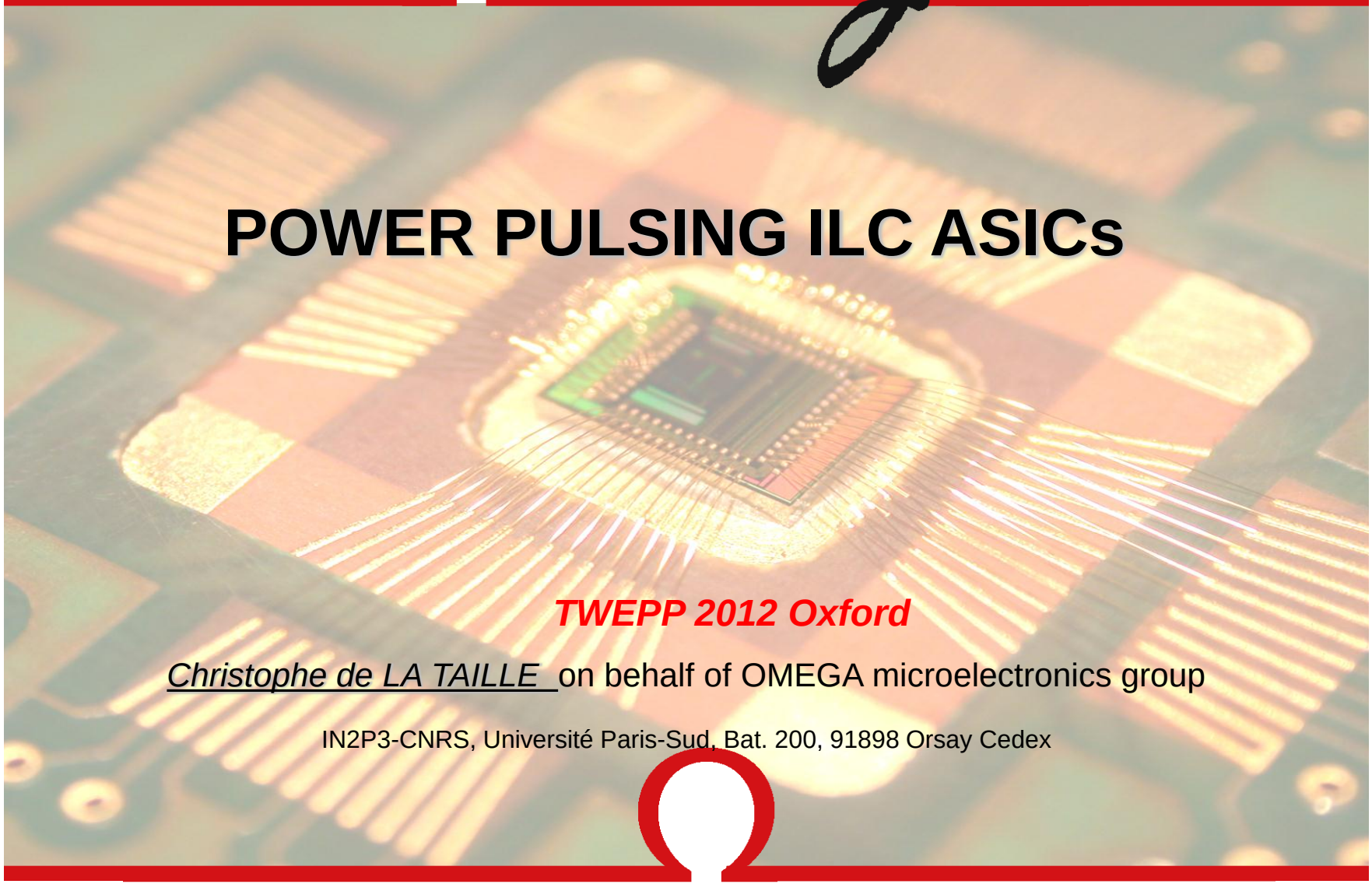


POWER PULSING ILC ASICs

TWEPP 2012 Oxford

Christophe de LA TAILLE on behalf of OMEGA microelectronics group

IN2P3-CNRS, Université Paris-Sud, Bat. 200, 91898 Orsay Cedex

Orsay MicroElectronics Group Associated

POWER :
a hot issue for ILC

It is gonna heat, hopefully, there is the power pulsing

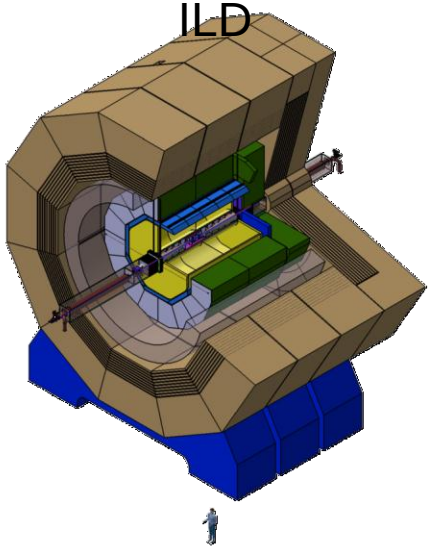
© Rammstein

ILC detectors

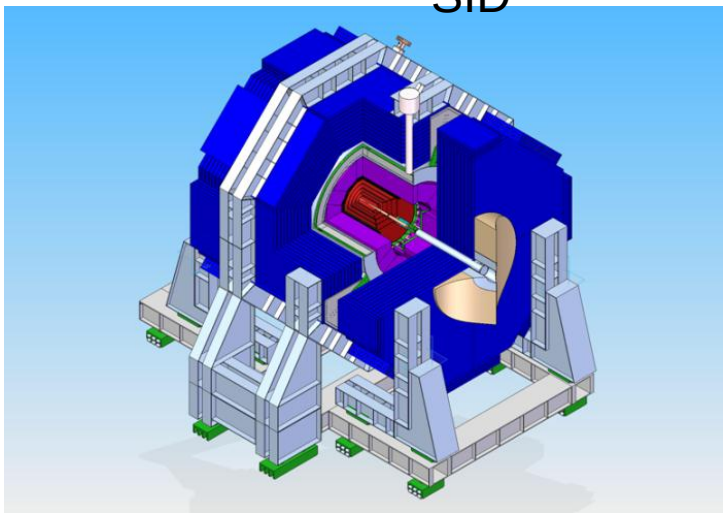
"Letters of Intent" March 2009, **DBD 2012**

Compact detectors, inside coil => power issues critical !

ILD



SID



Gaseous TPC main tracker

Mag. Field = 3.5 T

SiW ECAL

Analog HCAL

Si main tracker

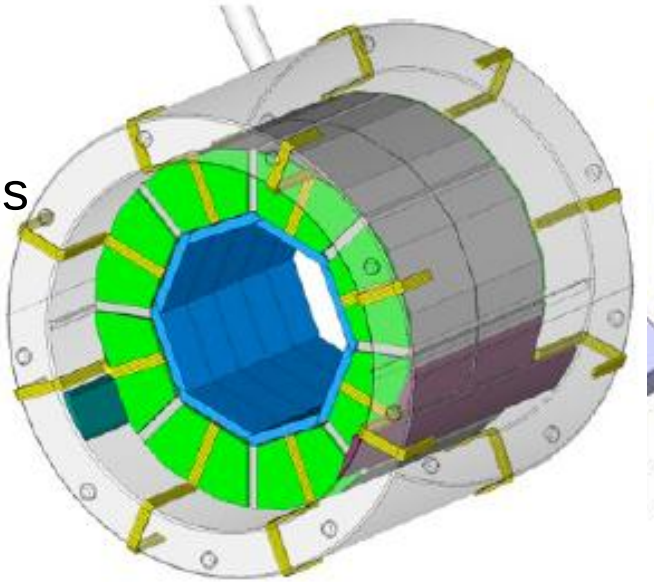
Mag. Field = 5 T

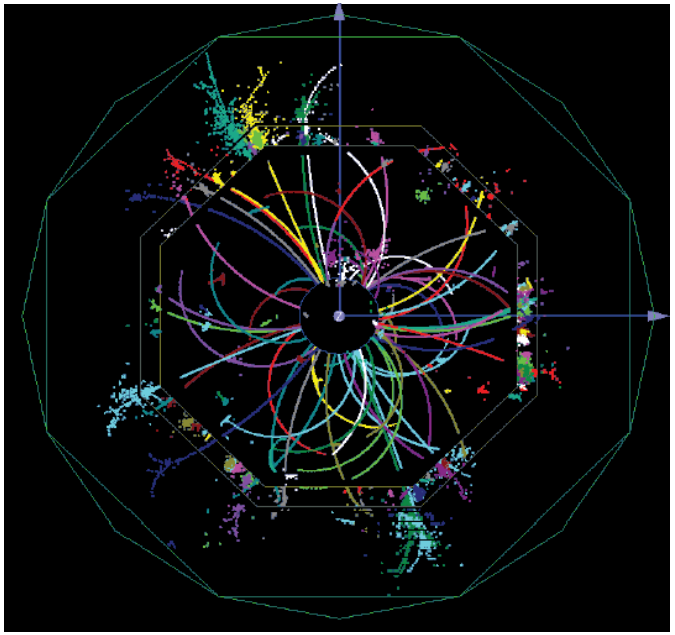
SiW ECAL

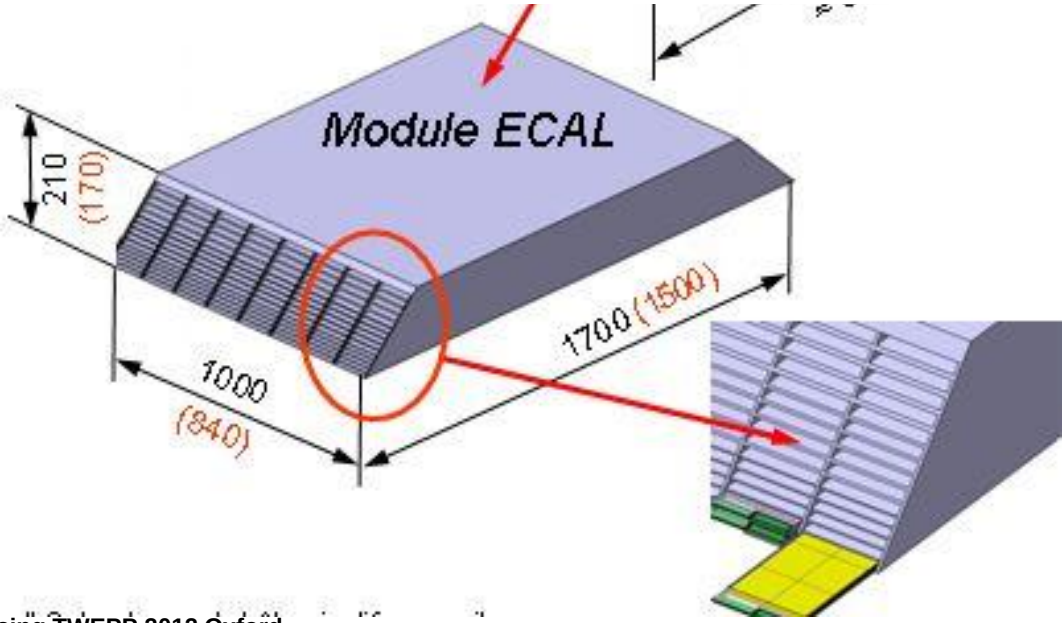
Digital HCAL

Example : SiW ECAL design

- Front-end ASICs embedded in detector
  - Very high level of integration
  - Auto-trigger, internal digitization, zero suppress
  - Ultra-low power : no cooling
- All communications via edge
  - 4,000 ch/slab, minimal room, access, power
  - small data volume (~ few 100 kbyte/s/slab)

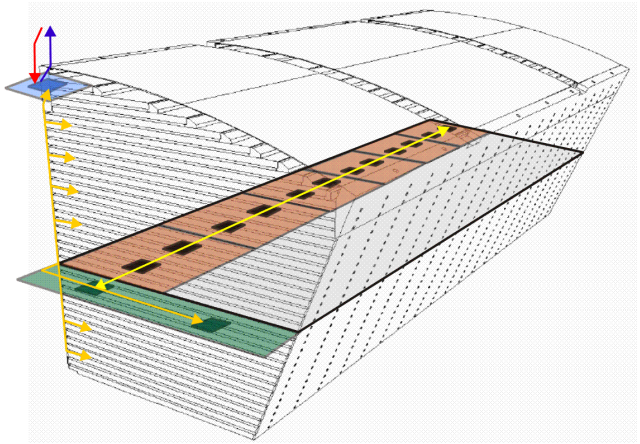






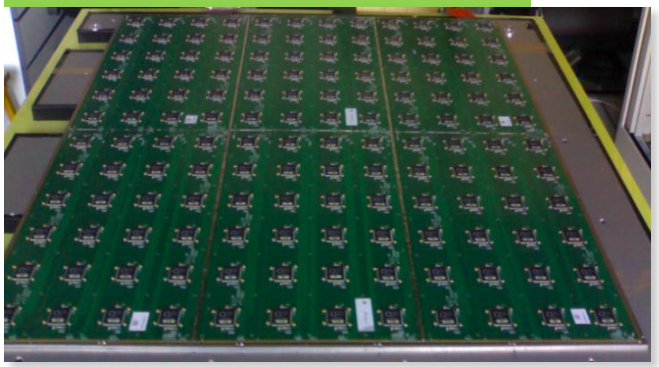
calorimeter technological prototypes

AHCAL: **8 M channels**

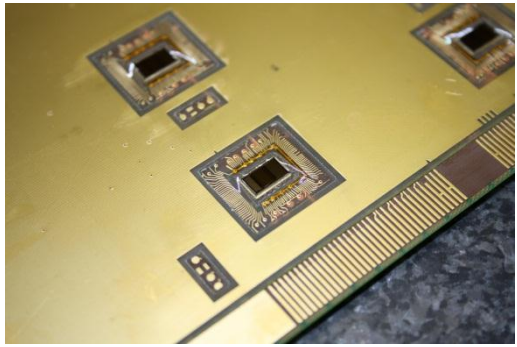


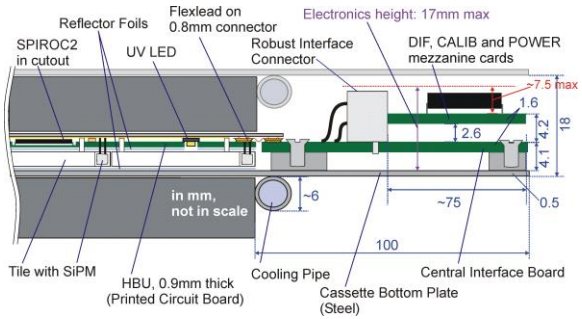
DHCAL: **50M channels**

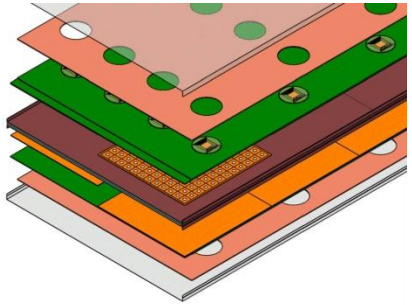
1 m2:144 chips x 64 ch ~ 10 000 Ch.
A few external components

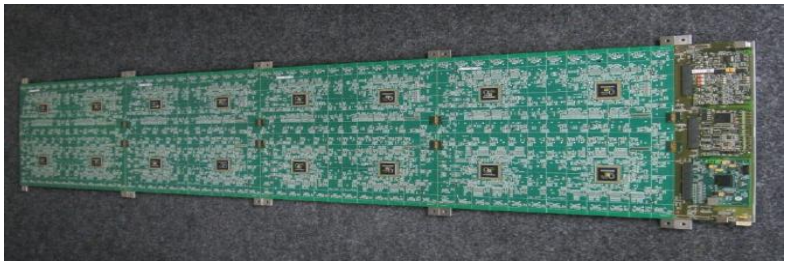


ECAL: **100 M channels**
Chips directly bonded
0 external components









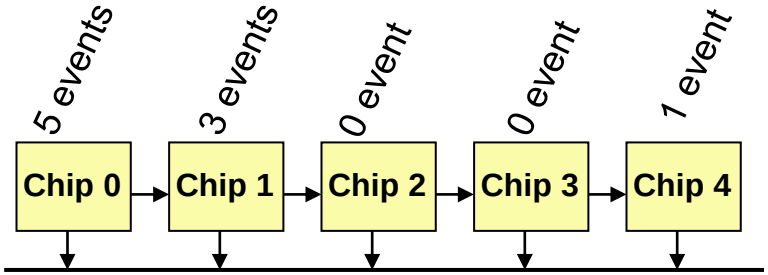
Power issues

- Before power pulsing, minimize power !!
  - Do not overdesign (noise, linearity, speed…)
  - Minimize data transfer (zero suppress)
  - Minimize digital currents : C dV/dt
  - Very different from LHC habits (and old habits die hard…)
- Power pulsing gives an additionnal factor up to 200
  - Any permanent bias should be extremely small
  - Avoid floating nodes, especially on digital inputs…
- R&D on power pulsing started early in ILC community
  - All detectors assume it (vertex, TPC, calorimeters…)
  - Calorimeters put emphasis early on this issue in CALICE

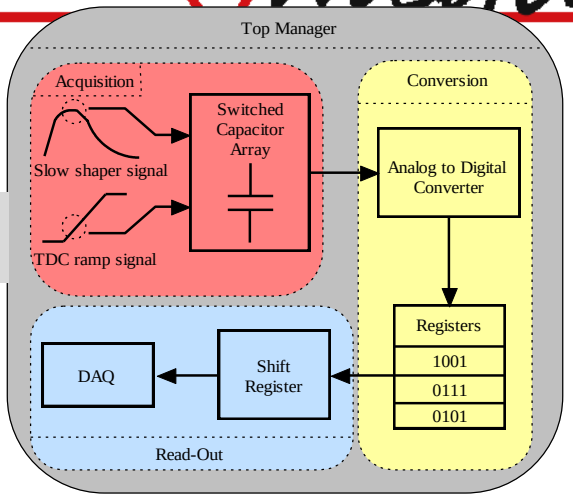
COMMON READOUT: TOKEN RING Mode

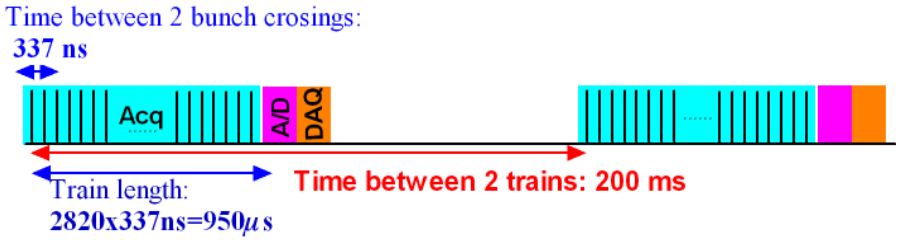
Readout architecture **common to all calorimeters** and **minimization of data lines & power**

- **Daisy chain** using token ring mode
- Open collector, low voltage signals
- Low capacitance lines

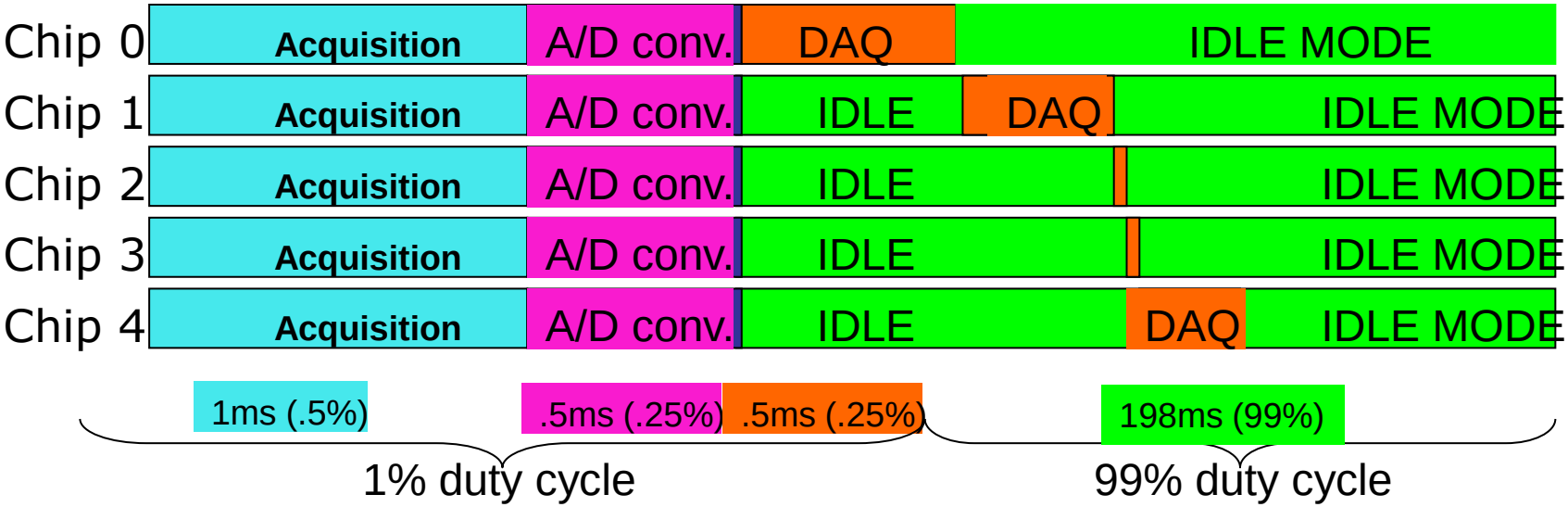


SCA in SK2 and Spiroc





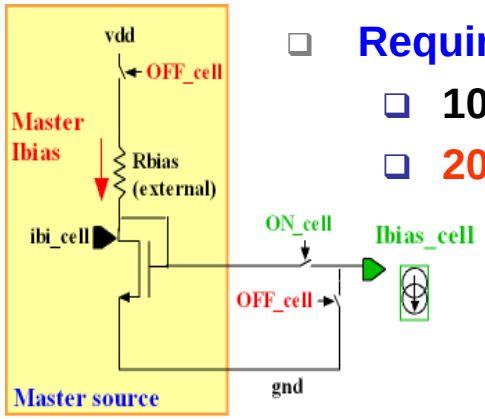
Data bus



Power pulsing issues

- ASIC level
  - Time to power on active parts
  - Reference voltages, DACs
  - Thermal issues
  - Stability issues
  - Accuracy issues
  - Mechanical issues : Lorentz force on bonding wires
- Board level
  - Power distribution and sequencing
  - Reliability issues
- System level : see talk by P. Goettlicher

POWER PULSING: HARDROC example

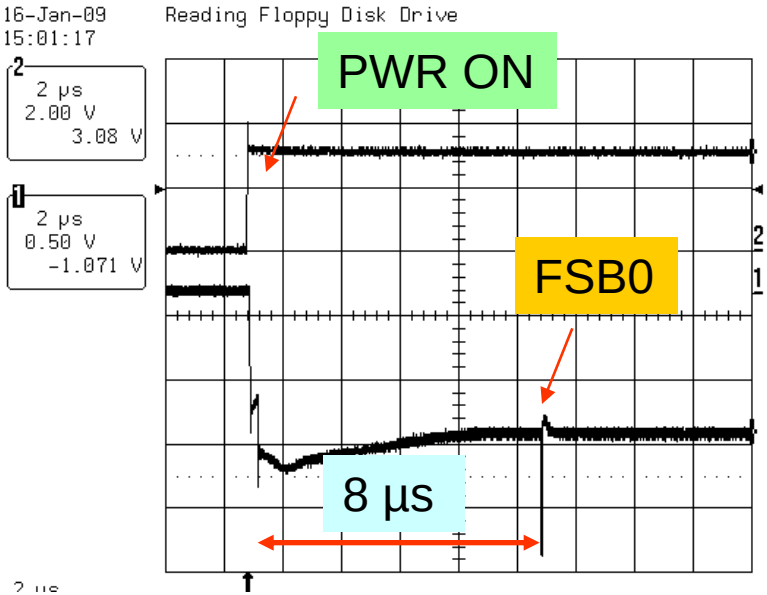


- **Requirement:**
  - **10 µW/ch with 0.5% duty cycle**
  - **200 µA for the entire chip (64 channels)**
- **Power pulsing:**
  - Bandgap + ref Voltages + master I: switched ON/OFF
  - **Shut down bias currents with vdd always ON**
- **HR2 power consumption measurement:**
  - 29 mA x 3.3V ≈ 100 mW => **1.5 mW/ch**
  - **7.5 µW/ch with 0.5% duty cycle**

HR2	ON
Vdd_pa	5.5 mA
Vdd_fsbx3	12.3 mA
Vdd_d0,1,2	7.3 mA
Vdd_bandgap	1.2 mA
Vdd_dac	0.84 mA
Vddd	0.67 mA
vddd2	0.4mA (=0 if 40MHz OFF)
Total (noPP)	29 mA
Total with 0.5% PP	145 µA

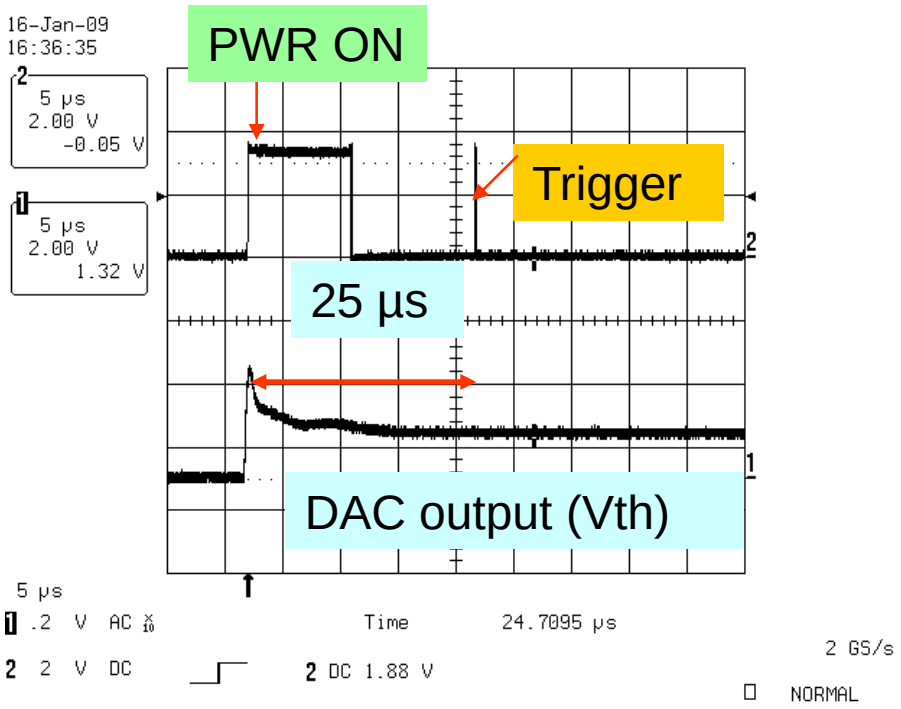
Pwr_on_a alone	26.5mA
Pwr_on_dac	1.0 mA
Pwr_on_d	1.0 mA
ALL OFF	<4µA

POWER PULSING: « AWAKE TIME »



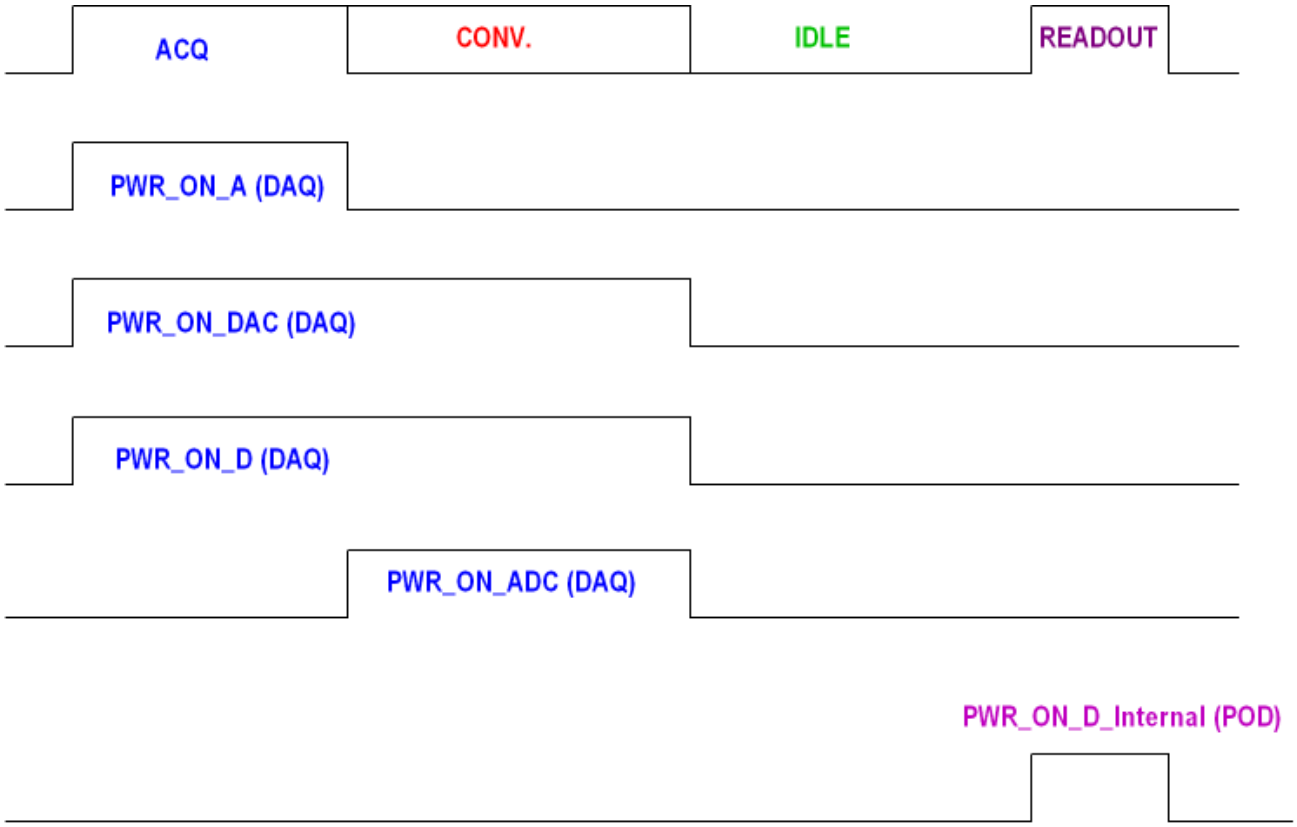
- All decoupling capacitors removed on bias voltages
- PWR ON: ILC like (1ms,199ms)
- PP of the analog part:
  - Input signal synchronised on PWR ON
  - Awake time= 8 µs

- **Power pulsing of the 10 bit-DAC:**
  - **25 µs (slew rate limited)**

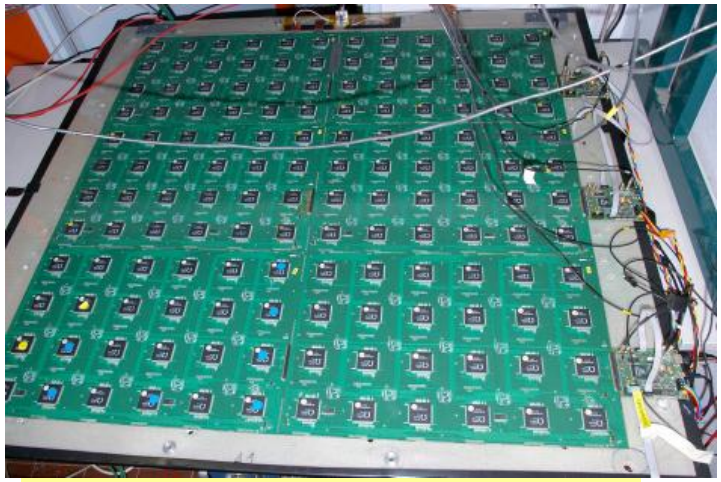


Power pulsing lines timing

- **4 Power pulsing lines handled by the DAQ** : analog, conversion, dac, digital
  - Most of the power in pwr_on analog
- Each stage can be forced **on/off by slow control**



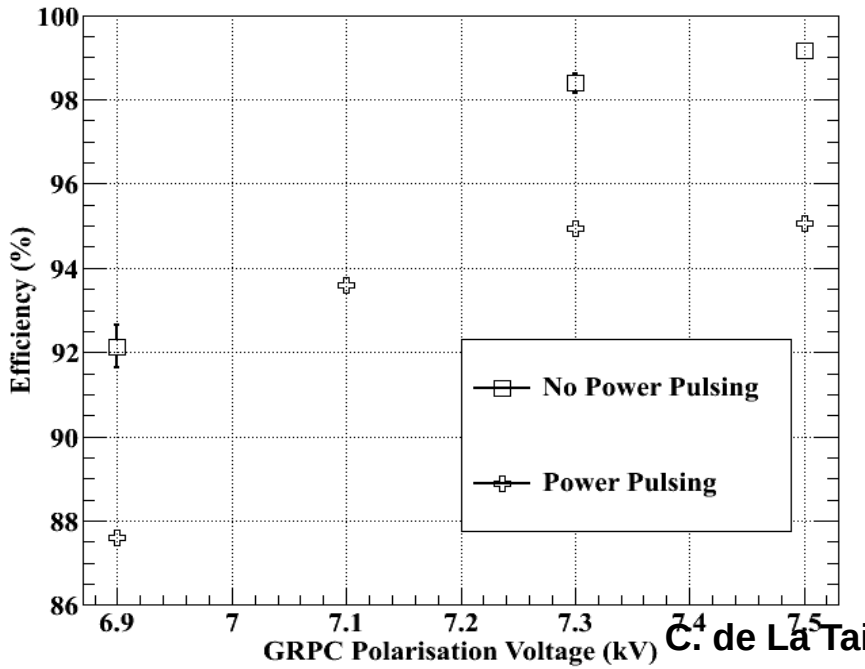
SDHCAL: POWER PULSING in TESTBEAM



1 m² PADs 1x1 cm²

1 m² GRPC detector in test beam Semi-digital electronics readout system validated in beam conditions (daisy chain, stability, efficiency, no external component)

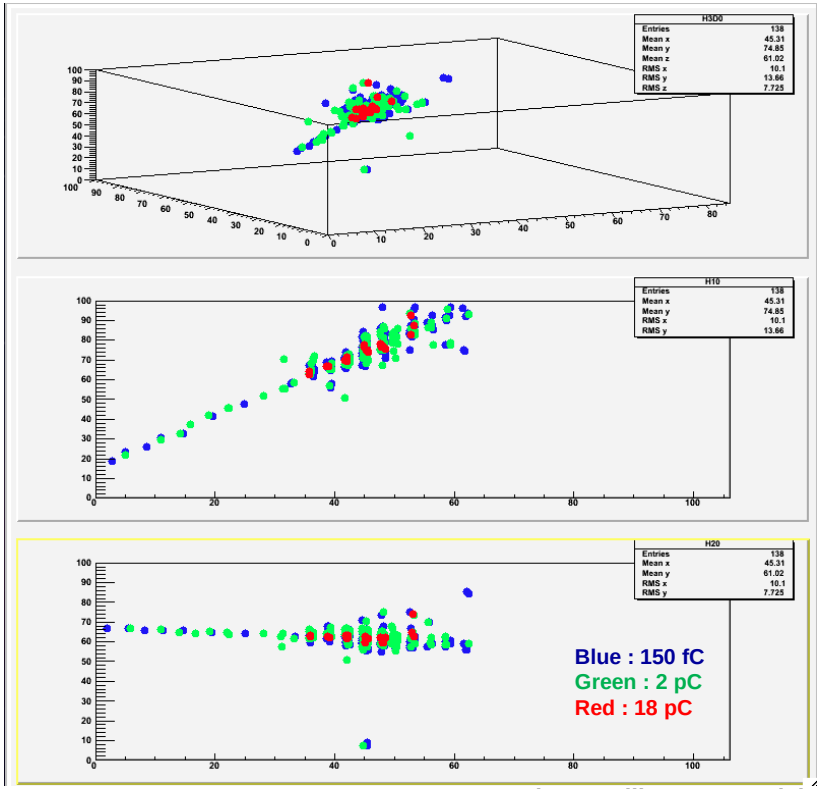
Power pulsing was successfully tested on a 24-ASIC electronic board in a 3-Tesla B field in June 2011 (SPS-H2)



RPC detector (SDHCAL-ILC)
Full power pulsing

SDHCAL technological proto with 40 layers (**5760 HR2 chips**) built in 2010-2011. and under tesbeam at CERN May 2012

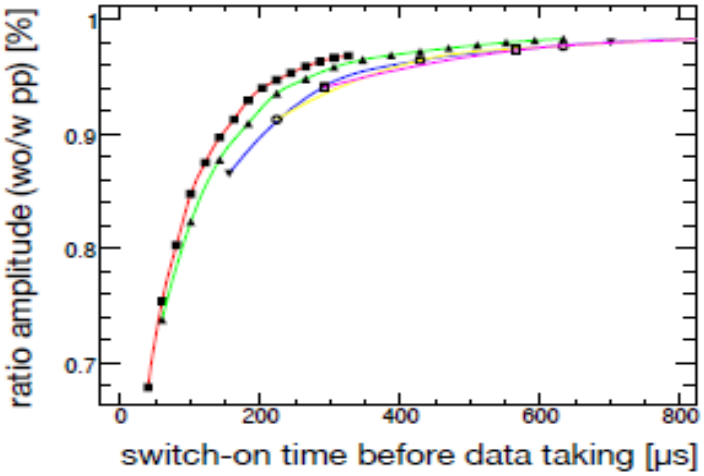
@IPN Lyon

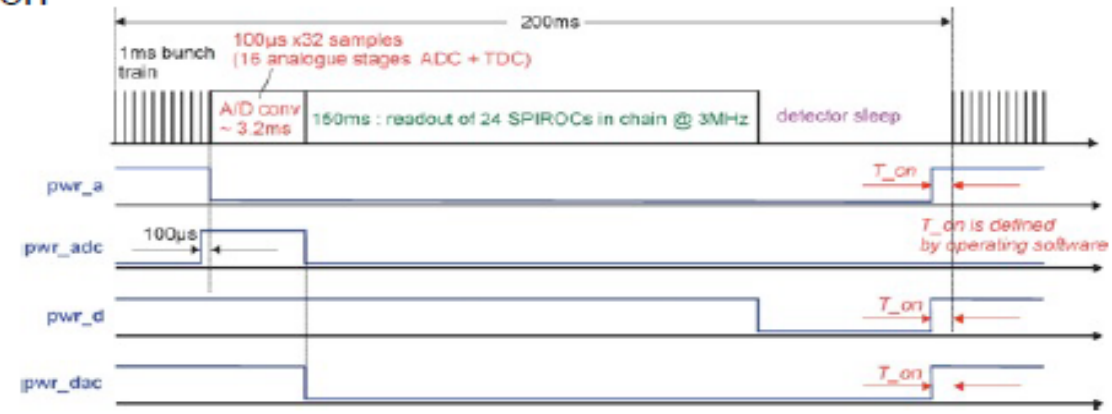


Power pulsing

- Necessary to avoid an extra cooling system
  → heat production limited to 40 µW/ch
- Electronics switched off between the bunch trains
- **Comparison w/wo power pulsing (pp):** With pp: reduced amplitude, depending on switch-on time (250 µs for 95% efficiency) (right slide)
- **Power consumption:** ~190 µW/ch (SPIROC2b + HBU2)

Improvement in SPIROC2c has to be checked!





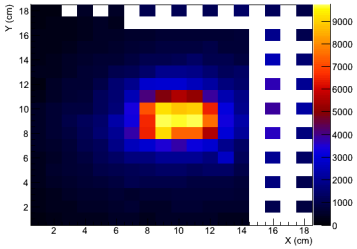
ECAL Test Beam 2012

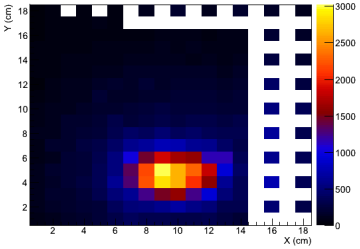
DESY - April 2012

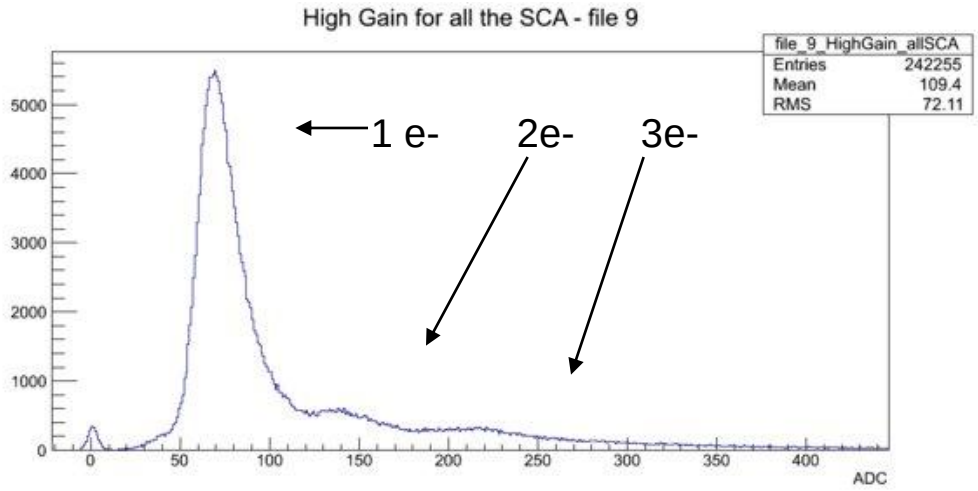
e- (3 → 5 GeV)

wafer 9x9 cm^2, 324 pixels **5x5 mm^2**

(lateral granularity = 4 × better than physics prototype)







Electron sources:

- Beam
- delta rays
- Bremsstrahlung + gamma conversion (2e-)+ Compton

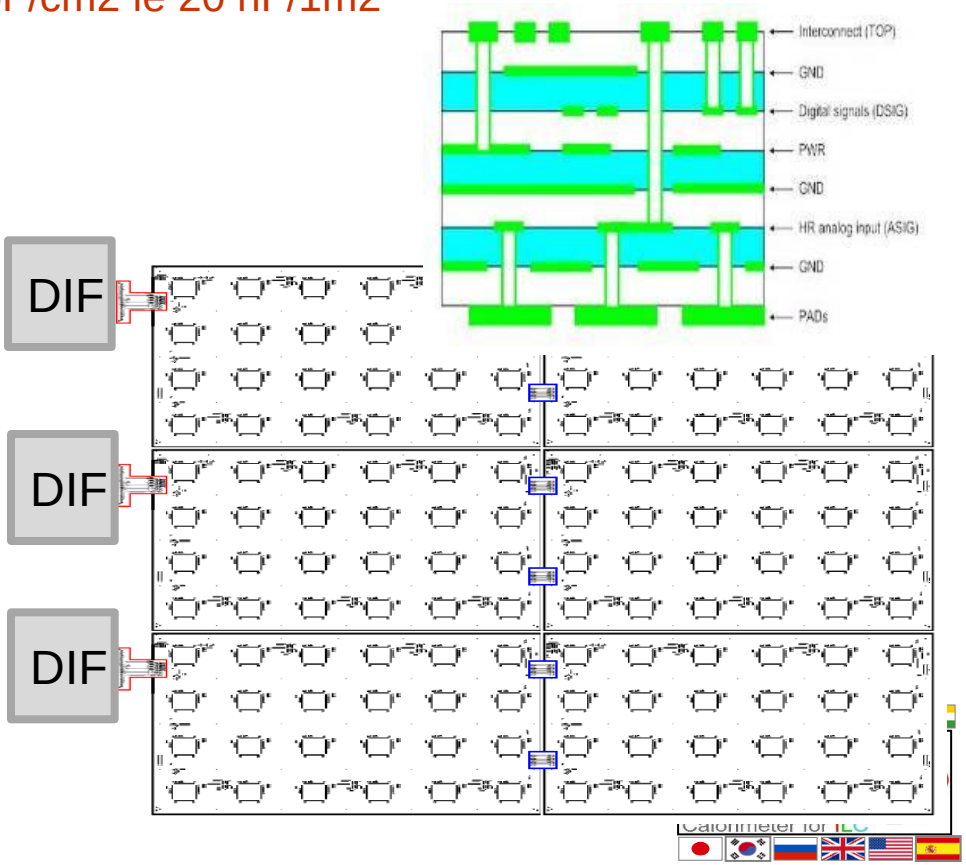
Conclusion

- Power pulsing now tested on large scale
  - 1 m3 DHCAL, 300 000 channels
  - Good performance at ~10% duty cycle
  - Now need to go to 0.5% !
- Tests also performed in 3T B field
  - 50 Hz operation for several days
- Need to go in details with ECAL and AHCAL
- And also other detectors…
  - Priority given to performance assessment

POWER and DECOUPLING

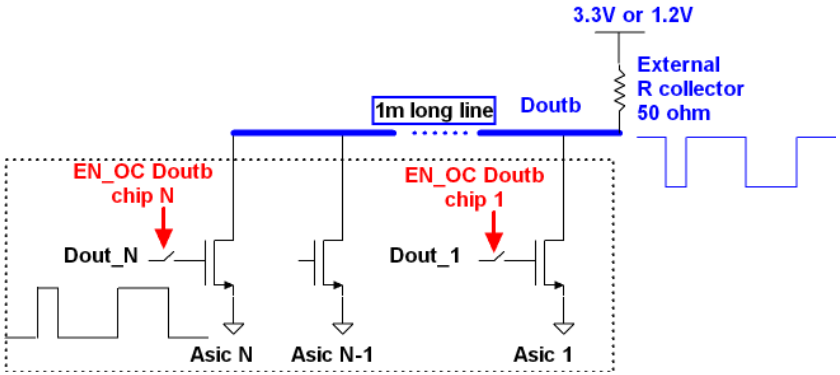
- DHCAL: 7.5 µW/ch => 2.5 µA/ch => <>=25 mA/m2 (10 000 channels/m2)
- 2AA battery: 1500 mAh => 60 hours
- I peak=5 A during 1 ms acquisition => need of energy storage, ΔV=1V (regulators) => C=Idt/dV =5 mF, on the DIF.
- DHCAL/AHCAL 100 nF (for HF decoupling) possible near the chip, ECAL: 0 external components => decoupling C at the edges (DIF board)
- Decoupling vdd/gnd on PCB= About 20 pF/cm2 ie 20 nF/1m2

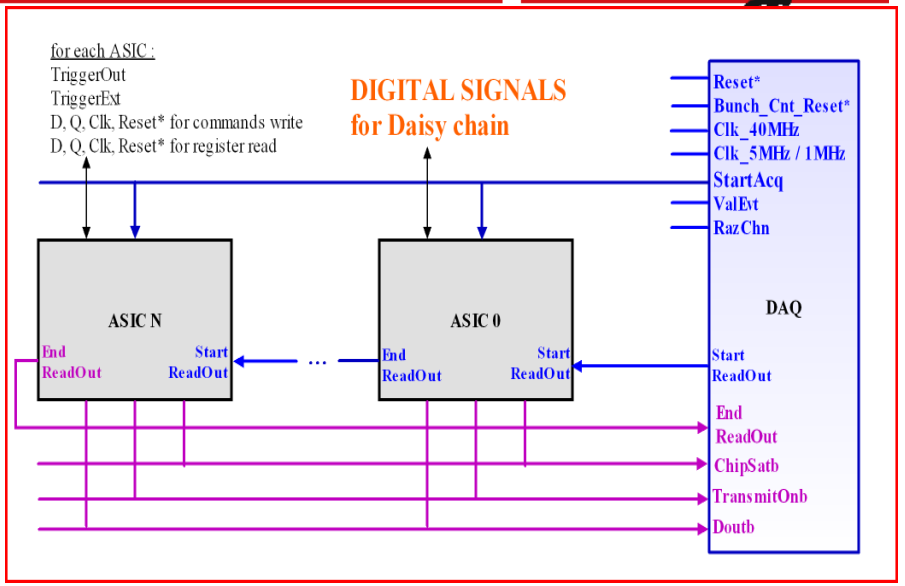
Ultra low power:
60h operation for 10 000 channels with a 2 AA battery



DAISY CHAIN: only 6 signals

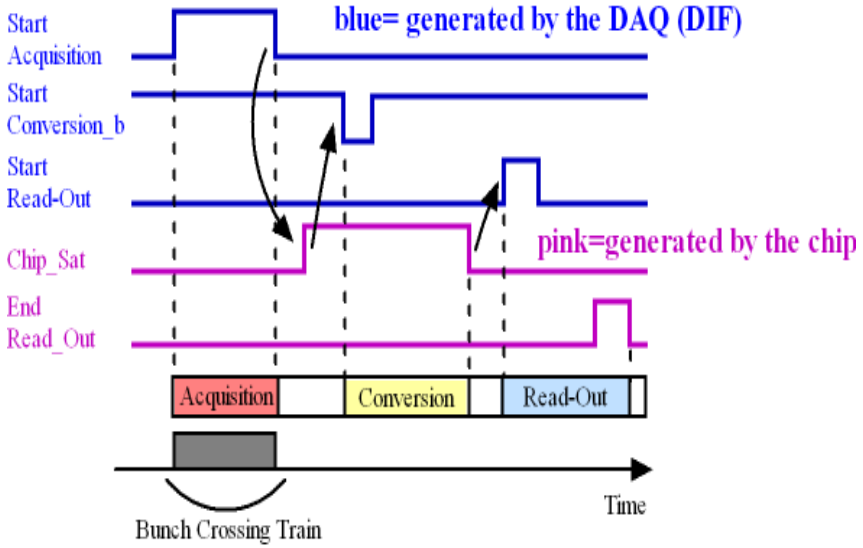
- **COMMON to all the ROC chips**
  - **StartAcq**
    - Start acquisition, generated by DAQ
  - **StartReadout:**
    - Generated by DAQ, start of the readout
  - **EndReadout**
    - Generated by chip, End of the readout
  - **ChipSat** (**O**pen **C**ollector signal):
    - Generated by chip, « 1 »: digital memory is full or acq finished
  - **Dout:** data out (OC signal)
  - **TransmitOn** (OC signal)
    - Generated by chip, Data out are transmitted
- Buffers integrated for OC signals





ILC

No conversion in Hardroc



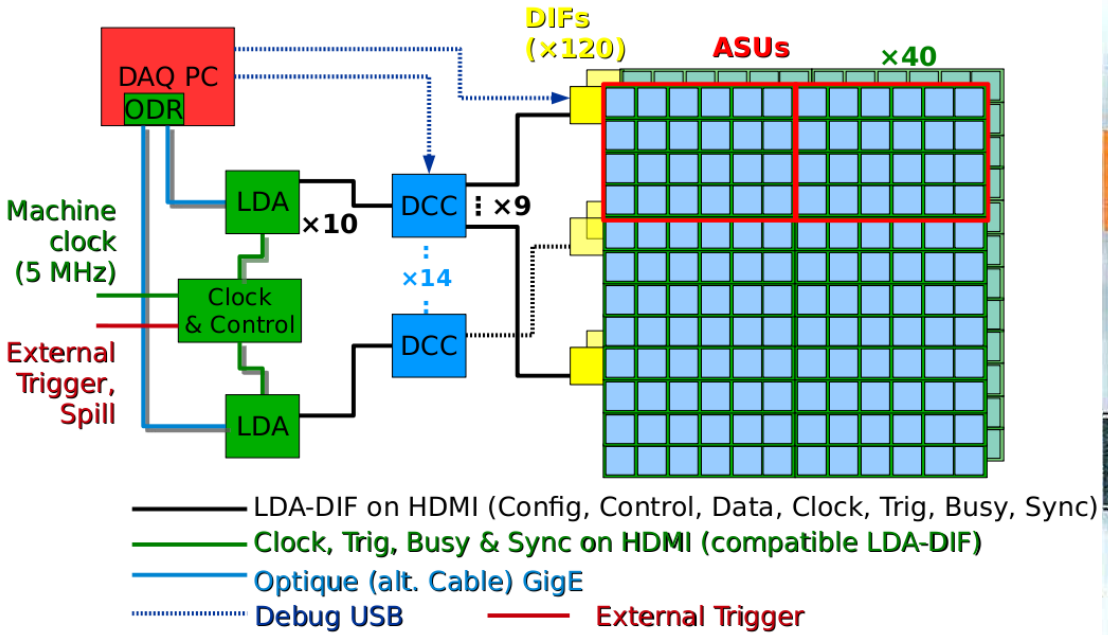
INTERFACE DAQ-ROC= DIF board

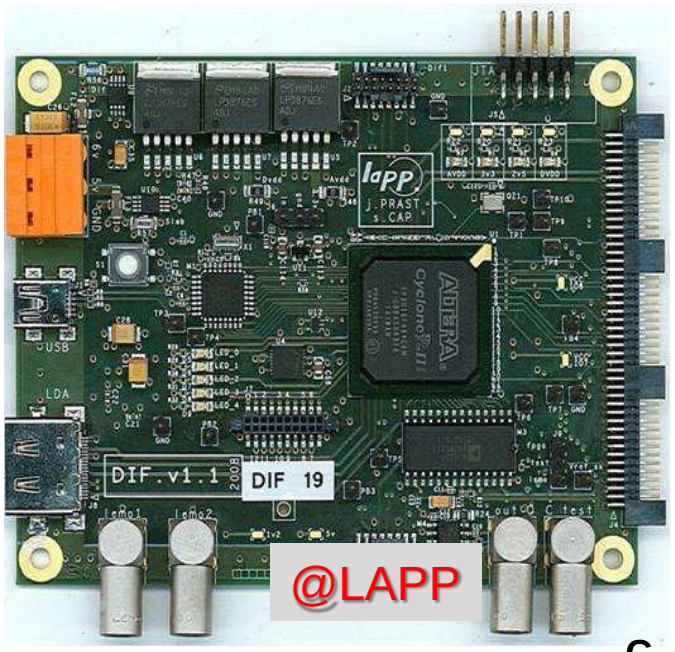
- Reception of the Slow Control parameters from a PC and transmission to the ASICs, launch acquisition, perform analog/digital readout and send all the data received from ASICs to a PC.

- Communication
  - with other DIFs
  - with DAQ either by USB or by HDMI

- The DIF should be able to handle more than 100 ASICs theoretically. The max which has been tested is 48

- **Regulators + Decoupling capacitors located on the DIF**

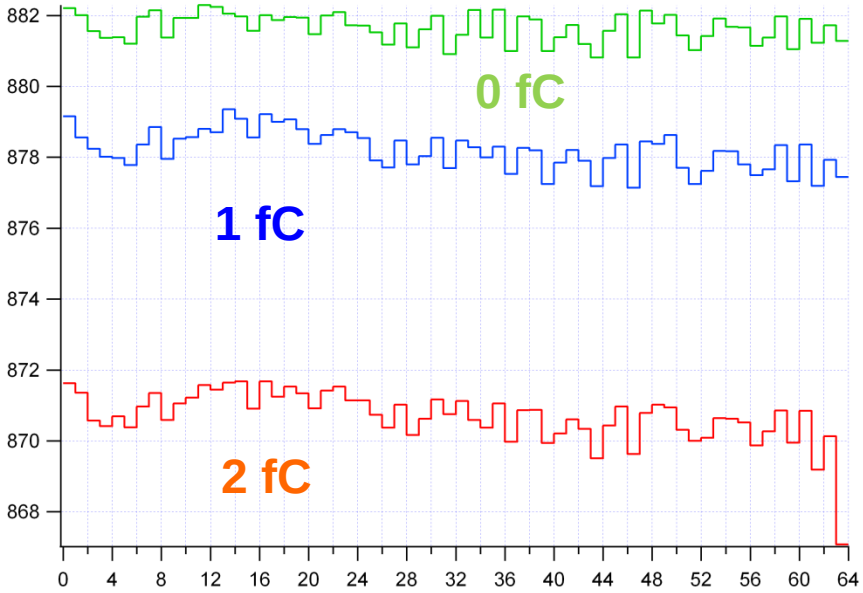




Variant: MICROROC

MICROROC: 64 channels for µMegas (DHCAL ILC)

- Very similar to HARDROC except for the input preamp (collaboration with LAPP Annecy) and shapers (100-150 ns)
- Noise: **0.2fC Cd=80 pF => Auto trigger on 1fC** up to 500fC
- Pulsed power: **10 µW/ch** (0.5 % duty cycle)
- **HV sparks protection**
- 1 m2 in TB in August and October 2011. Very good performance of the electronics and detector (Threshold set to 1fC).
- 2012: 4 m2 in TB



@LAPP Annecy

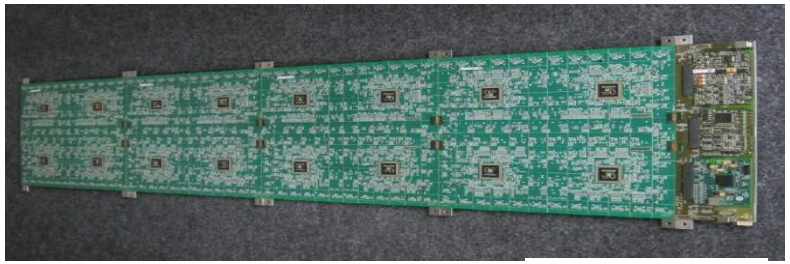
1m2 equipped with 144 MICROROC

SPIROC for SiPM

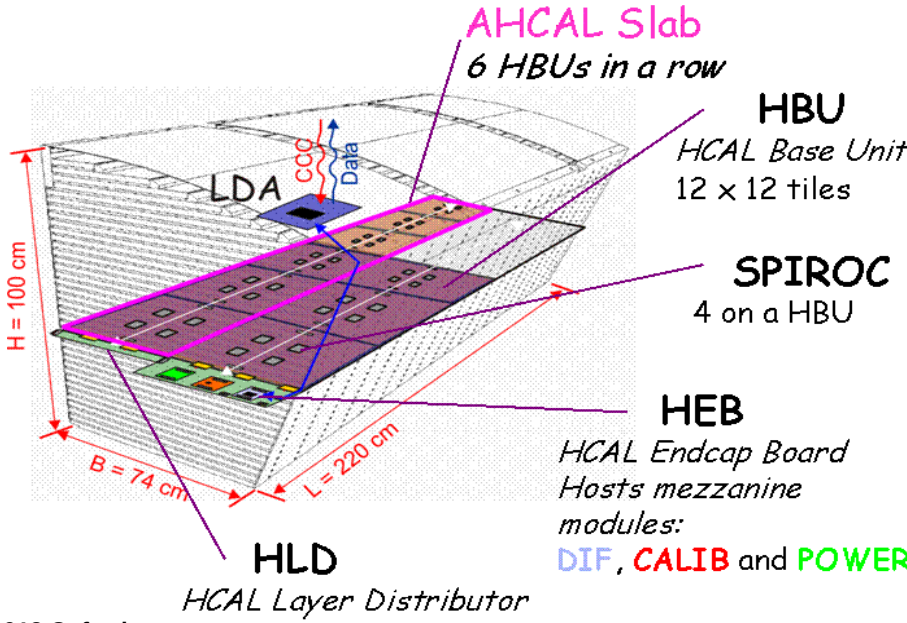
- SPIROC : Silicon Photomultiplier Integrated Readout Chip to read out the analog hadronic calorimeter for CALICE (ILC)
- Large detector with 8 millions channels= >Chip embedded in detector :
- **36-Channel ASIC**
- **Internal input 8-bit DAC** (0-5V) for individual SiPM gain adjustment
- **Energy measurement : 14 bits, 1 pe to 2000 pe**
  - pe/noise ratio : ~11
- **Auto-trigger on MIP or on single photo-electron**
  - Auto-Trigger on 1/3 pe (50fC)
- **Time measurement :**
  - 12-bit Bunch Crossing ID (coarse time)
  - 12-bit step~1 ns TDC->TAC (fine time)
  - Analog memory for time and charge measurement : depth = 16
  - Low consumption : ~25 µW per channel (in power pulsing mode)
  - 4kbytes internal memory and daisy chain readout

4 **new HBUs** in DESY lab

→ 70 channels equipped with scintillator tiles, LEDs, SiPM readout, 4 ASICs

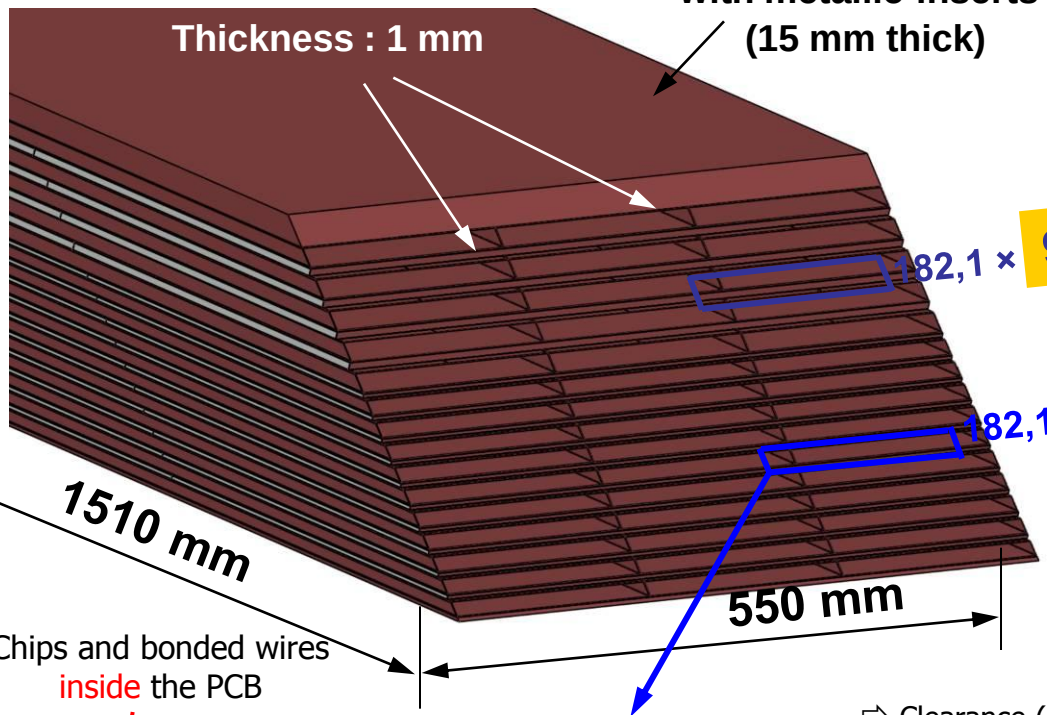


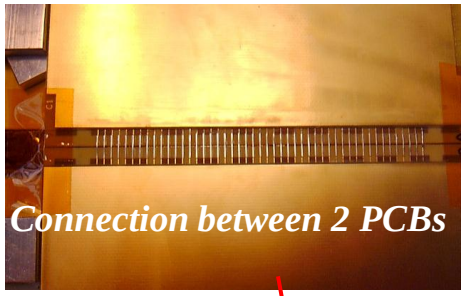
(0.36m)² Tiles + SiPM + SPIROC (144ch)

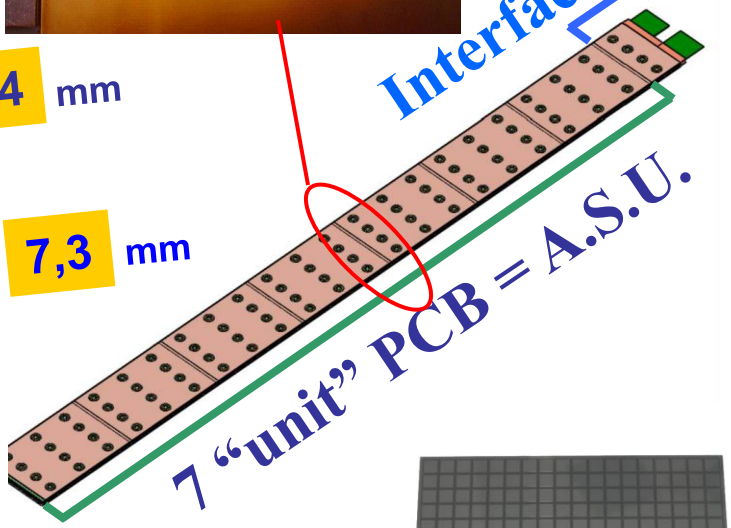


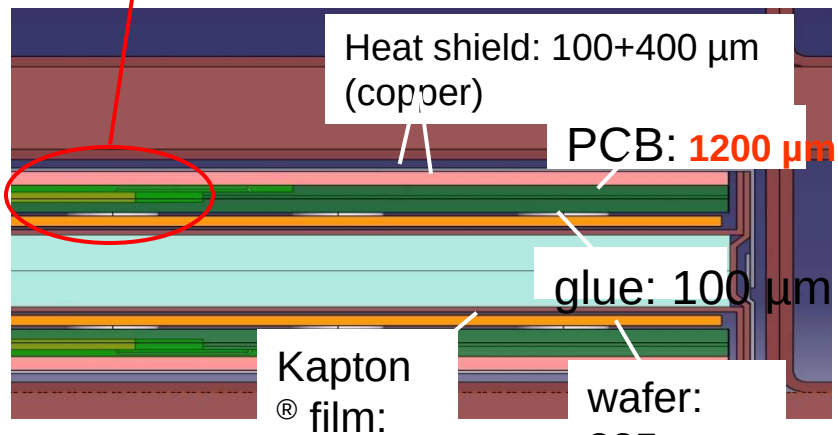
E-CAL DESIGN

Composite Part
with metallic inserts
(15 mm thick)

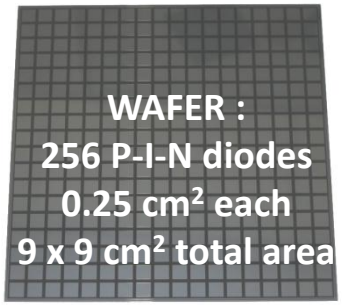








- ⇨ Clearance (slab integration) : 500 µm
- ⇨ Heat shield : **400 µm ?** →
- ⇨ PCB : **1200 µm ?** → design possibilities
- ⇨ Thickness of glue : 100 µm
- ⇨ Thickness of wafer : 325 µm
- ⇨ Kapton® film HV : **100 µm ?** → tests
- ⇨ Thickness of W : 2100/4200 µm (± 80 µm)



Courtesy :
Marc Anduze - LLR