A CMOS Pixel Sensor with 4-bit Column-Level ADCs for the ILD Vertex Detector

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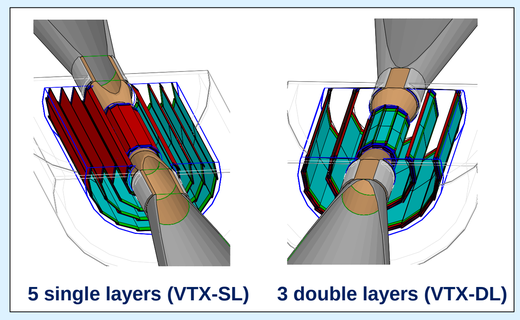
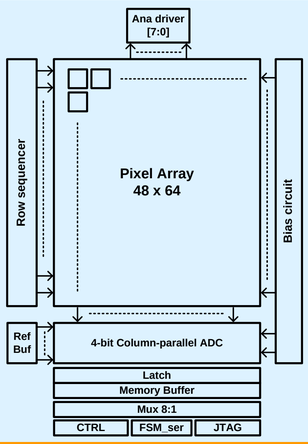
ABSTRACT A 48 × 64 pixels prototype CMOS Pixel Sensor (CPS) integrated with 4-bit column-level, self triggered ADCs for the ILD Vertex Detector (VTX) outer layers was developed and fabricated in a 0.35 µm CMOS process with a pixel pitch of 35 µm. The pixel concept combines in-pixel amplification with a correlated double sampling (CDS) operation. The ADCs accommodating the pixel read out in a rolling shutter mode complete the conversion by performing a multi-bit/step approximation. The design was optimized for power saving at sampling frequency.

INTRODUCTION

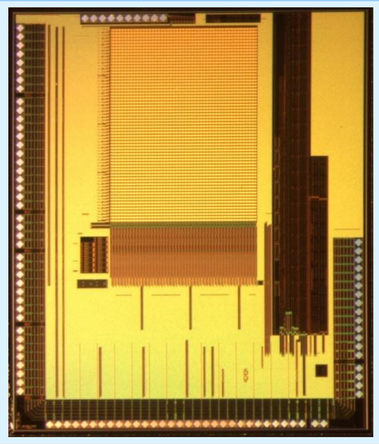
The ILD vertex detector (VTX) has two options. One of them (VTX-SL) features 5 equidistant single layers, while an alternative option (VTX-DL) features 3 double layers. Sensors equipping the innermost layer in both geometries should exhibit a single point resolution better than 3 µm associated to a very short integration time because of the beamstrahlung background. This requirement motivates an R&D effort concentrating on high read-out speed design. The sensors foreseen for the outer layers have less constrains in term of spatial resolution and read-out speed. A single point resolution of 3-4 µm combined with an integration time shorter than 100 µs are expected to constitute a valuable trade-off. In this case, the design effort focuses on minimizing the power consumption. A larger pixel pitch of 35 µm combined with a 4-bit ADC is proposed, therefore reducing the power consumption and keeping necessary spatial resolution. This work describes the design of prototype sensor (called MIMOSA 31), which is the first CMOS pixel sensor integrating column-level ADCs for the ILD-VTX outer layers.



MIMOSA 31



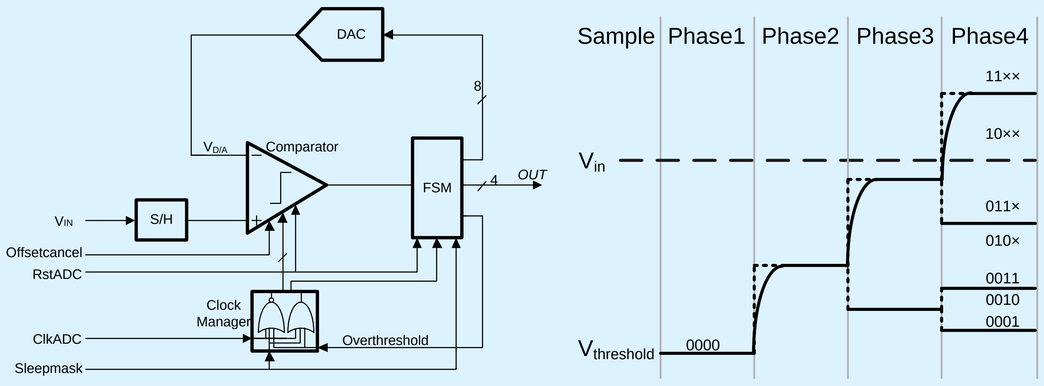
- The architecture includes a pixel array of 48 columns of 64 pixels, column-level ADCs and peripheral digital read-out micro-circuit
- The pixels are read out in row by row rolling shutter mode
- Each pixel combines in-pixel amplification with a correlated double sampling operation, which has been well used in previous sensors
  - MIMOSA 26 designed for EUDET beam telescope
  - ULTIMATE equipping the STAR-PXL sub-system
- The digital read out is implemented with 8 to 1 multiplexer, serializing the outputs of the ADCs
- The setting parameters of the sensor are remotely programmable through the JTAG circuits
- The design efforts are focused on the column-level ADCs



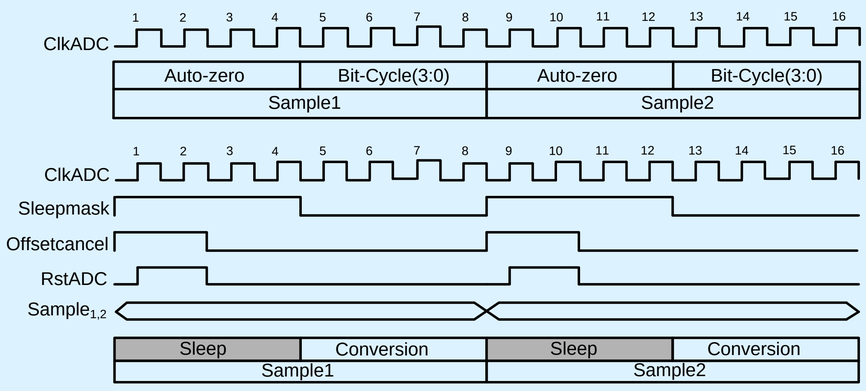
Column-Level ADC

ADC Architecture

- This ADC is based on a successive approximation register architecture
- This architecture requires 4 cycles to complete one conversion
- Complete the conversion by performing a multi-bit/step approximation
  - A maximum of 4 bits for signals of small magnitude to only 2bits for large signals

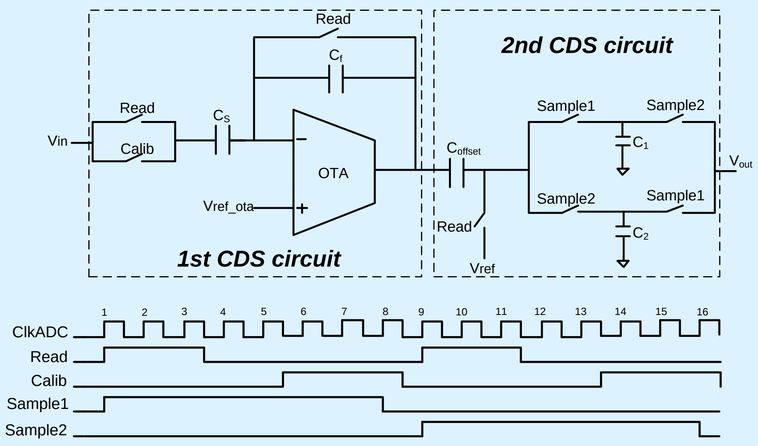


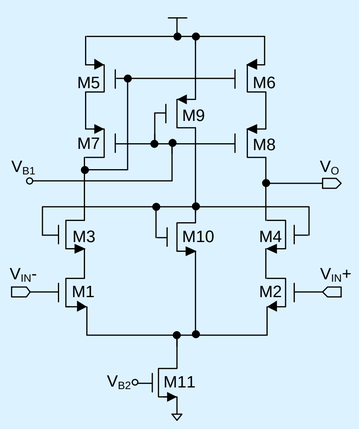
- The auto-zeroing and sampling operations are implemented asynchronously
- Power dissipation is scaled by clock-gating control between sleep-active conversions



S/H Circuit

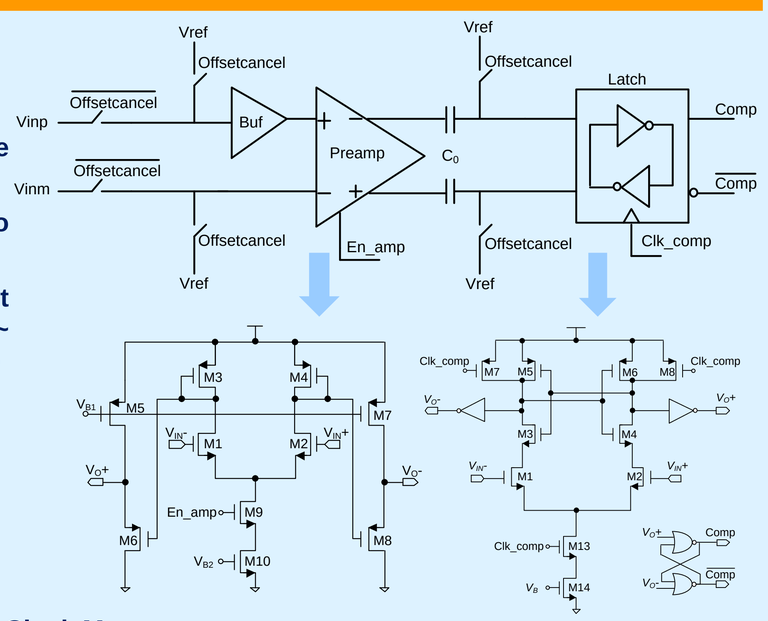
- Pipelined stage to achieve high conversion speed
- Dual CDS architecture to reduce the column offset
- Wide swing OTA

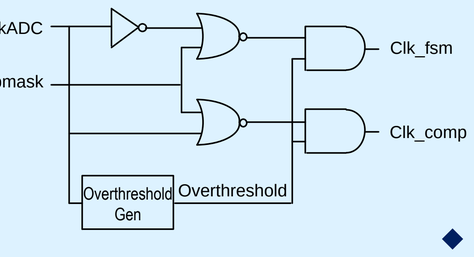


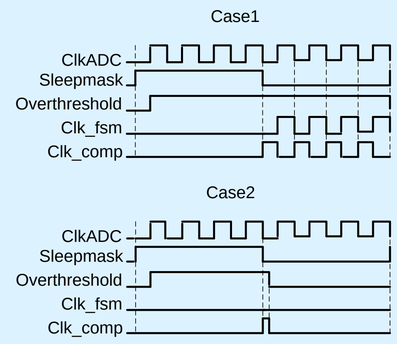


Comparator

- Output Offset Storage (OOS) stage
- The buffer is used to improve the drive capability of the input
- The preamplifier is enabled by M9 to turn off the current when appropriate
- The dynamic latch uses a current source M14 to decrease the offset (~ 2 mV in post Monte-Carlo simulation)





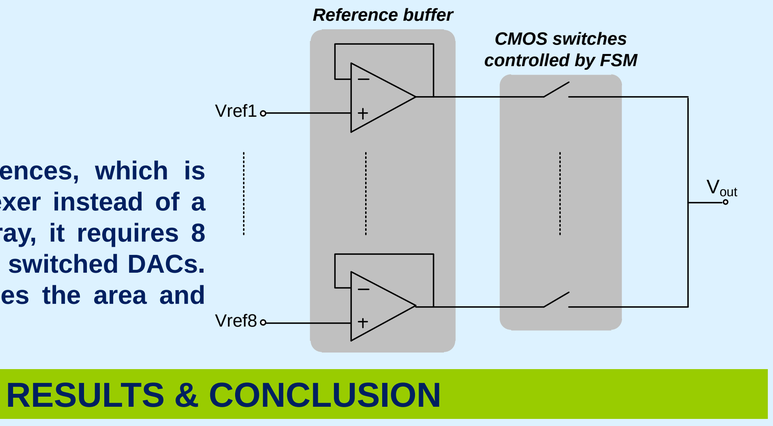


Clock Manager

- Clock-gate the dynamic latch and digital state machine (*Clk_comp* and *Clk_fsm*) during auto-zeroing
- *Overthreshold* signal is used to power-gate during bit-cycling. If the first comparison result is high, the *Overthreshold* keeps high. Otherwise, it goes low and sleeps the comparator and digital state machine until the next conversion

DAC

- The DAC only generates 8 references, which is implemented by a switch multiplexer instead of a capacitor network. For a pixel array, it requires 8 reference buffers to drive the total switched DACs. This approach significantly reduces the area and dynamic power consumption.



SIMULATION RESULTS & CONCLUSION

Technology	0.35 µm 2P 4M CMOS
Resolution	4/3/2
Active Area	35 × 545 µm²
Input Range	16 mV (single-ended)
Least Significant Bit (LSB) Voltage	1 mV
Sampling Rate	6.25 MS/s (160 ns/conversion)
Inactive Power (without hit)	486 µW @ 3V
Active Power (with hit)	714 µW @ 3V

The test of chip is being prepared and the preliminary test results will be shown. This is the first CMOS pixel sensor integrating column-level ADCs for the ILD-VTX outer layers. The prototype sensor was designed with specifications of the full scale sensor, and therefore can be easily extended in the future.

REFERENCES

[1] M. Winter et al., "Development of CMOS pixel sensors fully adapted to the ILD vertex detector requirements", 2011 International Workshop on Future Linear Colliders (LCWS'11), Spain, Sep. 2011.

[2] N. Verma and A. P. Chandrakasan, "An ultra low energy 12-bit rate-resolution scalable SAR ADC for wireless sensor nodes", IEEE J. Solid-State Circuit, vol. 42, no. 6, pp. 1196-1205, Jun. 2007.