Contribution ID: **13** Type: **Poster**

A CMOS Pixel Sensor with 4-bit Column-Level ADCs for the ILD Vertex Detector

Tuesday 18 September 2012 17:02 (1 minute)

A 48 × 64 pixels prototype CMOS pixel sensor integrated with 4-bit column-level, self triggered ADCs for the ILD vertex detector outer layers was developed and fabricated in a 0.35 μm CMOS process with a pixel pitch of 35 μm. The pixel concept combines in-pixel amplification with a correlated double sampling operation. The ADCs accommodating the pixel read out in a rolling shutter mode complete the conversion by performing a multi-bit/step approximation. The design was optimized for power saving at sampling frequency. Preliminary test results of the prototype will be shown.

Summary

The ILD vertex detector(VTX) has two options. One of them features 5 equidistant single layers, while the other features 3 double layers. Sensors equipping the innermost layer in both geometries should exhibit a single point resolution better than 3 μm associated to a very short integration time because of the beamstrahlung background. This requirement motivates an R&D effort concentrating on a high read-out speed design. The sensors foreseen for the outer layers have less constrains. A single point resolution of 3-4 μm combined with an integration time shorter than 100 μs are expected to constitute a valuable trade-off. In this case, the design effort focuses on minimizing the power consumption. A larger pixel pitch of 35 μm combined with a 4-bit ADC is proposed, therefore reducing the power consumption and keeping necessary spatial resolution. This work describes the design of a prototype sensor (MIMOSA31), which is the first CMOS pixel sensor integrating column-level ADCs for the ILD-VTX outer layers.

The architecture of MIMOSA31 includes a array of 48 columns of 64 pixels, column-level ADCs and digital readout microcircuit. The pixels are read out in row by row rolling shutter mode. Each pixel combines an amplification with a correlated double sampling, which was well used in previous sensors (MIMOSA26 designed for EUDET beam telescope and ULTIMATE equipping the STAR-PXL subsystem). The digital readout is implemented with 8 to 1 multiplexer, serializing the output of the ADCs. In this case, the design efforts are focused on the column-level ADCs.

The design of such column-level ADCs is constrained by several factors:

1. in order to accommodate pixel read out speed (160-200 ns/row), the ADCs require a high sampling rate;
2. due to the cooling system limitation, the consumption must be minimized, which should be less than 500 μW;
3. to decrease the dead zone of the sensor, the dimension should be minimized;
4. offset between different columns should be eliminated.

This ADC is based on a successive approximation register architecture. The conversion is completed by employing a multibit/step approximation. Accounting the fact that in the outer layers of ILD-VTX, the hit pixel density is in the order of a few per mille, the ADC is designed to operate in two modes in order to minimize the power consumption. If the pixel signal is higher than a threshold, the ADC works in active mode and does the conversion, otherwise, the ADC works in inactive mode and goes asleep until the next conversion.

The designed 4-bit ADC dissipates, at a 3 V supply and 160 ns/conversion, 486 μW in its inactive mode, which is by far the most frequent. This value rises to 714 μW in case of the active mode. Its footprint amounts to 35x545 μm2.

This paper will describe the details of the circuit implementation of the prototype sensor. The preliminary laboratory experimental results will be shown, complemented with an outlook on further design improvements.

Author: Mr ZHANG, LIANG (IPHC-UDS-IN2P3-CNRS)

Co-authors: Dr HU-GUO, CHRISTINE (IPHC-UDS-IN2P3-CNRS); Dr MOREL, FREDERIC (IPHC-UDS-IN2P-CNRS); Prof. HU, YANN (IPHC-UDS-IN2P3-CNRS)

Presenter: Dr MOREL, FREDERIC (IPHC-UDS-IN2P-CNRS)

Session Classification: POSTERS