The Design of 8-Gbps VCSEL Drivers for the ATLAS Liquid Argon Calorimeter Upgrade

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Abstract

We present the designs* of LOCld1 and LOCld4 VCSEL drivers in a commercial 0.25-μm Silicon-on-Sapphire (SoS) CMOS process for the ATLAS liquid argon calorimeter upgrade.

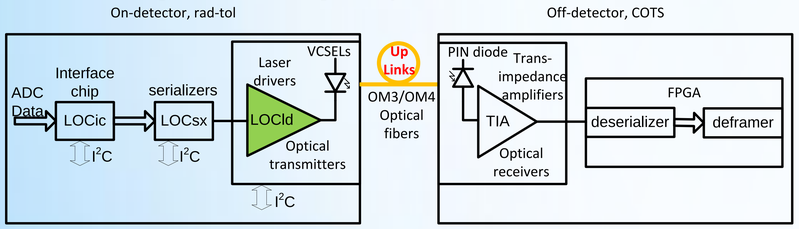
Active shunt peaking technique and multiple-stage amplification are used to achieve the data rate up to 8 Gbps.

LOCld1 is a single channel driver with a differential output, while LOCld4 has four channels with single-ended open-drain output. Both drivers have the adjustable modulation and peaking strength with bias current source embedded.

*The preliminary test results will be present in the proceeding.

Introduction

Vertical-Cavity Surface-Emitting Lasers (VCSEL) drivers, LOCld1 and LOCld4, belong to the LOC chip family, as shown below.



Block diagram of the optical link.

The LOC chip family is designed for the data transmission optical link in ATLAS liquid Argon calorimeter upgrade. LOCld1 and LOCld4 are to be implemented in the optical transmitter subassembly.

LOCld1 and LOCld4 receive low swing CML signals (minimum 2 mA) and drive high swing CML signals (up to 8 mA) at 8 Gbps. LOCld1 also provides a tunable bias current to the VCSEL. In the case of array connection, the bias current of LOCld4 is combined with the modulation current.

Goals and challenges

Prior irradiation tests indicate that commercial laser drivers fail in detector front-end electronics especially in a p-p collider environment.

Design goals:

- Data rate up to 8 Gbps.
- Minimum 2 mA low swing CML signals input.
- Up to 8 mA modulation current CML signals output.
- LOCld1 with 50 ohm differential output for TOSA based implementation.
- LOCld4 a 4-lane array driver with open drain connection to work with VCSEL arrays.

The transit frequency (f_T) of the IN device in the commercial 0.25-μm SoS CMOS process is 30-GHz. We used the RN devices in our design for its high gain. The f_T for the RN device is lower than that of the IN devices. We therefore deployed both multiple-stage amplification and active shunt peaking technique to achieve the target output strength at the target data rate.

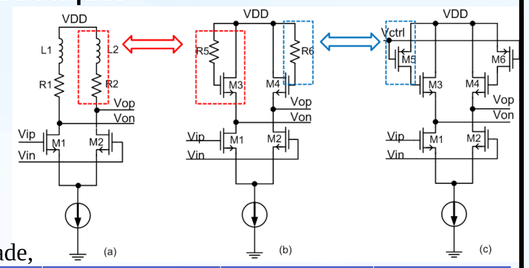
Techniques

1. Active shunt peaking.

Shunt peaking technique is widely used to extend the bandwidth.

Passive inductor peaking (a) has the best performance, but a on chip inductor takes a large die area.

Active shunt peaking (b) balances the performance and area. But the on chip resistor is not tunable after the chip is made, leaving the final performance to process variations.



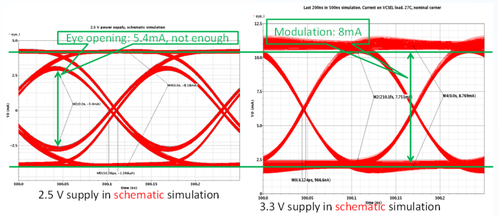
	Passive inductor peaking	Active shunt peaking	Used in our design
Performance	Best	Good	Good
Area	Very large	Small	Small
Adjustable	No	No	Yes

In our design, we use PMOS transistors (M5, M6) instead of resistors (R5, R8) (c). The PMOS transistors operate in the triode region and act as resistors. With an external voltage (Vctrl), we can adjust the equivalent resistance of M5 and M6 to modify consequently the peaking strength. In the meanwhile, an adjustable resistor-equivalent PMOS can reduce the effect on resistor in different process corners and different temperatures.

2. Multiple stages

We use multiple stages to enlarge the total GBW. The amplitude (voltage and current) is amplified in each pre-drive stage.

We have six pre-drive stages and one main drive stage in LOCld1 and five pre-drive stages and on main drive stage in LOCld4.



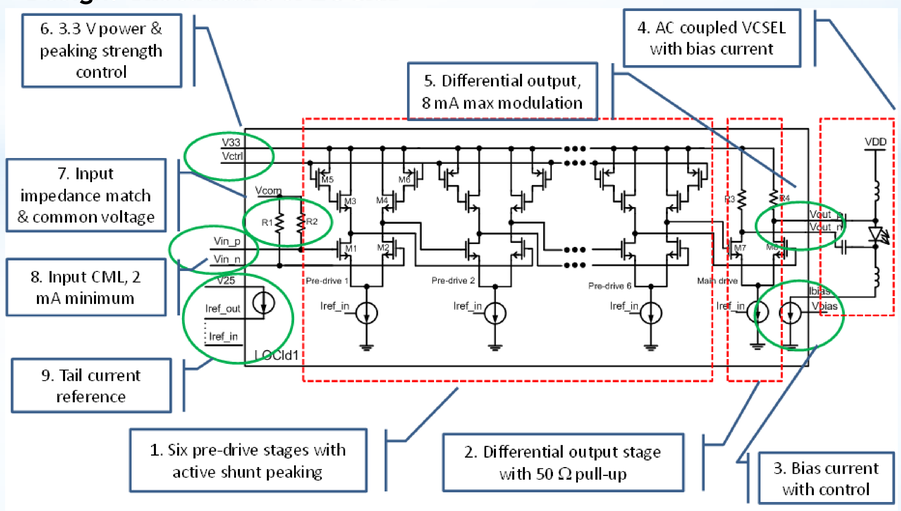
2.5 V supply in schematic simulation

3.3 V supply in schematic simulation

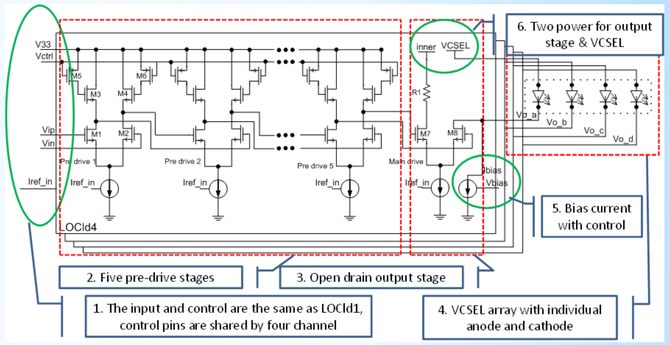
3. Higher level voltage supply

We pay the price of power to enlarge the bandwidth. The higher level of 3.3V is chosen for the voltage supply.

Design: The structure of LOCld1

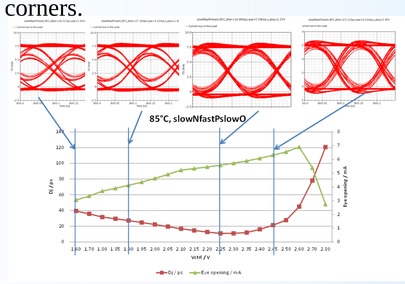


Design: The structure of LOCld4



Simulation Results

Thorough simulations are conducted on the active shunt peaking structure. We made sure the adjustable peaking can satisfy the performance in "all conditions", across temperature and process corners.



Worse case post-layout simulation is shown in the left with the deterministic jitter and the eye opening of the output current signal at different Vctrl. The target operation Vctrl is chosen to get the best eye diagram in all conditions.

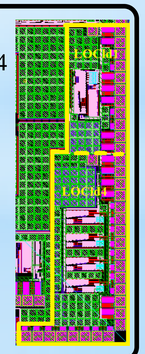
Summary

We designed two VCSEL drivers – LOCld1 & LOCld4 for the ATLAS liquid argon calorimeter upgrade.

Specification highlights:

- Data rate up to 8 Gbps.
- Low input swing -- Minimum 2 mA CML
- Up to 8 mA output swing -- CML modulation current
- Single-end interface to VCSEL array

The designs are submitted in a MWP run. The chip is to be delivered on Sep. 20th, 2012. We will report the preliminary test results in the proceedings.



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