

The Design of 8-Gbps VCSEL Drivers for the ATLAS Liquid Argon Calorimeter Upgrade

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We present the design and the preliminary test results of LOClD1 and LOClD4, the VCSEL drivers fabricated in a commercial 0.25- μm silicon-on-sapphire (SOS) CMOS process for the ATLAS liquid argon calorimeter upgrade. Because of the bandwidth limitation of the process, we use an active shunt peaking technique, multiple-stage amplification and a voltage higher than the nominal voltage to achieve the data rate up to 8 Gbps. LOClD1 is a single channel driver with a differential output, while LOClD4 has four channels with single-ended open-drain output. Drivers have the adjustable modulation and peaking strength.

Summary

The VCSEL drivers, LOClD1 and LOClD4, are designed for the ATLAS liquid argon calorimeter upgrade. The input signals of drivers can be CML signals with the swing as small as 2 mA on a 100-ohm input impedance. LOClD1 has one channel and differentially drives a VCSEL, and LOClD4 has four channels and drives a four-channel VCSEL array with single-end outputs. The drivers are designed to operate at up to 8-Gbps data rate with up to 8-mA modulation current.

For the radiation tolerance purpose, we use a commercial 0.25- μm silicon-on-sapphire (SOS) CMOS process. Due to the bandwidth limitation of the process, we have to employ bandwidth extending techniques. In a previous prototype, we have designed a CML line driver to 5 Gbps. In LOClD1 design, in order to achieve a higher bandwidth, we use an active shunt peaking technique in which active transistors are used to replace large-area passive on-chip inductors. We use pMOS's to replace resistors in the classic active shunt peaking structure. With the control of the pMOS gate voltage, we can overcome the variation of the on-chip resistor and adjust the peaking strength. Because of the small area of the active shunt peaking structure, we employ the active shunt peaking in every amplifier stages. Besides the active shunt peaking, we use six amplifier stages to extend the total gain bandwidth product and a 3.3 V power supply voltage instead of the 2.5 V nominal power supply voltage. With the efforts above and from the post-layout simulation results, LOClD1 can operate at 8 Gbps with an adjustable peaking strength. An adjustable bias current source for the VCSEL is embedded in LOClD1.

The differential output of LOClD1 requires extra AC coupling capacitors and low pass inductors to drive the VCSEL. It is impossible to use simple copies of LOClD1 to drive a VCSEL array for a high channel density purpose. To drive the high channel density VCSEL array, we design a four-channel prototype LOClD4 based on LOClD1. We modify the differential output stage into open drain mode and only use one branch as the output with bias current DC coupled inside of the chip. We reduce amplifier stages to meet the modulation current requirement. The bandwidth extending techniques in LOClD4 are the same as LOClD1. The peaking strength, modulation current and bias current are also adjustable.

In the post-layout simulation, LOClD1 has 4.12-ps deterministic jitter, 7.75-mA eye opening, and 194.7-mW power consumption when operates at 8 Gbps, 27 °C and the nominal process corner. LOClD4 has 2.05-ps deterministic jitter, 6.98-mA eye opening, and 131.4-mW power consumption per channel in the same condition.

LOClD1 and LOClD4 will be submitted on June 1st, 2012 and will be tested in September, 2012. We will present preliminary test results in the final presentation.

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