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A complete DCDC converter ASIC for LHC upgrades

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A new and complete DCDC converter ASIC prototype has been designed and manufactured in a commercial 0.35um CMOS technology. The circuit is aimed at applications in LHC upgrades, where it can function in the intense magnetic field and survive to the radiation environment of even the trackers. Rated for an input voltage up to 10V, it provides a selectable output voltage and embeds under-voltage, over-temperature and over-current protections as well a soft-start to prevent excessive inrush current at startup. The characteristics of the ASIC are described, and first electric and radiation tests are presented.

Summary

The use of DCDC converters on-detector is an attractive option for the distribution of low-voltage power in upgraded LHC electronic systems. In view of such application, we are pursuing the development of a radiation and magnetic-field tolerant step-down buck converter based on an ASIC. At TWEPP 2011, a first complete prototype ASIC in the selected 0.35um CMOS technology has been presented. Although the circuit was functional, a number of issues needing to be addressed before production readiness were observed. After an in-depth cycle of measurements, a redesign of the ASIC based on the lessons learnt started and led to a new prototype - named AMIS5 - sent to the manufacturer for fabrication in early February. The general specifications of the circuit remain unchanged: input voltage up to 10V, selectable output voltage between 1.2 and 3.3 V, output current up to 3 A, switching frequency in the 1-2 MHz range, inductance of 200-500 nH, efficiency of about 80%. While the previous prototype met most of these, it lost stability in some conditions, had a poorly working pre-regulator and had an unreliable soft start procedure (amongst other minor flaws). These problems have been addressed in the new version with some architecture modification, but mainly with a generous layout rework to isolate the noisy switching transistors from everything else, and to strictly separate power domains on-chip. Additionally, the pre-regulator has been fully redesigned and the logic levels of the enable (input) and power good (output) signals have been changed. The over-current protection circuitry has also been redesigned and is now present in 2 alternative versions, embedded in 2 versions of AMIS5 differing also in the driving strength of the power transistors'drivers. The over-current signal does not induce anymore a reset of the circuit, rather it limits the current to a pre-defined value while the converter continues to function. Samples of these circuits are expected back for testing in August, and first results - including some radiation tests at our X-ray machine, will be presented together with a detailed description of the functionality of AMIS5. Plans for the pursue of the work will be presented, and in particular the design of another version, also in manufacturing and expected in silicon in October, customized for bump-bonding assembly directly on PCB without any package.

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