Design of a New Switching Power Supply for the ATLAS TileCal Front-End Electronics

TWEPP 2012

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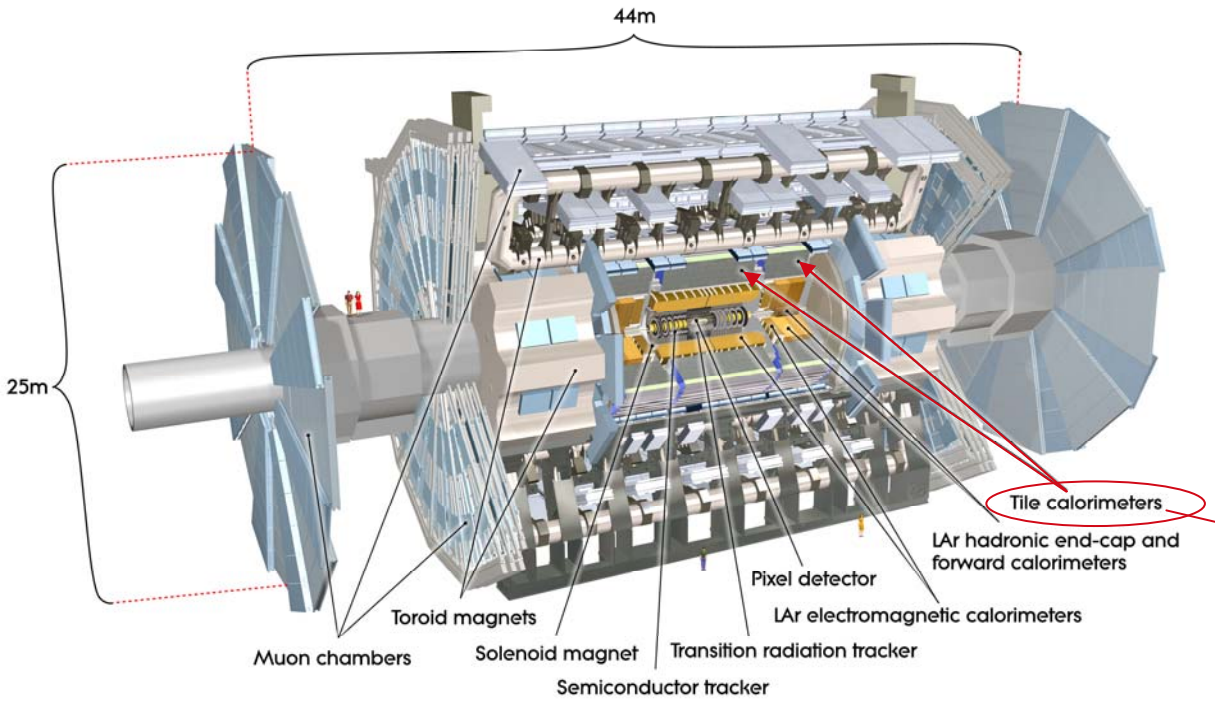
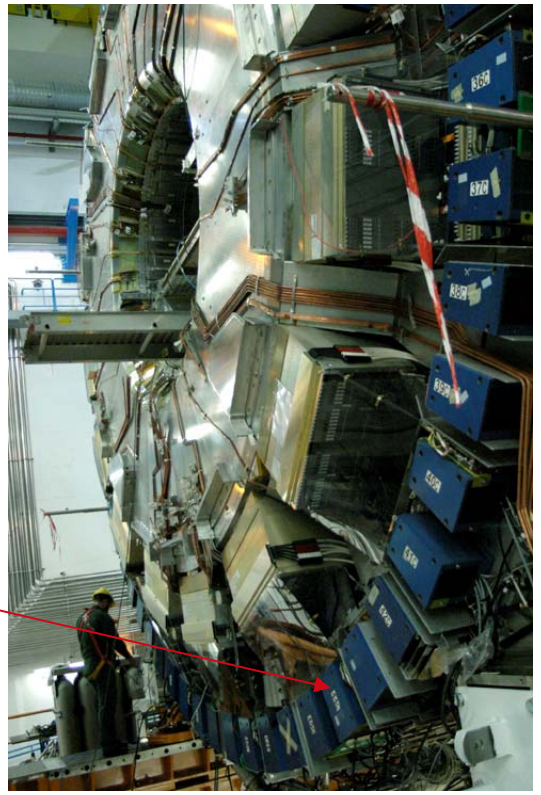
Sept. 20, 2012

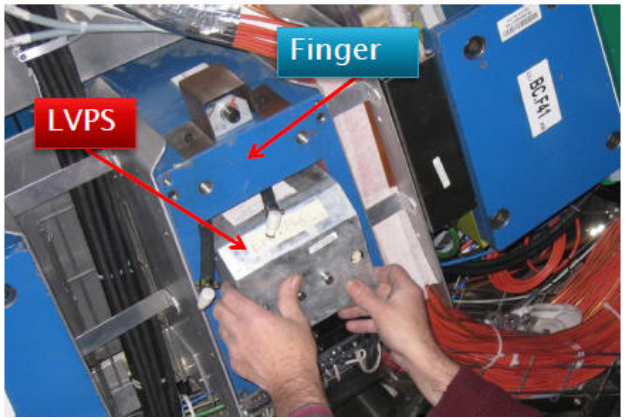
Outline

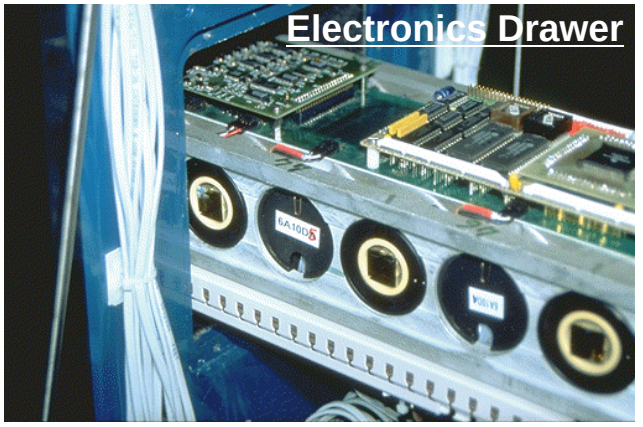
- Brief description of the TileCal Detector & power system
- Motivation for the redesign of the power supplies
- Description of a few design changes
- Radiation testing
- Performance on the detector to date
- Design plans for Phase 2
- Summary

TileCal in the ATLAS Detector





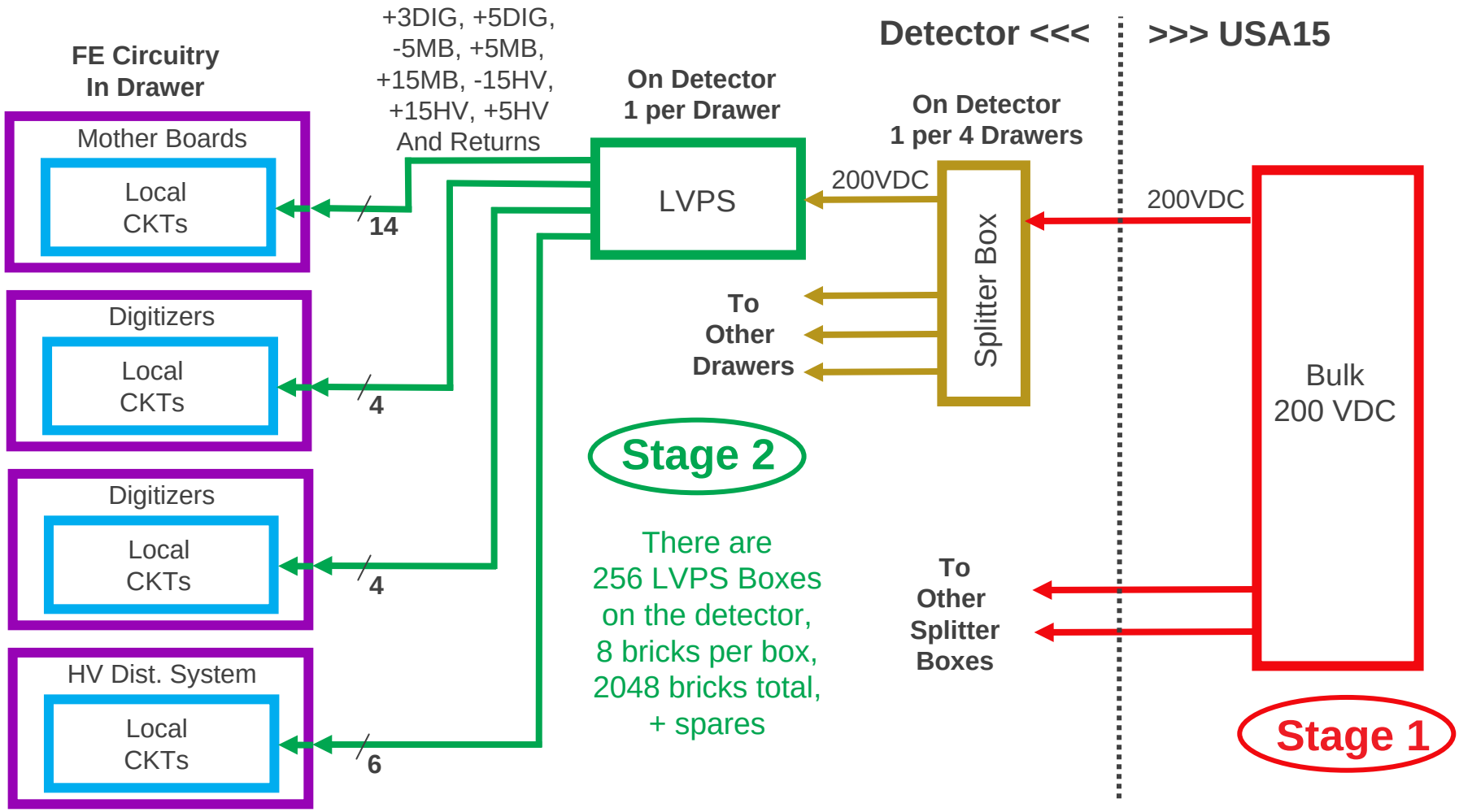




⇨ **There are 256 modules in the detector, ~10,000 readout channels**

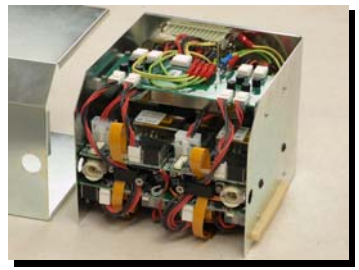
Block Diagram of the TileCal Power Dist. System

- **Block Diagram of the TileCAL Power Distribution System:**

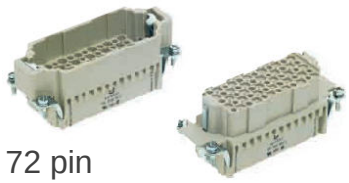


The ATLAS TileCal Low Voltage Power Supply (LVPS)

- **Block Diagram of the LVPS Box:**



Picture by Ivan Hruska



72 pin Harting Connector

Range of Voltages: 5:1
Range of Currents: 62:1

⇨ **One Basic Brick Design**
Different Component Values

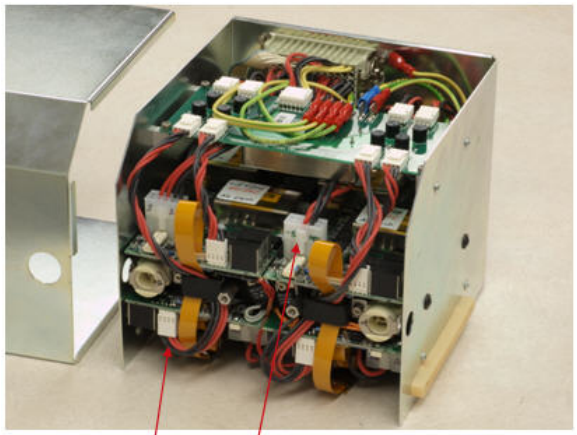
⇨ **Note: No Redundancy…**

The ATLAS TileCal LVPS (Cont.)

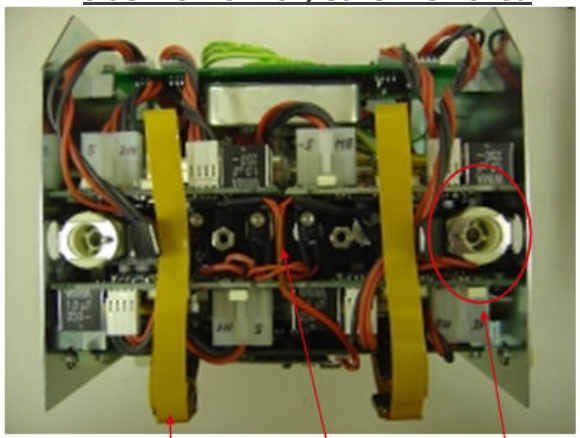
- **Full Custom Design**
  - Novel switching DC-DC power supply; 300 KHz
  - Original design by Ivan Hruska
- **Features:**
  - Custom, compact, high-efficiency, 250 Watt
  - 8 different voltages → Customized bricks
  - Water cooled; System interface & monitoring
  - Environment: Magnetic field; Radiation tolerant
  - Efficiency target: 85%
- ***Reliability is Important → Infrequent Access***

Brick Type	Nominal Voltage	Nominal Current
-5MB	-5.3	5.6 / 4.2
+5MB	+5.4	11.1 / 8.3
+15MB	+14.5	0.45 / 0.34
+3DIG	+3.45	4.74 / 3.56
+5DIG	+5.30	5.6 / 4.2
-15HV	-14.5	1.55 / 1.16
+5HV	+5.0	0.18 / 0.14
+15HV	+14.5	0.29 / 0.22

View of Box, Cover Removed



Side View of Box, Cover Removed



Individual Brick (Not to Scale)

Pictures by B. Palan

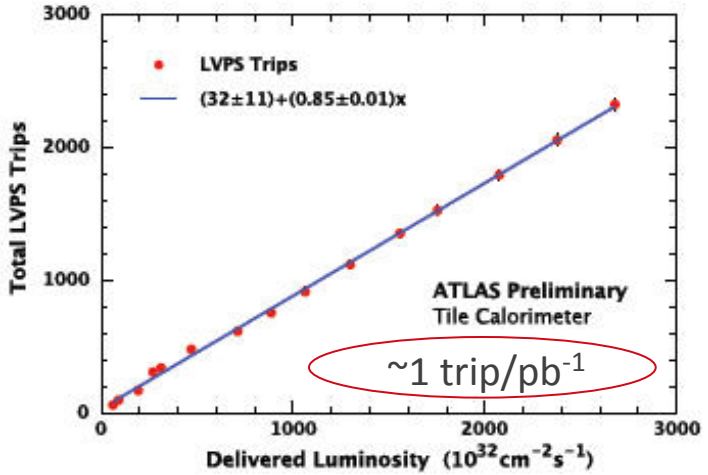
TileCal LVPS Redesign Project

- **Original production**
  - Produced in 2005
  - Installed on detector in 2006-2007
  - Performance & reliability concerns developed:
    - Board fabrication problems
    - Assembly & soldering problems
    - Substantial rework
    - Stability problems
    - Spontaneous tripping on detector → Noise
    - Hard failures on detector - ~6-10 per year
    - Later – tripping correlated with beam →
- **Redesign project**
  - Community was concerned about long-term reliability
  - Review recommendation in 2009: Consider new design
  - ANL Elec. Eng. Group collaborating since 2006, took on redesign project
    - ⇨ ***Thorough evaluation of problems & testing***
    - ⇨ ***Conclusion: Redesign best way to address issues***
    - ⇨ ***Goals & constraints:***
      - ⇨ ***Address issues***
      - ⇨ ***Minimize system perturbation***
      - ⇨ ***Design "drop-in" replacement***

Post-assembly modifications

Burned capacitors

Original Bricks: Spontaneous Tripping, Non-Destructive



Original Brick

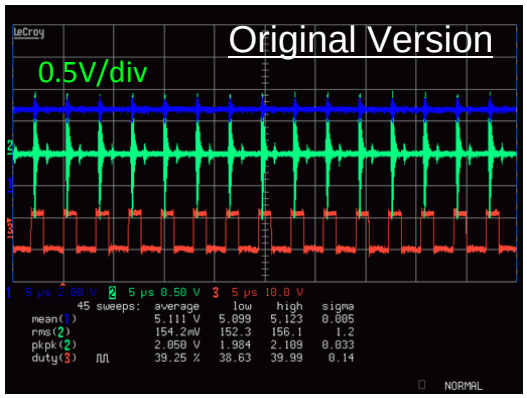
ANL"Blue Brick"

Brick Issues & Improvements

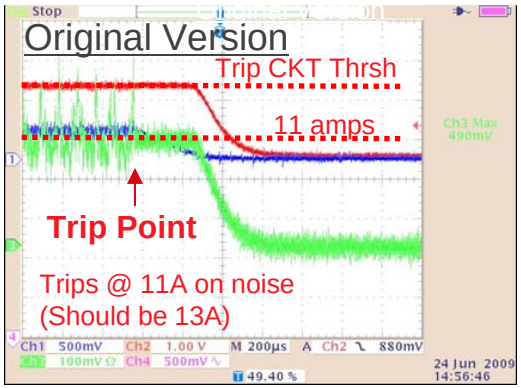
Improved Reliability

Improved Performance

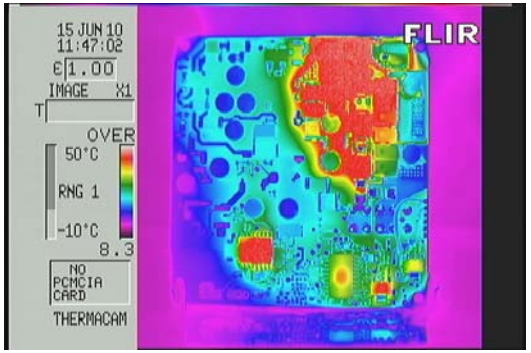
- **Critical Issues**
  - Reduce Noise
  - Opto-Isolator latch-up
  - Thermal Management
  - Better ESD protection of ICs
- **Medium-Impact Issues**
  - Improve stability
  - Improve trip circuitry
  - Power sequencing
  - Fabrication and soldering quality
  - Capacitor Voltage Ratings
- **Non-Critical But Highly Desirable**
  - Start-up pulse current
  - Eliminate pre-loads
  - Improve monitoring circuitry
  - IPC specs for assembly
  - Reduce/improve tuning



Output Noise



Tripping on Noise



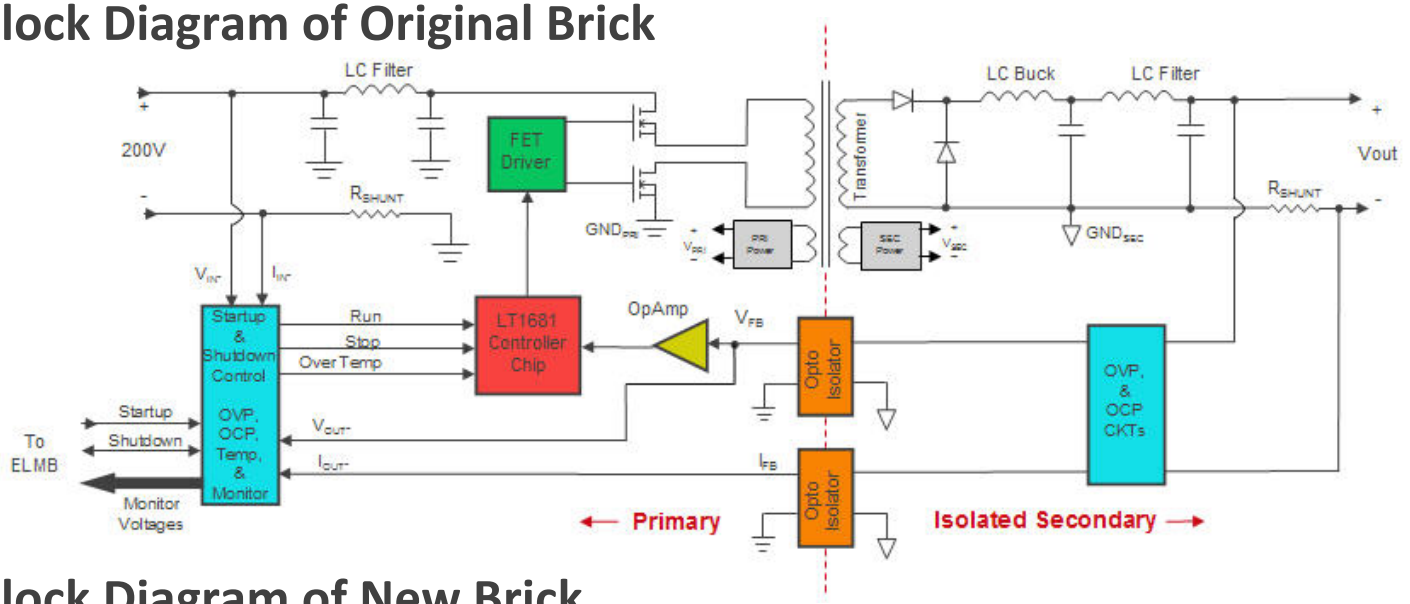
Thermal Image

⇨ ***Improved noise performance will reduce tripping***

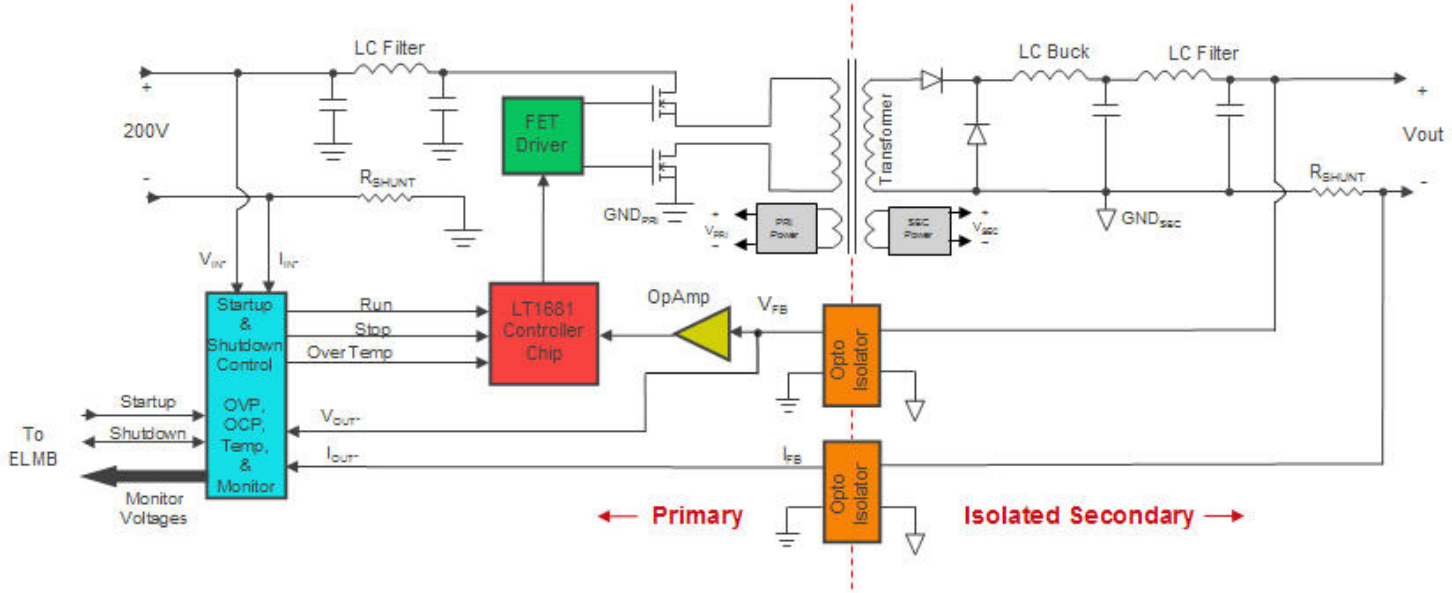
⇨ ***Other improvements in reliability as well***

Brick Improvements (Cont.)

- Block Diagram of Original Brick

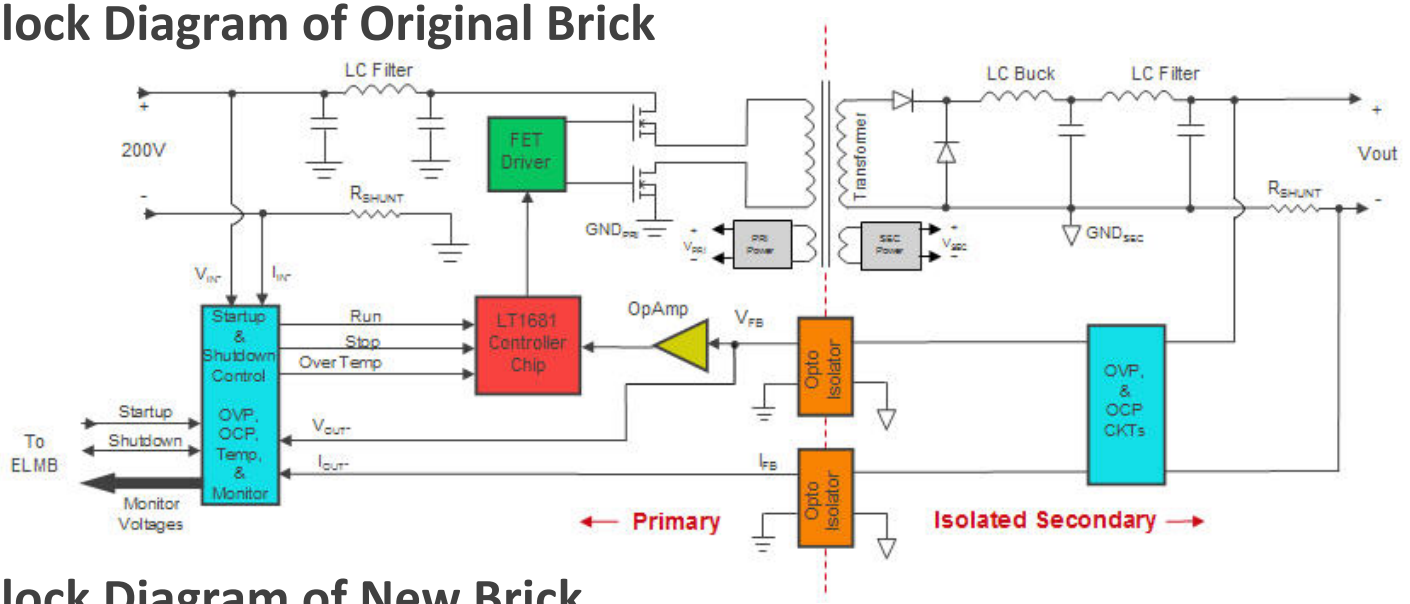


- Block Diagram of New Brick

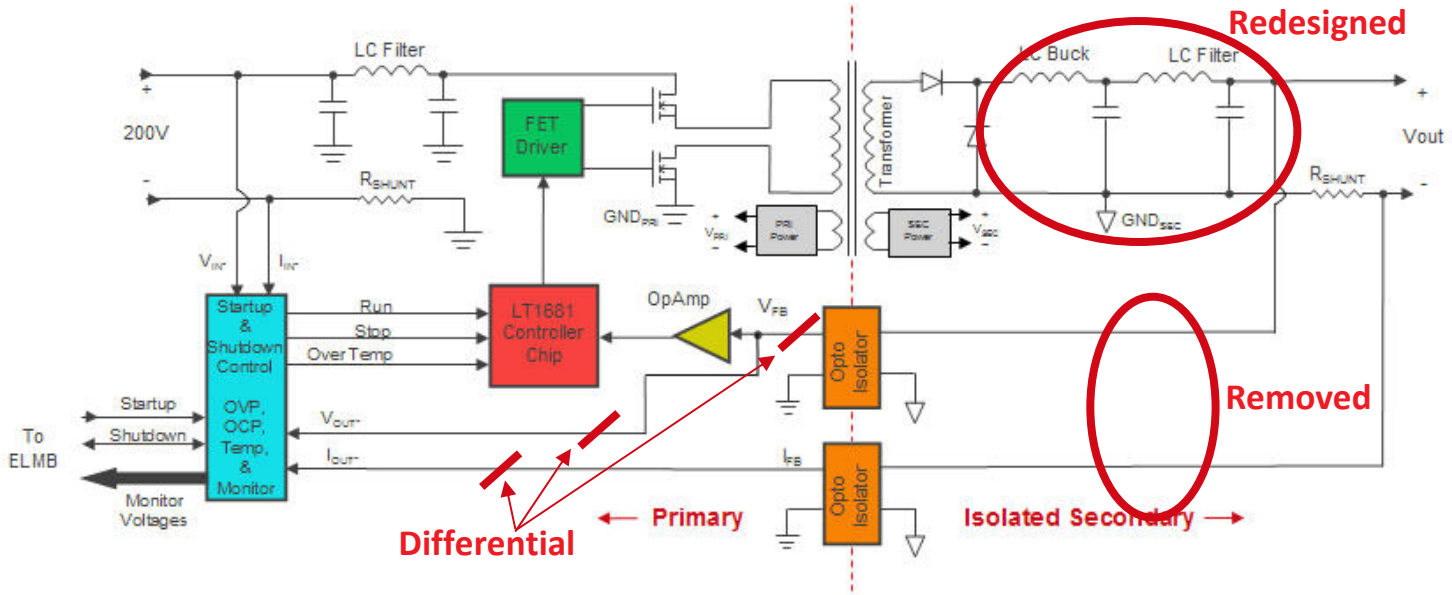


Brick Improvements (Cont.)

- Block Diagram of Original Brick

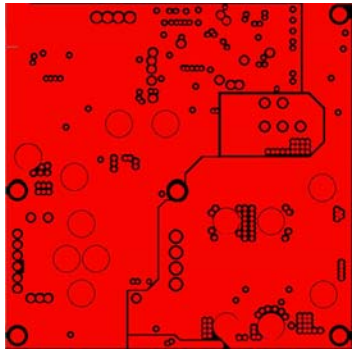


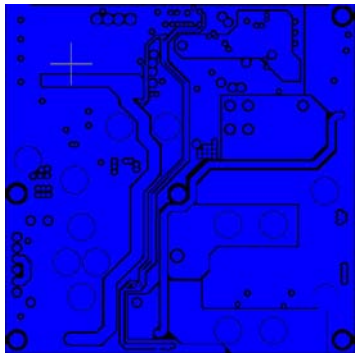
- Block Diagram of New Brick

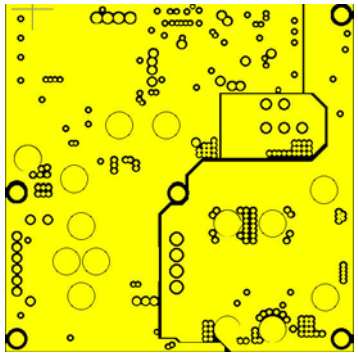


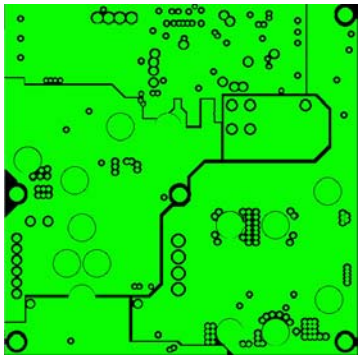
Discussion of Improvements to Design

- **Critical Issue: Reduce Noise**
  - ⇨ ***What we did:***
    - *– Add/improve ground planes*
    - *– Add/improve filtering*
    - *– Differential signals*
    - *– Careful attention to return currents*





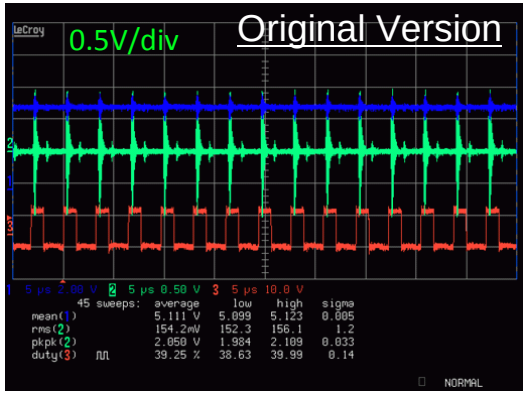




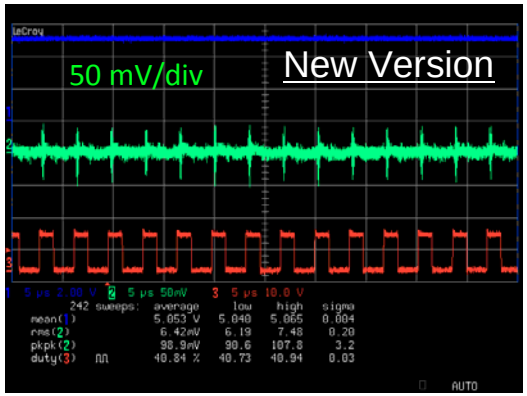
V7.3.0 – Internal Layers
(Colors = Cu)

V_{out} AC-Coupled

Clock

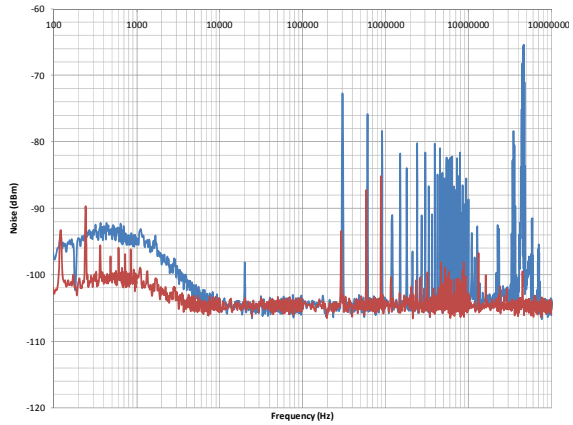


Output Noise
- +5MB @ 13A
- 2.05V p-p
- 154 mV RMS



Output Noise
- +5MB @ 13A
- 99 mV p-p
- 6.4 mV RMS

⇨ ***~X20 Improvement***



Output Noise
- +5MB @ 13A

Old Version

New Version

Improvements to Design (Cont.)

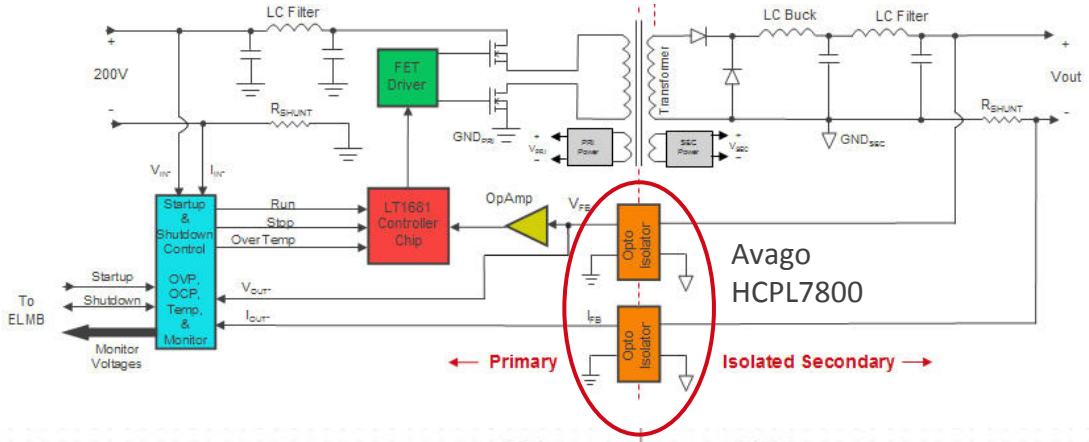
- **Critical Issue: Opto-Isolator Latch-up**

⇨ ***The symptoms:***
- ***– Bricks would latch up spontaneously***
- ***– Can persist for a long time…***

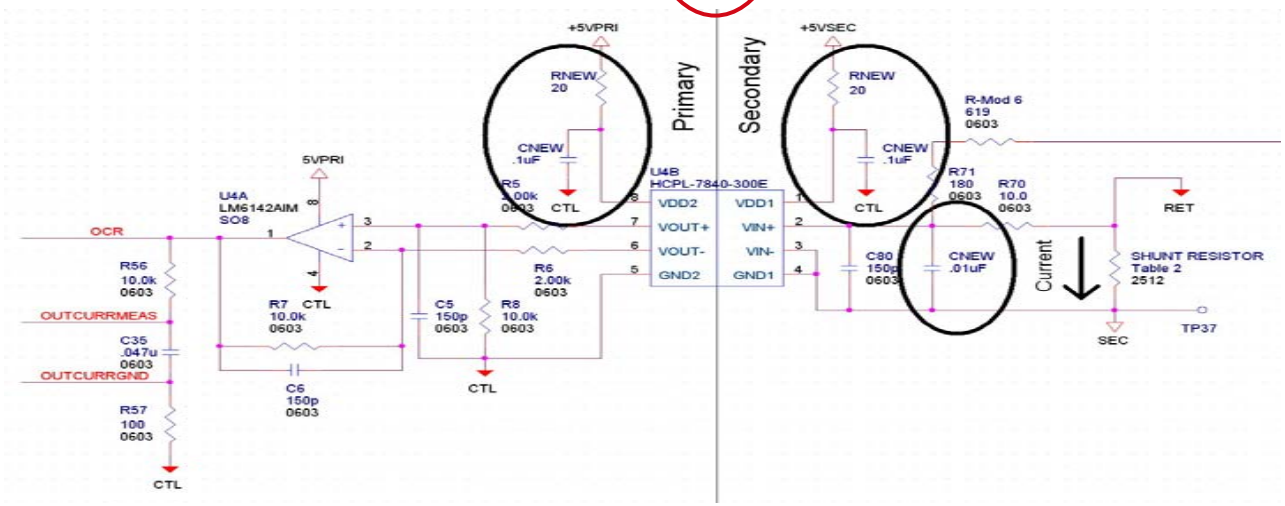
⇨***The cause:***
- ***– Undocumented requirement for extra bypass capacitors***

⇨***What we did:***
- ***– Add bypass capacitors to inputs***
- ***– Add RC filter to power pins***

Brick Block Diagram



Opto-Isolator Circuit Schematic



Improvements to Design (Cont.)

- **Critical Issue: Thermal Management**

⇨ ***The symptoms:***

– ***U1 (controller chip) & U2 (FET driver) had high failure rates***

⇨***A possible cause:***

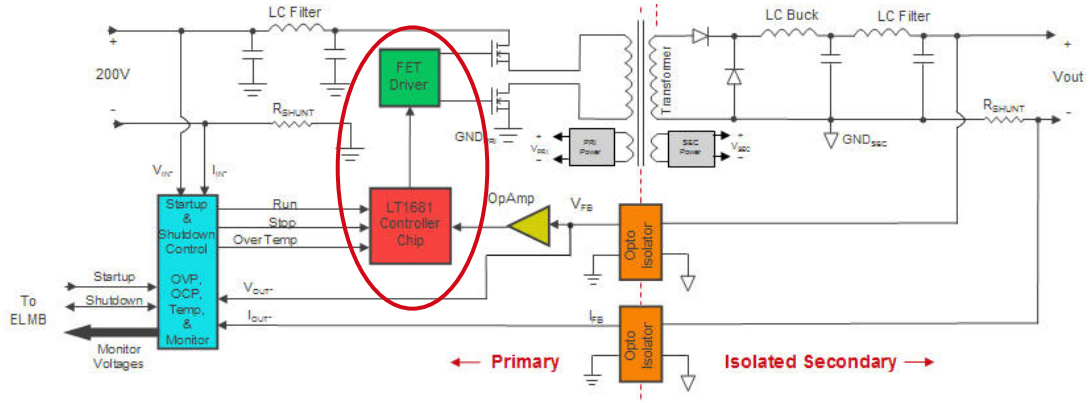
– ***Insufficient thermal coupling to cold plate***

⇨***What we did:***

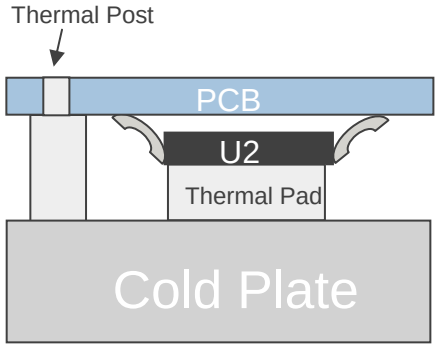
– ***New layout to get chips over cold plate***

– ***Add thermal foam (Gap Pad) to couple chips to cold plate***

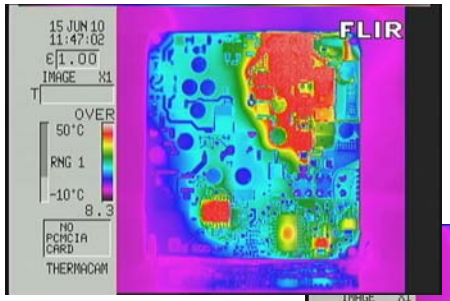
Brick Block Diagram



Implementation



Bergquist Gap Pad 1500S30



Original Version

- +5MB @ 13A

New Version

- +5MB @ 13A

Summary of Design Changes

Improved Reliability

Improved Performance

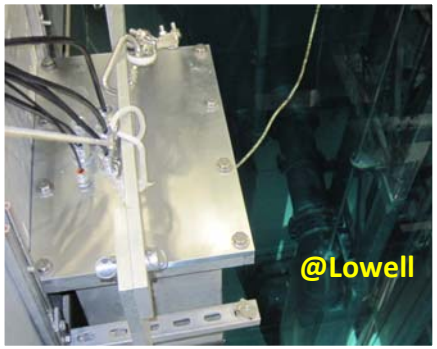
- **Critical Issues**
  - Reduce Noise……
  - Opto-Isolators……
  - Thermal Management……
  - Better input protection of U2…..
- **Medium-Impact Issues**
  - Address stability……
  - Improve trip circuitry……
  - Power sequencing……
  - No kludges ……
  - Fabrication and soldering quality
  - Tantalum capacitors……
- **Non-Critical But Highly Desirable**
  - Start-up Pulse current……
  - Eliminate pre-loads……
  - Improve monitoring circuitry…..
  - IPC specs for assembly……
  - Reduce/improve tuning…

- **What we have done:**
  - ⇨ More ground planes; improved filtering
  - ⇨ Filter supply & input pins
  - ⇨ U1 & U2 over cold plate; Use Gap Pad
  - ⇨ Add diode protection of inputs
  - ⇨ Feedback completely redesigned
  - ⇨ Simplify secondary; OVP & OCP Logical OR
  - ⇨ New regulator with programmable delay
  - ⇨ No kludges in production
  - ⇨ Will use approved vendors
  - ⇨ Use 25V caps on 15V sec. out., not 16V
  - ⇨ New regulator with programmable delay
  - ⇨ No preloads → New feedback design
  - ⇨ Differential techniques
  - ⇨ Design adheres to IPC specs
  - ⇨ Tuning of OVP now 1 step process

Radiation Tests of Bricks

- **Needed to redo radiation tolerance studies**
  - ⇨ ***We used ~same parts, but was something missed?***
  - ⇨ ***Requested by Atlas PRR committee…***
- **Requirements:**

Photons (TID)	Neutrons (NIEL)	Protons (SEU
37 KRad	6E12 n/cm2-sec	1.7E12 p/cm2-sec
Safety Factor: 70	Safety Factor: 20	Safety Factor: 20

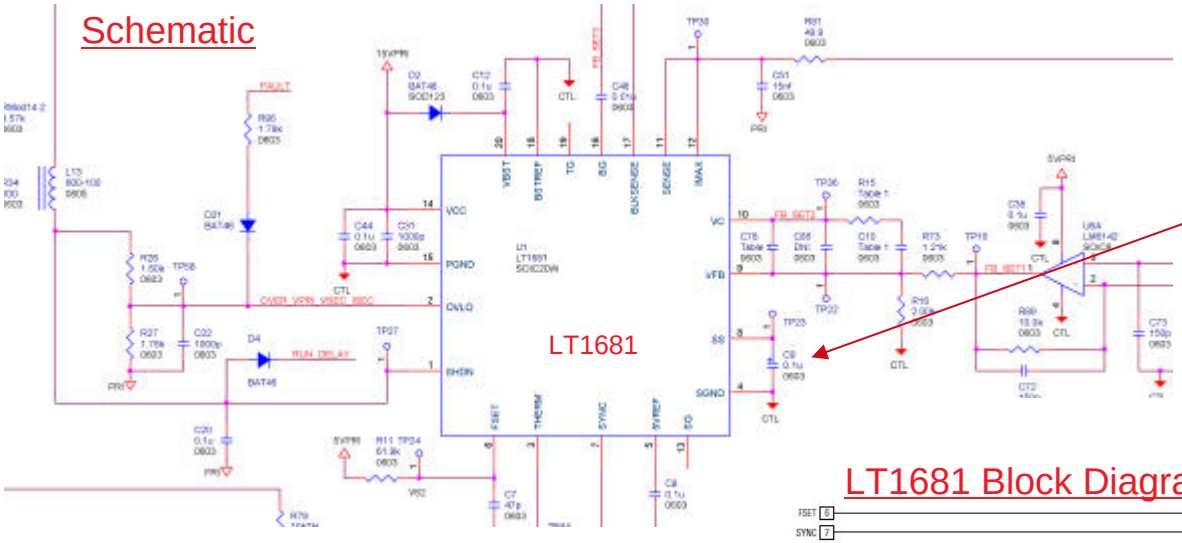


- **We performed 8 Sessions – Dec. 2010 – Apr. 2012**
  - Photons (TID) @ BNL, 1.2 MeV from Co-60
  - Neutrons (NIEL) @ UMass-Lowell, U-235 reactor
  - Protons (SEE) @ Mass General Hospital, 200 MeV radiation treatment beam line
- **Results:**
  - Photons: Slow degradation; No failures
  - Neutrons: Slow degradation, No failures
  - *Protons: Found Single Event Upset with controller chip*
  - *Protons: Energy scan found dependence on energy (SEUs not seen before in tests at 60 MeV)*

The SEU Problem

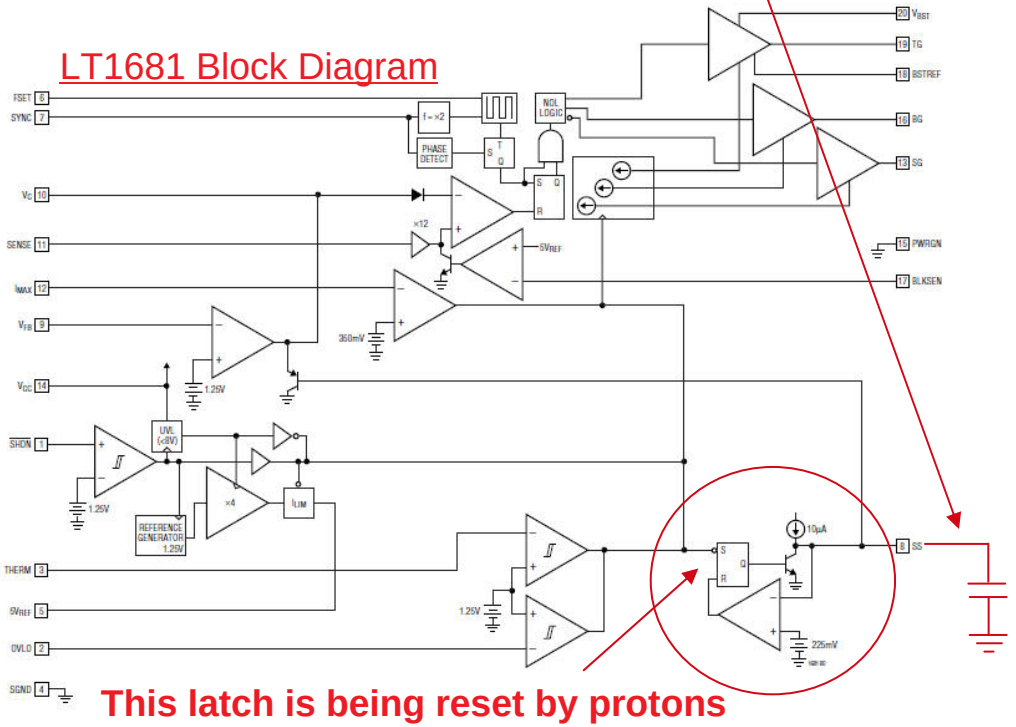
- What is happening:

Schematic



Soft-start capacitor
External component
Value controls startup delay

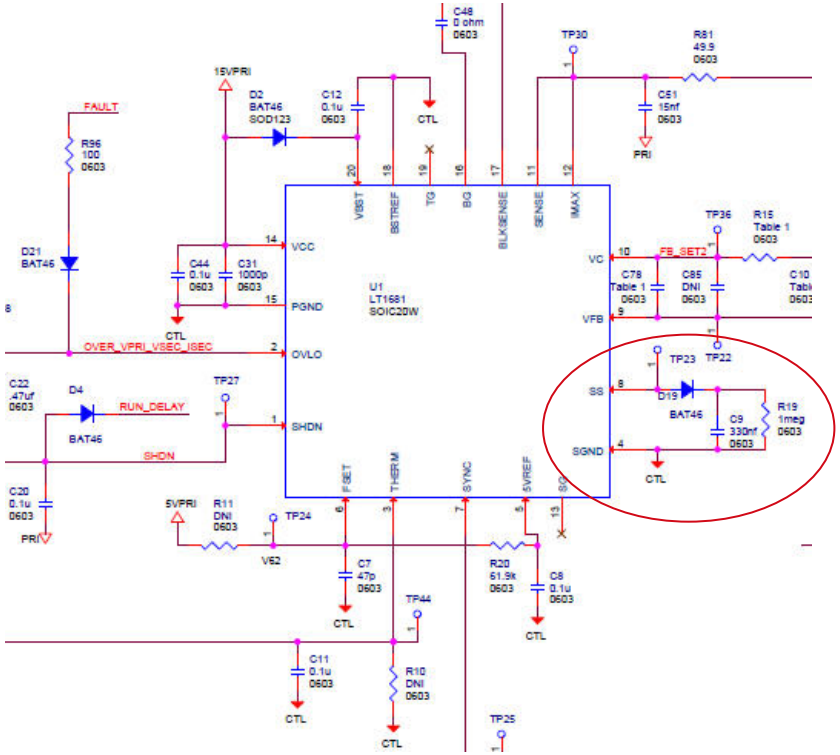
LT1681 Block Diagram



This latch is being reset by protons

The SEU Problem (Cont.)

- **Solution to the SEU Problem**



⇨ ***Tested in Building 175 on all bricks***
- ⇨ ***No overshoot on cold start***
- ⇨ ***No trips from SEU***
- ⇨ ***No damage to electronics***
- ⇨ ***No abnormal behavior in DAQ***
- ⇨ ***All other faults work normally***

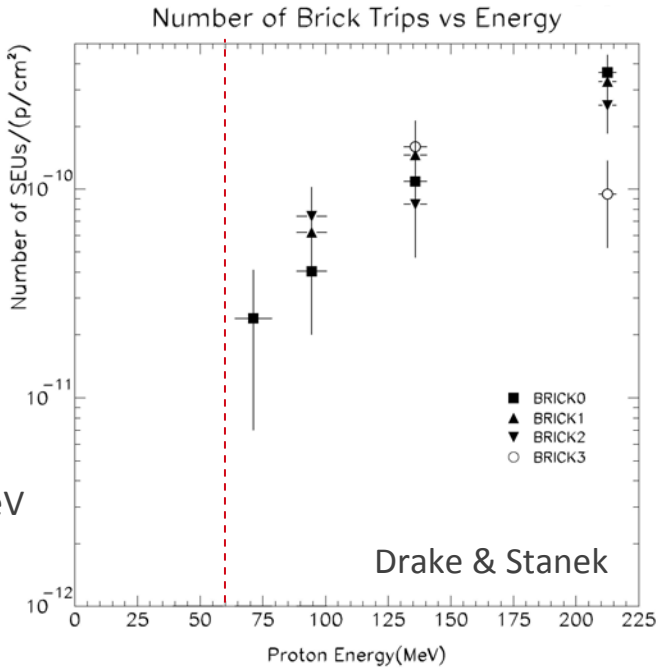
– **An elegant solution to a nasty problem, requiring only 2 additional parts**
- Diode is forward biased during cold start → Normal startup
- Diode is reverse biased for an SEU → Fast recovery since capacitance is ~ 0

⇨ ***Has been incorporated into final design, V7.5.0***

Final SEU Testing at MGH

- **Session: April 1, 2012**
  - **Energy scan: 60 MeV, 80 MeV, 100.5 MeV, 140 MeV, and 216 MeV**
  - **Used (4) V7.5.0 bricks without SEU fix**
- **Preliminary Results:**

No trips at 60 MeV



⇨ ***Can clearly see an energy threshold…***

⇨ ***Analysis continuing… → Collaboration with UW-Madison***

⇨ ***Will publish an Atlas Note shortly***

⇨ ***Energy scan not part of specs… Should it be?***

Further Studies

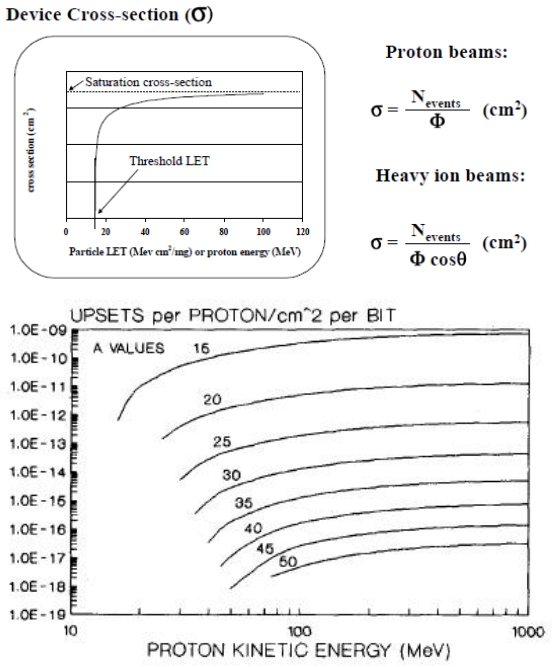
- **SEU Energy Dependence**
  - Theory: Bendel Parameters
    - ⇨ ***Originates in space instrumentation***
    - ⇨ ***How well known in HEP instrumentation?***
  - Formed research project: ANL & UM-Madison + students
    - ANL: J. Proudfoot, G. Drake, R. Stanek
    - UW: Bruce Mellado, Abhirami Senthilkumaran, Anusha Gopalakrishnan
  - Study & characterization of SEU effect in semiconductors underway
    - Dependence on technology, feature size of devices, & layout
  - Hope to contribute to future radiation tolerance specs

  ⇨ ***Paper coming at 2012 IEEE NSS***

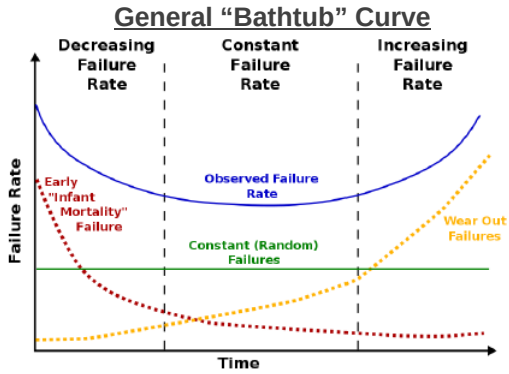
- **Reliability**
  - The power supplies have had a history of reliability problems
    - Single point failures, no redundancy
    - No analytical study done on reliability of circuitry

    ⇨ ***Typically not done in HEP instrumentation either***
  - New bricks expected to be better but no analysis done
  - Formed research project: ANL & UM-Madison + students
    - ANL: J. Proudfoot, G. Drake, R. Stanek
    - UW: Bruce Mellado, Abhirami Senthilkumaran, Anusha Gopalakrishnan
  - Study & characterization of failure rates, MTBF
  - Expect that this will influence future design methodology

  ⇨ ***Paper coming at 2012 IEEE NSS***



Stapor et al., IEEE-TNS, Vol 37-6, 1990



Our result: Probability of Failure-free operation:

R(t = 2 years)	R(t = 5 years)	R(t = 10 years)	R(t = 20 years)
0.993	0.982	0.965	0.932

⇨ ***Expect ~2 failures per year***

Project Summary to Date

- **Project Time Line**
  - **Prototype design cycle begun ~June, 2009**
  - **V7.1.0 – December, 2009, Quantity 10 bricks**
    - Tested at CERN in Box 066

    ⇨ ***Ran in long-term test since Mar. 2010 → ~1.5 yrs***

    ⇨ ***No significant problems, Now stopped*** ***Box 0_p****
  - **V7.3.1 – November, 2010, Quantity 64 (→ 80) bricks**
    - Delivered 5 boxes to CERN (+ 1 from Oct. = 5 boxes total)
    - Tested at CERN, "medium-term" test, ~1-2 months
    - **Boxes 1-5 installed on detector during Dec. 2010 shutdown**

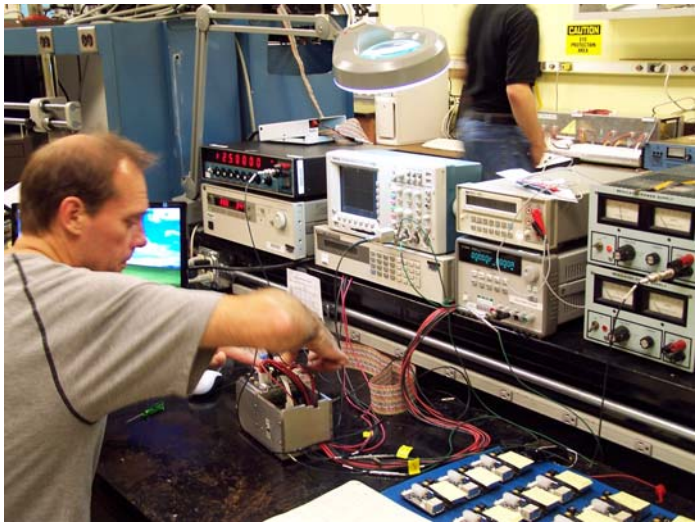
    ⇨ ***Ran in long-term test Nov.-Dec., 2010 → ~30-45 days***

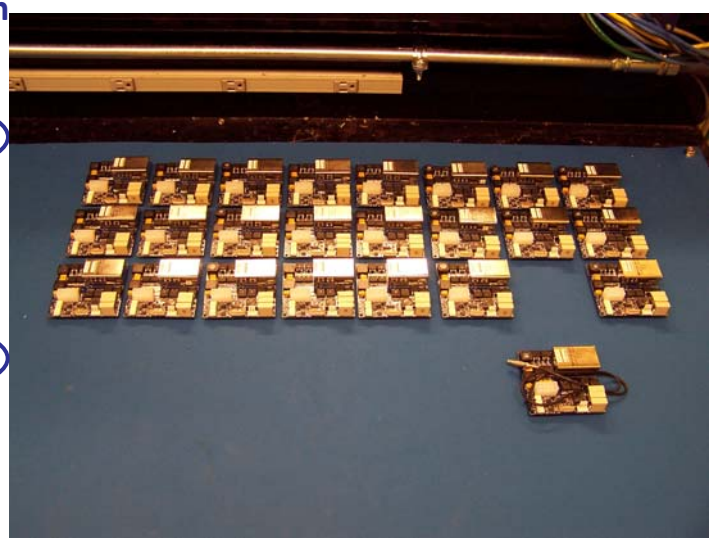
    ⇨ ***4 trips on detector to date → ~600 days (Real SEU?...)*** ***Boxes 1_p-5_p****
  - **Production Readiness Review – Aug. 17, 2011**
  - **V7.5.0 – December, 2011, Quantity 320 bricks**
    - Delivered 40 boxes to CERN
    - Installed on detector
    - → Total of 40 boxes on detector

    Boxes 6-45

    ⇨ ***1 trip on detector to date → ~240 days***
  - **V7.5.1 – January, 2012-present, Quantity 2080 bricks**
    - We are in production now, nearly complete

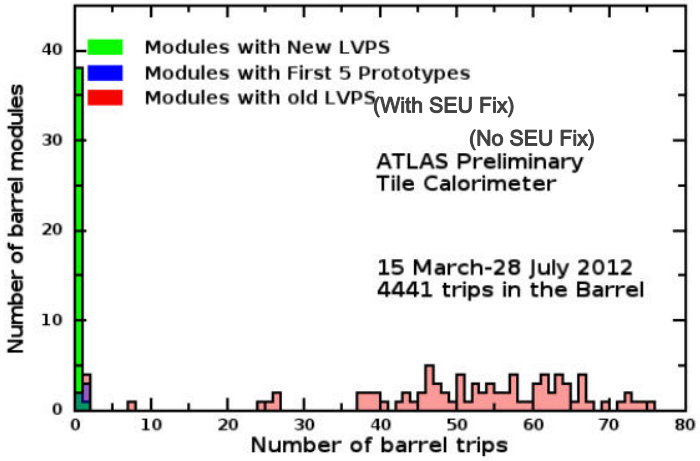
    ⇨ ***Will install remaining supplies during 2013 shutdown***





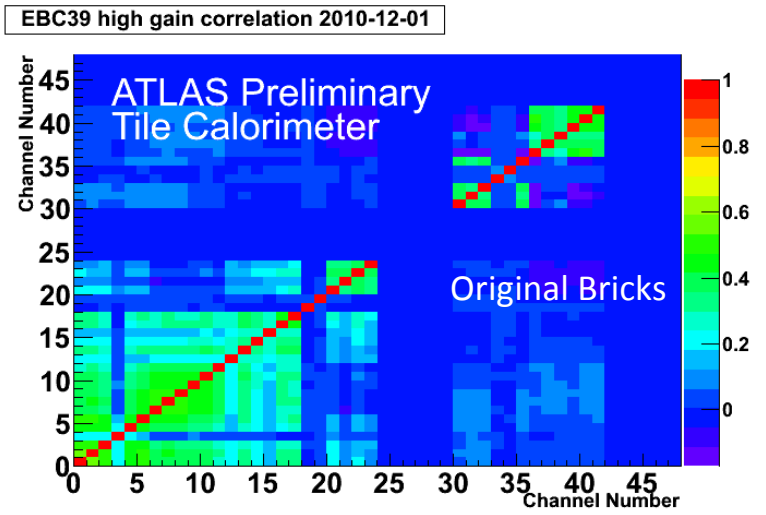
Performance on Detector

- Trips in detector by module

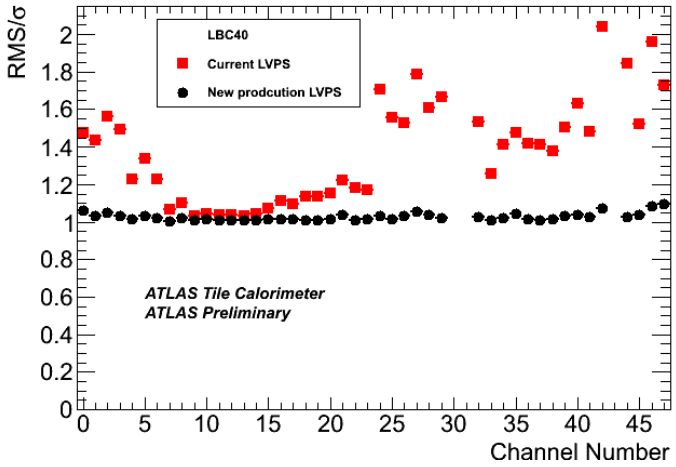


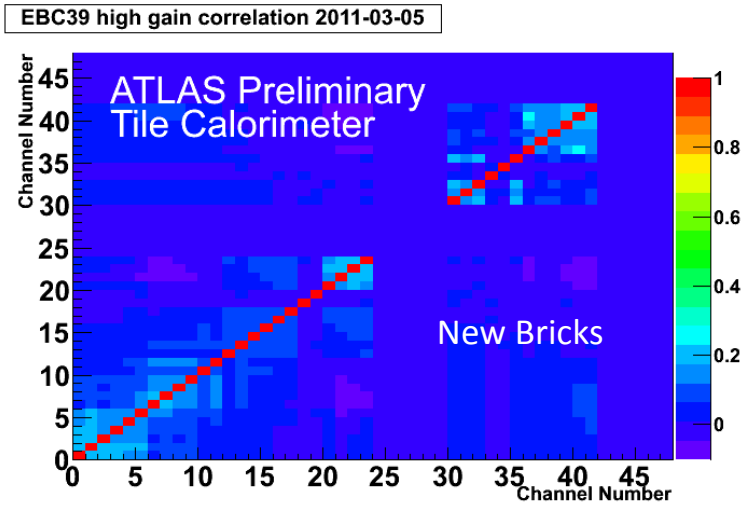
⇨ *Current Numbers (as of Sept. 1, 2012):*
- ⇨ *8404 trips of old bricks*
- ⇨ *4 trips of pre-production boxes (5 on detector)*
- ⇨ *1 trip of production boxes (40 on detector)*

- Noise Comparison – Correlated Noise



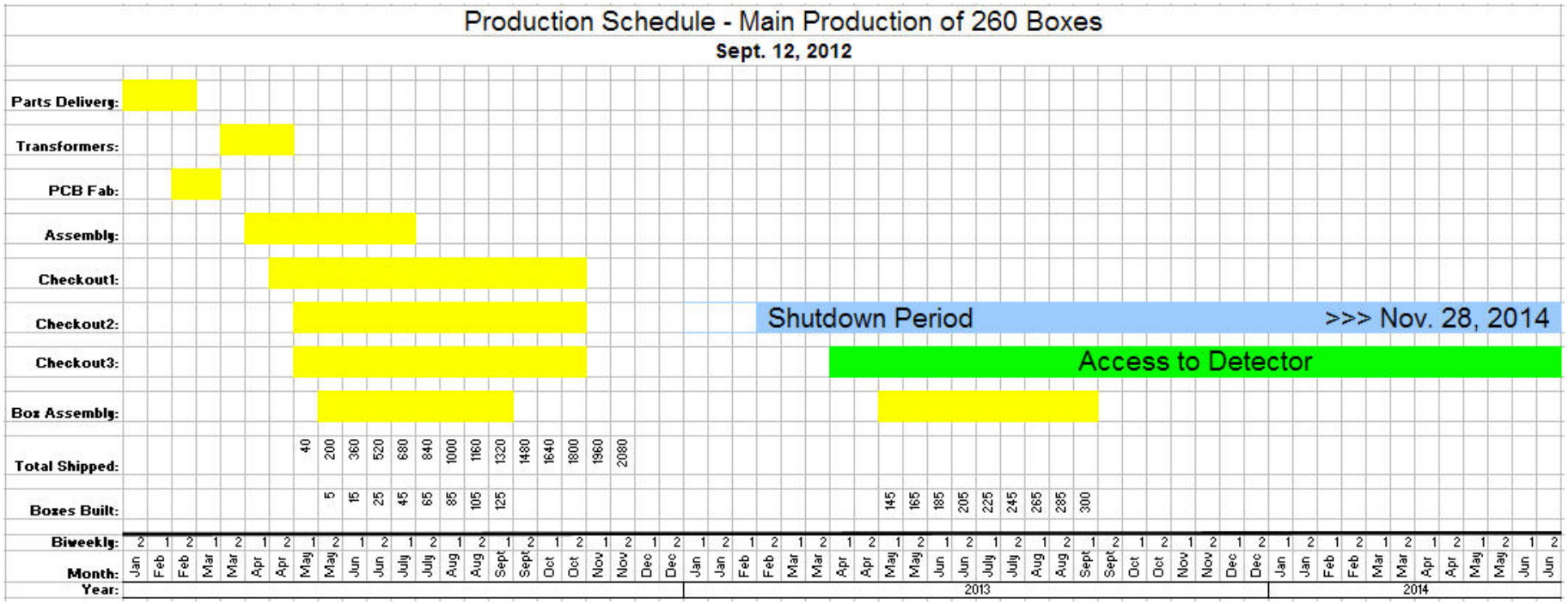
- Noise Comparison – RMS/σ





Schedule & Manpower

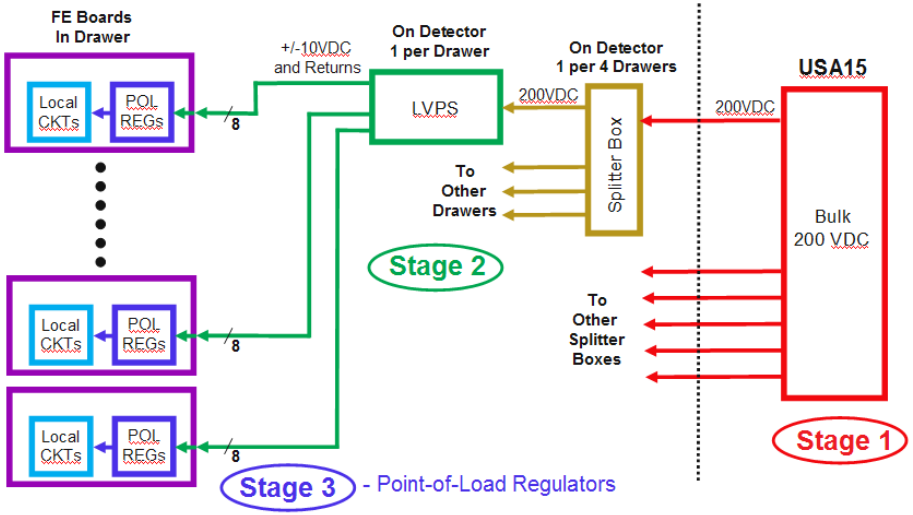
- **Main production schedule – 260 boxes**



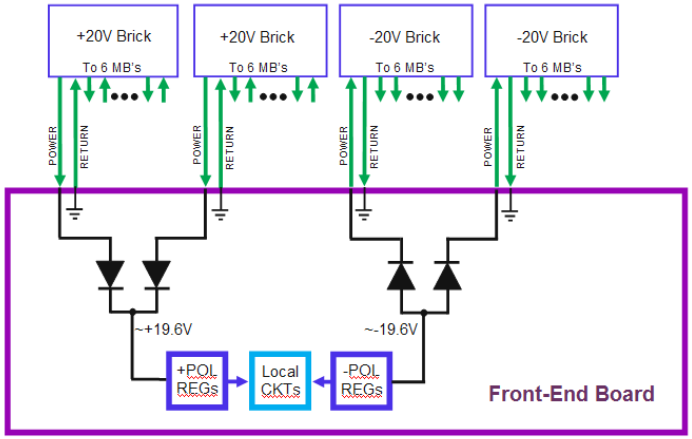
Atlas TileCal Upgrade - Phase 2

- **New Front-End Power Supplies – LVPS**
  - **Current system – 2 stages**
  - **New system – 3 stages**
    - 200V bulk (high voltage, low current)
    - Front-end switchers - +/-10V
    - ***New: Point-of-load regulators***
  - **General Features of the new system**
    - Keep 200V bulk supplies
    - Only 2 types of LVPS (8 currently)
    - Adding redundancy – diode OR
    - Point-of-load regulators
      - Low drop voltage regulators in 130nm and below
      - DC-DC buck converter architecture
      - Vin: +15VDC, Vout: +1.8 ~ +5V, 5W, 85 – 90% efficiency
      - Radiation-hard and magnetic field-tolerant
  - **Argonne responsibilities**
    - Overall power system design
    - Design of new LVPS
      - Leverages experience with current supplies
      - Rad testing of POL Regs
  - **Status:**
    - Prototype design of LVPS in progress
    - Candidate POL Regs being obtained for rad testing
      - Candidate: CERN custom ASIC
    - Target: Test beam in 2015

New 3-Stage Power System



Implementing Redundancy



Summary

- Redesign project of ATLAS TileCal front-end power supplies is nearing completion
  - Begun in 2009
  - Steady progression of prototype development, pre-production, and production
  - Will have full replacement complete in 2013 shutdown
- New design addresses several performance issues
  - Noise
  - Latch-up of opto-isolators
  - Thermal management
  - SEUs in controller chip
  - Tripping as a function of luminosity
  - + others…
- Current status of 45 boxes on detector
  - Only 4 trips of pre-production boxes in ~600 days
    - ⇨ *Probably real SEUs…*
  - Only 1 trip of production boxes in 240 days
- Radiation Tolerance Measurements & Analysis
  - Tolerance to photons & neutrons OK
  - Discovered SEU problem with controller chip
  - SEU probability has energy dependence, ~80 MeV threshold
    - ⇨ *Not specified in radiation tolerance specs…*
  - Problem has been addressed with circuit modification
  - Study under way to incorporate theoretical Bendl Curves
- Reliability analysis
  - Have developed reliability models for the new power supply
  - Expect ~2 failures per year
  - Next Gen: Redundancy
- Production checkout is nearing completion at Argonne
  - 2400 bricks total, 300 boxes
  - 45 boxes installed on detector to date; Performance looks very good
  - On track to complete on time & on budget

⇨ ***LVPS Replacement should significantly improve the performance of the TileCAL Detector***

Backup Slides

Improvements to Design (Cont.)

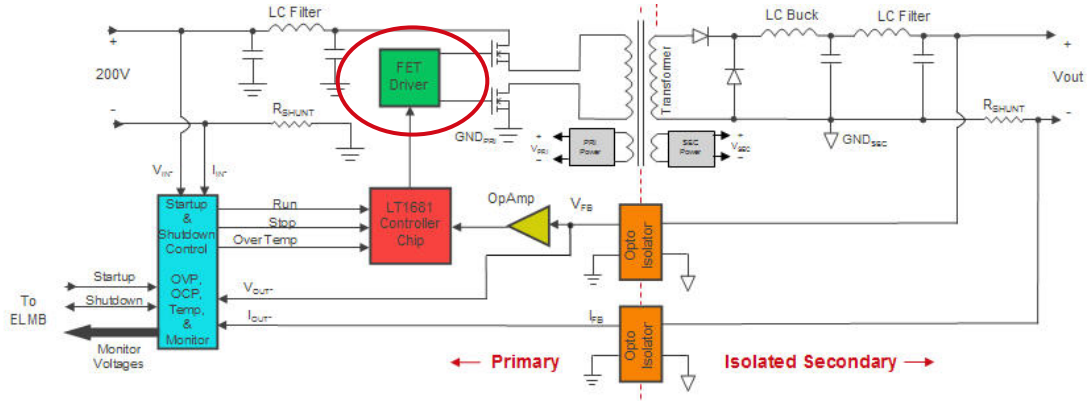
- **Critical Issue: Overload protection of U2 (FET driver)**

⇨ ***The symptoms:***
- ***U2 (FET driver) had high failure rates***

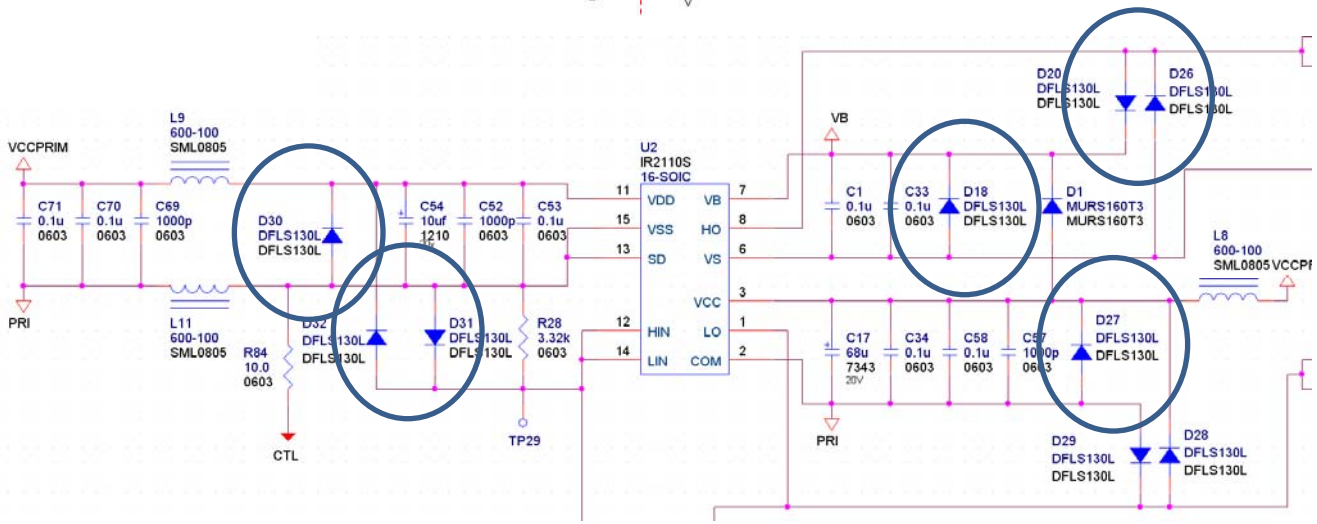
⇨***A possible cause:***
- ***Overload on input pins (→ Noise?)***

⇨***What we did:***
- ***Add diode protection to input pins***

Brick Block Diagram

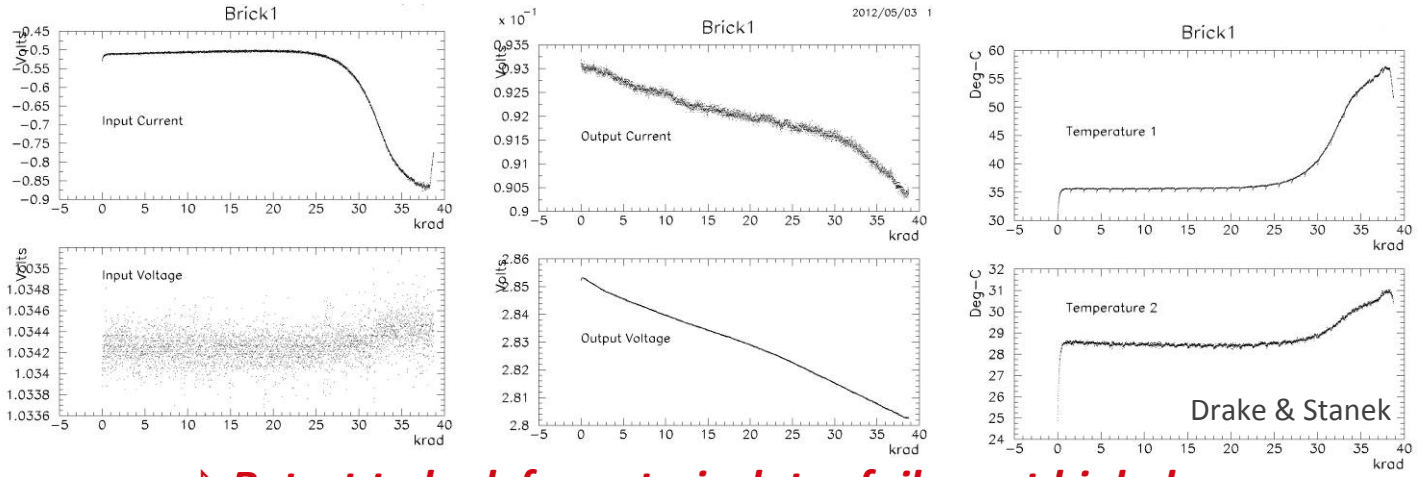


FET Driver Circuit Schematic



Final Photon Testing at BNL

- **Session: April 3, 2012**
  - The test was run over a period of 13 hours
  - Accumulated a total dose of ~37 krads
  - The output voltages and currents were monitored continuously through this period
  - Modest changes to some of the monitored values were observed
  - The inflection point in the plots seen at about 37 krad corresponds to the time the source was closed
  - There were no hard failures during the test



⇨ ***Retest to look for opto-isolator failure at high dose***

⇨ ***Found none → OK***

⇨ ***Atlas Note forthcoming***

Production Testing of Prototypes at Argonne

- **Test List:**
  - Frequency response & stability
  - Voltage range (@ minimal load)
  - Voltage range (@ nominal load)
  - Stable operating range vs. voltage
  - Stable operating range vs. current
  - Output voltage vs. output current
  - Voltage trip level vs. load
  - Current trip level vs. load
  - Output noise vs. output voltage
  - Output noise vs. output current
  - Output noise frequency spectrum
  - Clock duty factor vs. output voltage
  - Clock jitter vs. output voltage
  - Clock duty factor vs. output current
  - Clock jitter vs. output current
  - Voltage monitor output vs. output voltage
  - Current monitor output vs. output current
  - Input voltage monitor read-back
  - Input current monitor read-back
  - Temperature monitor read-back
  - Burn-in @ ~nominal load
  - Check for abnormal tripping

⇨ ***Multiply by X8…***
Tests needed for each brick type

⇨ ***Goal for production: ~0.5 hrs./brick***
(Not all tests, not as extensive…)

⇨ ***Box assembly & QA additional time***

Brick Checkout

- Block Diagram of New Test Stand