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Prototype Test Results of the Data Handling Processor for the DEPFET Pixel Vertex Detector.

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In the new Belle II detector, which is currently under construction at the Super-KEKB e+/e- collider, two additional pixel layers using the DEPFET technology will be introduced- to improve the vertex reconstruction in the high luminosity environment. The Data Handling Processor chip, which is directly bump bonded to the silicon of the DEPFET modules, is designed to steer the readout process, pre-process and compress the data. Latest test results of prototype chips, including the data processing quality, the integrity of the transmission line and SEU cross sections for storage cells will be presented here.

Summary

The DEPFET pixel vertex detector is an all-silicon detector with the readout ASICs directly bump-bonded to the sensor substrate. The Data Handling Processor (DHP) is one of the main chips, which is responsible for controlling the readout and pre-processing the data by common mode correction and pedestal subtraction algorithms to allow the zero suppressed readout with high efficiency and purity.

Each chip receives an incoming data rate of 20.5Gbps from the digitizer chips (DCD) which has to be reduced to an acceptable rate to transmit it through the DHP's serial data link. Special attention was given to the design of the differential output driver since it has to transmit the data to the backend electronics through 20 meters of cable at a signal rate of 1.6Gbps.

By carefully optimizing the on-chip data processing and storage resources, the DHP allows operation at the highest luminosities, yielding occupancies up to 3% and a maximum trigger rate of 30 kHz, with minimum data loss.

After the first half-size prototype chip, the DHP0.1(submitted in 90nm technology), a second, full-size version of the chip(DHP0.2) was designed and is currently tested. Lately the design was switched to 65nm CMOS technology and first test structures (memories, Gbit link + 1.6 GHz PLL, DAC) have been designed and characterized too. In particular the SEU cross-section of the memories and the performance of the Gbit link have been studied.

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