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A Radiation-Hard PLL for Frequency Multiplication with Programmable Input Clock and Phase-Selectable Output Signals in 130 nm CMOS

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A PLL (ePLL) is presented that is intended to be used as a frequency multiplier. The ePLL accepts 40, 80, 160 or 320 MHz as a reference and generates clocks at the same frequencies, regardless of the input. Moreover, the outputs are available with a phase resolution of 90° for the 40, 80 and 160 MHz output and 22.5° for the 320 MHz output. The radiation-hard design, integrated in a 130 nm CMOS technology, is able to operate at a supply voltage between 1.2 V and 1.5 V.

Summary

Clocking is often among the most challenging aspects in a variety of applications (data acquisition, serialization, de-serialization, etc.). Typically, a high-quality reference clock is readily available while one regularly needs a clock with a frequency that is a multiple of that of the reference clock. An example can be found in the GBT project that is currently under development at CERN as part of the LHC upgrade program. It aims at the realization of a radiation-hard chipset to be used as an on-detector transceiver for a bi-directional optical link to the counting room. A 40 MHz machine clock is available as a reference while 40, 80, 160 and 320 MHz are needed for the communication between the front-ends at the sub-detectors and the GBT while a 4.8 GHz clock is required to transmit the serialized data to the counting room. To tackle a problem like the first issue, a programmable PLL, the ePLL, has been developed as a general available building block that can handle the task of frequency multiplication efficiently. To comply with the current trend in IC technology for HEP experiments, a 130 nm CMOS technology has been selected. It is able to operate at a supply voltage between 1.2 V and 1.5 V and is fully radiation-hardened.

The ePLL accepts an input clock of 40, 80, 160 or 320 MHz, while it has output clocks at these same frequencies which are always available, regardless of the input clock. This has been realized by means of a programmable input divider of which the division ratio is such that a 40 MHz clock is presented to the phase detector. As the VCO oscillates at 320 MHz, the division ratio equals 8. The natural frequency and damping factor of the ePLL can be regulated by means of a programmable charge pump current and filter resistance and capacitance.

The VCO is a ring oscillator consisting of 8 differential stages. The 16 phases that are naturally available are used to generate the output clocks with different phase relationships to the input clock. This way, the 40, 80 and 160 MHz outputs are available in 4 phases with a resolution of 90° while the 320 MHz clock is available in 16 phases having a resolution of 22.5°.

Measurements have shown that the ePLL power consumption at a supply voltage of 1.5 V equals 17 mW. The absolute jitter for an input frequency of 40 MHz is below 16 psRMS and 20 psRMS for the 160 and 320 MHz output clock respectively.

This ePLL has been adapted to fit the needs of the GBT project as discussed before. Only 40, 80 and 160 MHz input clocks are required while only 160 and 320 MHz outputs are needed. The programmability has been realized in this case by means of an adaptive divider ratio. Moreover, both the 160 and 320 MHz outputs are available with a phase resolution of 22.5°.

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