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Readout Electronics for the MicroBooNE LAr TPC, with CMOS Front-end at 89K

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MicroBooNE experiment will use a ˜100 ton LAr TPC detector to observe interactions of neutrinos from the on-axis BNB and off-axis NuMI Beam at Fermilab. The experiment will address the low energy excess observed by MiniBooNE experiment, measure low energy neutrino cross sections, and serve as the necessary next step towards massive LArTPC detectors. An overview of the front-end readout architecture of the MicroBooNE experiment will be presented. The design, prototypes and production of electronics system will be described. The results of extensive tests on the noise versus temperature and the uniformity of response will be presented.

Summary

The MicroBooNE TPC will have 3 readout wire planes with a total of 8,256 wires/signal channels. All signals will be pre-amplified, shaped, digitized and pre-processed online before recording for offline analysis of a wide variety of physics programs. To optimize the detector performance and signal-to-noise ratio, analog front end ASIC designed in 180 nm CMOS technology, containing a preamplifier and shaper, will be deployed and operated in LAr. Pre-amplified and shaped detector signals will be differentially driven to ADC boards operated in detector hall where signals are digitized and prepared for online data pre-processing in FPGAs.

The cold electronics includes CMOS analog front-end ASIC and cold mother board, operated in LAr to obtain optimum performance. Various design considerations of the cold electronics have been taken into account to ensure reliable operation at cryogenic temperature over with a very long lifetime. The prototype cold mother board assembly has been tested by ˜1,000 chip-immersions into Liquid Nitrogen without failure. The warm interface electronics is located on top of the signal feed-through of the MicroBooNE cryostat. The intermediate amplifier is to provide appropriate gain for detector signals to make them suitable for transmission to the readout electronics board in the readout crate on the electronics platform about 20 meters away. The service board and ASIC configuration board are to provide power, charge calibration, configuration (gain and shaping time) and monitoring of the cold electronics. The TPC digitizing electronics receive the amplified and shaped detector signals from the intermediate amplifiers, then sample these signals continuously at a rate of 16 MHz. The digitized outputs from the ADC pass to an FPGA for data processing, data reduction, and preparation for readout by the DAQ system. The full chain of the MicroBooNE front-end readout electronics system of one feed-through, total of 768 channels, has been realized with the prototype electronics boards. A system test has been performed successfully. The test results show the noise of the front-end readout electronics system decreasing uniformly for all 768 channels from ˜1200 rms e at 293K to less than 600 rms e at 77K with 150pF detector (sense wire) capacitance.
The front end electronics parts have been prototyped successfully and final production is scheduled to be finished by mid 2013.

LAr TPC is a high resolution imaging technology with excellent background rejection for neutrino oscillation measurement and proton decay with potential to reveal new physics. Cryogenic electronics installed close to the detector elements is critical to make possible scaling up of such a detector into multi-kiloton range and achieve a high signal to noise ratio. MicroBooNE readout electronics system architecture and data flow are designed so as to accommodate different running modes. MicroBooNE will be the first running neutrino experiment instrumented with cryogenic CMOS analog front end ASIC.

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