

The Upgrade of the ATLAS Level-1 Central Trigger Processor

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The ATLAS Level-1 Central Trigger Processor (CTP) combines information from calorimeter and muon trigger processors as well as other sources and makes the final Level-1 Accept (L1A) decision. Due to the increasing luminosity of the LHC and the growing demands of physics and monitoring placed on the ATLAS Level-1 trigger system, the current CTP has reached its design limits. Therefore and in order to provide some margin for future operation, the CTP will be upgraded during the LHC shutdown of 2013/14.

Summary

The ATLAS Level-1 Central Trigger Processor (CTP) combines information from calorimeter and muon trigger processors as well as other sources and makes the final Level-1 Accept (L1A) decision based on a list of selection criteria in the trigger menu. Due to the increasing luminosity of the LHC and the growing demands of physics and monitoring placed on the ATLAS Level-1 trigger system, the current CTP has reached its design limits. All 160 trigger inputs signals that can be used in the trigger combinations and almost all of the 256 individually maskable and prescalable combination items are being used with the latest trigger menus.

Therefore and in order to provide some margin for future operation, the CTP will be upgraded during the LHC shutdown of 2013/14. The upgrade is threefold: First, the number of the trigger inputs signals will be doubled by running them internally at twice the speed. Secondly, a new core module (CTPCORE) will allow to combine the trigger input signals in twice the number of trigger items. Thirdly, the backplane of the CTP and the output module (CTPOUT) will be modified in order to provide more outputs towards the front-end electronics of the experiment and to allow for several partitions of L1A with independent trigger menu and busy handling. In addition to the above, provision will be made on the new CTPCORE module to receive trigger input signals on optical high-speed links for new trigger development, e.g. a topological trigger processor.

The specifications and design of the new modules will be presented.

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