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Design and characterization of a radiation-tolerant wide dynamic-range DC coupled and double polarity charge-to-digital converter for ionization chambers and diamond detectors

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The design is based on charge-to-frequency conversion, with the addition of a new system to reconfigure the front-end - depending on the input signal level to increase the dynamic range at constant sampling frequency. The ASIC has been designed in 0.25 µm radiation tolerant CMOS technology aiming to cover a dynamic range of six decades with a 25kHz sampling rate: design, simulation and measurements are presented.

Summary

Ionization chambers are employed in the Large Hardon Collider at CERN to detect beam losses by the Beam Loss Monitoring system (BLM), to protect the superconducting magnets and provide aid to machine setup and diagnostic information. The ASIC provides a digital output code corresponding to the integral of the input current over the 40us acquisition interval, aiming for a 120dB dynamic range. It has been designed in a commercial CMOS technology to meet the radiation tolerance requirements of 10 Mrad. The ASIC digitizes input charge of both negative and positive polarity over six decades (120dB) and is foreseen working without calibration, by referencing the conversion to an on-chip 1.2-V bandgap voltage reference. consumes less than 40 mW from a 2.5-V supply (pads excluded).

The paper includes design, simulation, layout considerations and analysis of the results from a manufacturing run that took place at the end of January.

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