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Ultra-Low-Power Radiation Hardened Analog to Digital Converter for Particle Detector Readout Applications

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Radiation hardened analog to digital converter (ADC) has been designed for future high energy physics experiments. The ADC has been designed in a commercial 130nm CMOS process and it achieves 12-bit resolution,40 MS/s sampling speed, 15 mW power consumption and hardness to at least 1 Megarad(Si) of total ionizing dose (TID). 16 ADC channels will be placed on one packaged silicon chip. The ADC is a perfect match to the readout boards of the Liquid Argon Calorimeter of the ATLAS detector in the planned high-luminosity large hadron collider and to many other future experiments.

Summary

The planned large-scale high energy particle collider experiments with very high-density readout electronics have created an urgent need for ultra-low-power radiation hardened analog to digital converters (ADCs). As of today, such devices are not available in spite of numerous efforts to find commercial "component of the shelves (COTS)"ADCs that meet the needed specifications of the future experiments. Thus, a need exists for custom-designed ADCs that are suitable for these experiments.

We have designed an ultra-low-power radiation hardened ADC for future high energy particle physics experiments. The ADC has been designed in a commercial 130nm CMOS process and it achieves 12-bit resolution (ENOB is 10.7 bits), 40 MS/s sampling speed, 15 mW power consumption per channel and higher than 1 Mrad(Si) total ionizing dose hardness. The 130 nm logic transistors that are used in the design are inherently hard to more than 1 Mrad(Si) of total ionizing dose. Radiation hardness by design (RHBD) techniques are used in the ADC in order to guarantee sufficient tolerance to single event radiation effects, such single event latchup (SEL) and single event functional interrupt(SEFI). 16 ADC channels will be placed on one packaged silicon chip and LVDS outputs will be provided from this chip. The ultra-low-power radiation hardened ADC is a perfect match to the readout boards of the Liquid Argon Calorimeter of the ATLAS detector in the planned High-Luminosity Large Hadron Collider (HL-LHC) and to many other future experiments as well.

We have successfully implemented the full 12-bit ADC design using thin-oxide 130nm CMOS transistors that are rated to 1.2 volts. The ADC is based on a design technique called "correlated level shifting" (CLS) that effectively "squares"the gain of the used amplifiers and thus allows the use of robust, low-power amplifier circuit topologies in the inherently TID-tolerant deep sub-micron nanotechnology CMOS fabrication processes that, from an analog designer's perspective, suffer from limited power supply levels. We have also used other innovative techniques to achieve an ultra-low power dissipation value, namely 15mW per channel. Note that the commercial ADC currently used in the readout boards of the Liquid Argon Calorimeter of the ATLAS detector at LHC consumes 595 mW per channel.

We have currently finished a transistor-level design of the ADC in a U.S. Department of Energy (DOE) Small Business Innovative Research (SBIR) phase I program and we are waiting for phase II funding that will allow us to move to the prototype manufacturing phase. Simulation results, low-power circuit techniques and radiation hardening methods for the full ADC will be discussed in the proposed presentation and paper.

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