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First experience with radiation-hard active sensors in 180 nm HV CMOS technology

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We explore the concept of using a deep-submicron HV CMOS process to produce a drop-in replacement for traditional radiation-hard silicon sensors. Such active sensors contain simple circuits, e.g. amplifiers and discriminators, but still require a traditional (pixel or strip) readout chip. This approach yields most advantages of MAPS (improved resolution, reduced cost and material budget, etc.), without the complication of full integration on a single chip.

After outlining the design of the HV2FEI4 test ASIC, characterization results and first experience obtained with pixel and strip readout will be shown before discussing future prospects of active sensors.

Summary

Deep-submicron HV CMOS processes feature moderate bulk resistivity and HV capability and are therefore good candidates for drift-based radiation-hard monolithic active pixel sensors (MAPS). It is possible to apply 60-100V of bias voltage leading to a depletion depth of ˜10-20 um. Thanks to the high electric field, charge collection is fast and nearly insensitive to radiation-induced trapping. Due to the dopant concentration, the depletion voltage is stable up to ˜1E16 neq/cm2.

We explore the concept of using such a HV CMOS process to produce active sensors that contain simple circuits to amplify and discriminate the signal. A traditional readout chip is still needed to receive and organize the data from the active sensor and handle high-level functionality such as trigger management. We test our devices with the ATLAS FE-I4 pixel readout chip and the ATLAS ABCN and the LHCb Beetle strip readout chips. Either strip-like or pixel-like readout can be selected on the same device. The active sensor approach offers many advantages with respect to standard silicon sensors: fabrication in fully commercial CMOS processes costs less than traditional diode sensors, aggressive thinning is resulting in much lower mass, bias voltage and operation temperature requirements are favourable. From a practical perspective, maintaining the traditional separation between sensing and processing functions lowers development cost and makes use of existing infrastructure.

To explore the performance and radiation hardness of active sensors, the HV2FEI4 ASIC was produced in the AMS H18 process. It is compatible with the pixel and strip readout chips mentioned above and features a matrix of 60 by 24 pixels with a pixel cell size of 33 by 125 um. Thanks to relying on active circuits, capacitive coupling to the pixel readout chip appears feasible and is explored with HV2FEI4 chips glued to FE-I4s. The option to replace the expensive and time-consuming bump-bonding by gluing would significantly lower the cost of future large-scale Pixel Detector upgrades and enable the instrumentation of larger areas with pixel detectors. For comparison, bump-bonding the HV2FEI4 with gold stud-bumps is still possible.

The HV2FEI4 pixels are combined to match the readout multiplicity of the respective chips: for the pixel readout, three HV-CMOS pixels are multiplexed onto one FE-I4 pixel such that the hit pixels are encoded by the pulse height. In this way, the position resolution of the HV-CMOS sensor can be significantly better than the granularity of the readout chip suggests. For the strip readout, the pixel cells are combined to form virtual strips. Here, the z-position of the hit is encoded via the discriminator's pulse height and can be evaluated by analogue strip readout electronics like the Beetle chip.

The presentation will give an overview of the characterization results of the HV2FEI4 chip and highlight first experience with both pixel and strip readout. In addition, the status of the irradiation programme will be summarized and future prospects will be discussed.

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