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A monolithic pixel sensor (TRAPPISTe-2) for particle physics instrumentation in OKI 0.2µm SOI technology

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A monolithic Active Pixel sensor for charged particle tracking has been developed. This sensor is within the frame of a R&D project called TRAPPISTe (Tracking Particles for Physics Instrumentation in SOI Technology), with the aim of studying the feasibility of developing a Monolithic Active Pixel Sensor (MAPS)with SOI technology. TRAPPISTe-2 is the second prototype in this series and was fabricated with OKI 0.20µm fully depleted (FD-SOI) CMOS process. This Monolithic pixel sensor has been designed, fabricated and is being tested. The first results that will be presented are based on the measurements performed.

Summary

The use of different technologies in the field of particle physics detector has been always limited by the effects of radiation in both the sensors and the processing circuitry. This fact has force the community to evaluate the use of different technological approaches to minimize the impact of radiation in new developments. Nowadays, most pixel detectors that are in operation are hybrid active pixel sensors. The limitation of hybrid detectors for particle physics applications comes from the material budget of having two separate wafers, the cost of bump bonding and the minimum pixel size. This problematic integration step has led to increased efforts related to monolithic solutions, where the sensor, amplification and logic circuitry are found in the same Si-wafer. These monolithic solutions have evolved from basic epi-layer thicker solution, to more sophisticated ones, such as new 3D integration technologies. Another solution evaluated is Silicon On Insulator (SOI) technology, which is the one that has been studied in this project.

TRAPPISTe (Tracking for Particle Physics Instrumentation in SOI Technology) is a R&D project used to study the feasibility of developing a Monolithic Active Pixel Sensor (MAPS) with SOI technology. In this paper we present the results obtained with the second prototype in this series of sensors, called Trappiste-2. The device is fabricated with 0.20µm fully depleted (FD-SOI) CMOS technology, provided by OKI Semiconductors, through the SOIPIX collaboration. The main characteristics of the technology are the use of 700 Ohm n-type substrate with a 5 metal layer for the top circuitry layer and the prototype thickness is around 250µm.
The prototype submitted for fabrication included different readout architectures for evaluation, and several test transistors. The architectures are the basic 3-transistor readout and a charge sensitive amplifier (CSA) with a shaping amplifier. Although they have been widely used in the past, they have to be characterized, validated and optimized. The chip has a 6x6 pixel matrix which consists of detector implants connected to both 3T and CSA readout architectures, where each pixel size is 150µm x 150µm. The shapes of these detectors have been changed to study the breakdown voltage of the detector. For this prototype different shapes of implants, such as square, octagonal and rounded have been used.

A problem related to SOI wafer is the back gate effect. Since the area under the transistor acts as a back gate its potential affects the threshold voltage and the leakage current of the transistor. Back gate effect depends on many factors, like thickness of the bulk substrate, voltage applied for detection and guard ring patterns that can be introduced below the oxide to improve signal acquisition. The OKI technology provides a method to mitigate the back gate effect with a buried P-well (BPW). The first results that will be presented are based on the measurements performed at different back voltage. One main effort will be focused on the testing of the viability of the technology as a particle detector.

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