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ATLAS Level-1 Calorimeter Trigger Upgrades for Phase I

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The ATLAS Level-1 Trigger requires several upgrades to maintain physics sensitivity as the LHC luminosity is raised. One of the most challenging is the electron trigger, with a major development planned for installation in 2018.
New on-detector electronics will be installed to digitise electromagnetic calorimetry signals, providing trigger access to shower profile information. The trigger processing will be ATCA-based, with each multi-FPGA module processing ˜1 Tbit/s of calorimeter digits within the current 2.5 microsecond Level-1 Trigger latency limit. The presentation will address the system architecture and design, with status of current tests.

Summary

The Phase-I ATLAS upgrade programme includes several changes aimed at improving the Level-1 Trigger performance, involving both the ATLAS detector and the Level-1 Trigger system. For the upgraded electron trigger, sensitivity to electroweak processes makes it essential to maintain an acceptable trigger rate for electron trigger thresholds as low as 20 GeV range. To realise this performance, additional electromagnetic calorimeter data will be provided for the trigger in digital form by a partial replacement of the Liquid Argon Calorimeter on-detector electronics. This will give higher-granularity calorimeter information both laterally and in depth. New algorithms running in additional hardware will be added to the existing Level-1 Trigger to process these data, which are expected from simulation studies to give the required trigger performance with higher LHC pileup of Phase-I running. The additional trigger logic must remain within the existing hardware trigger latency envelope for compatibility with existing detectors.
The new off-detector digital processing chain will consist of two subsystems: a Digital Processor System (DPS) will perform digital filtering on the new digital calorimeter data; and a feature extractor subsystem with Electron and Jet processors (eFEX, jFeX) will identify calorimeter trigger signatures. While the DPS processing in principle handles each digital channel separately, the eFEX and jFeX logic is based on sliding-window algorithms and requires substantial data duplication and overlap between adjacent copies of the algorithms. It is expected that the eFEX will process a tenfold increase in trigger data input compared to the current electron trigger.
The eFEX will be designed as a modular subsystem, housed in two ATCA crates and consisting of around 20 modules, each receiving data on 150-200 optical fibres at 6-10 Gb/s. The optical signals will be passed to transceivers near FPGAs on the main modules via dense optical connectors in the ATCA Zone-3 connector area. To provide the data environment needed by the overlapping window algorithms, additional copies of many of the input signals from the DPS will be fanned out to neighbouring modules as well as to adjacent FPGAs on the same module.
Information describing objects identified by the FEX subsystems will be sent over optical fibres to a Topology Processor subsystem currently under development, for use in combination with information from the upgraded Level-1 Muon and the present Level-1 1Calorimeter systems. Information on the features will also be used to seed the Level-2 Trigger processing.

The presentation will include the motivation for architectural design choices, first results from test modules, and comparison with high-speed link simulations.

Primary author: Dr QIAN, Weiming (Rutherford Appleton Laboratory)

Presenter: Dr QIAN, Weiming (Rutherford Appleton Laboratory)

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