The AMC13 Module

A Common Solution for Clock, Controls and DAQ Services in CMS MicroTCA Systems

Status Report, Test Updates

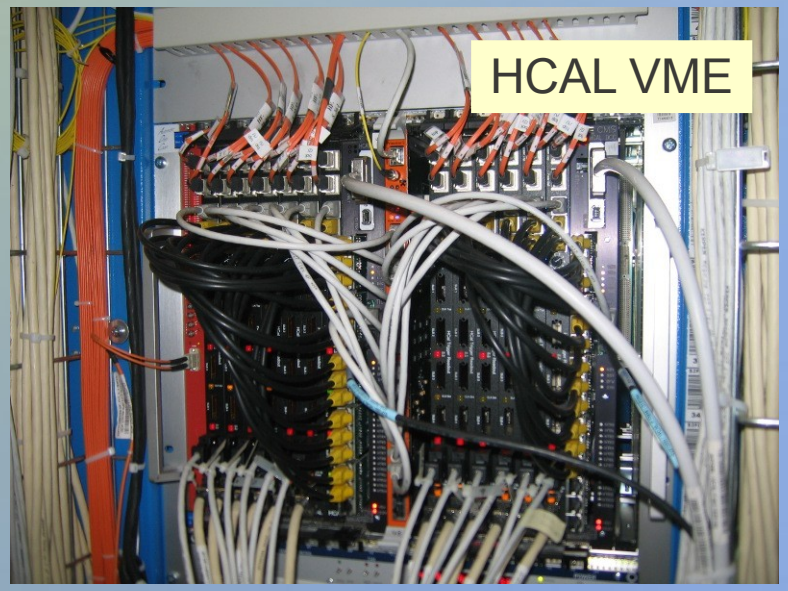
E. Hazen for the CMS Collaboration

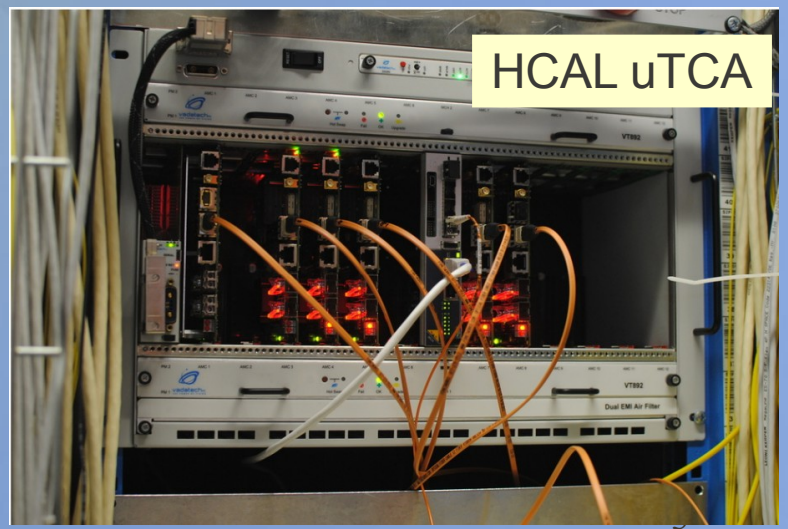
Outline

- Motivation
- MicroTCA Migration
- CMS MicroTCA Crate
  - Crate Overview
  - uHTR Module
  - The AMC13 Module
- HCAL Slice Test
- Summary and Plans

Migration to MicroTCA

- Reasons are by now well-known:
  - VME approaching end-of-life
  - Inadequate bandwidth
  - No clock/trigger support
- xTCA standards are a good fit
  - High-performance backplane
  - Low-latency/jitter paths possible
  - *but: complex infrastructure*
  - *boards are too small!*

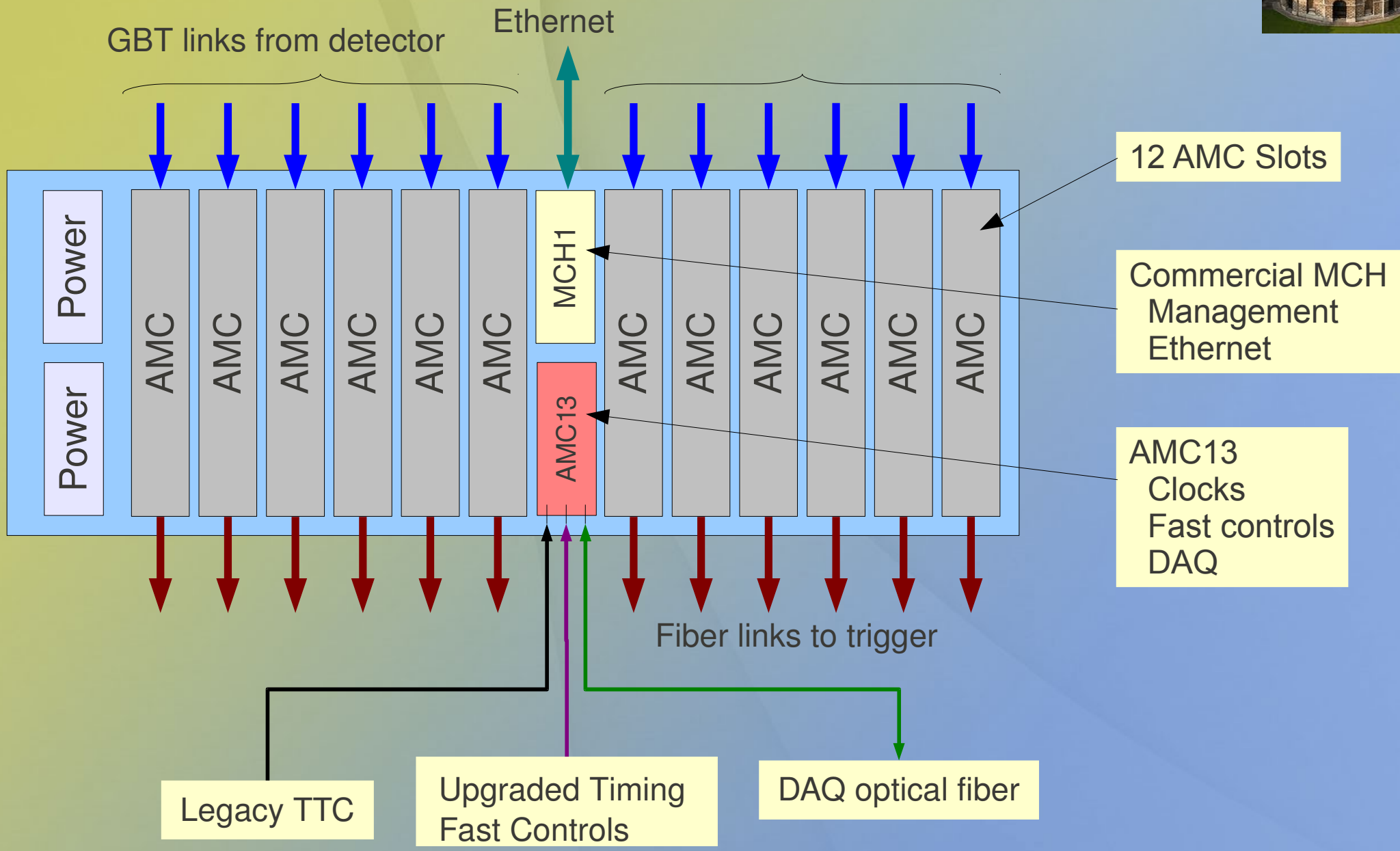




Upgrade Hardware Requirements
(Typical for all subdetectors)

- Distribute Clock, LHC timing, controls
  - Legacy (TTC) and (as yet undefined!) upgrade
- Process trigger backpressure (TTS) send to L1 trigger
- Process fixed-latency trigger data (local trigger)
- Collect DAQ event fragments and send to CDAQ

CMS uTCA Readout Crate (i.e. HCAL)



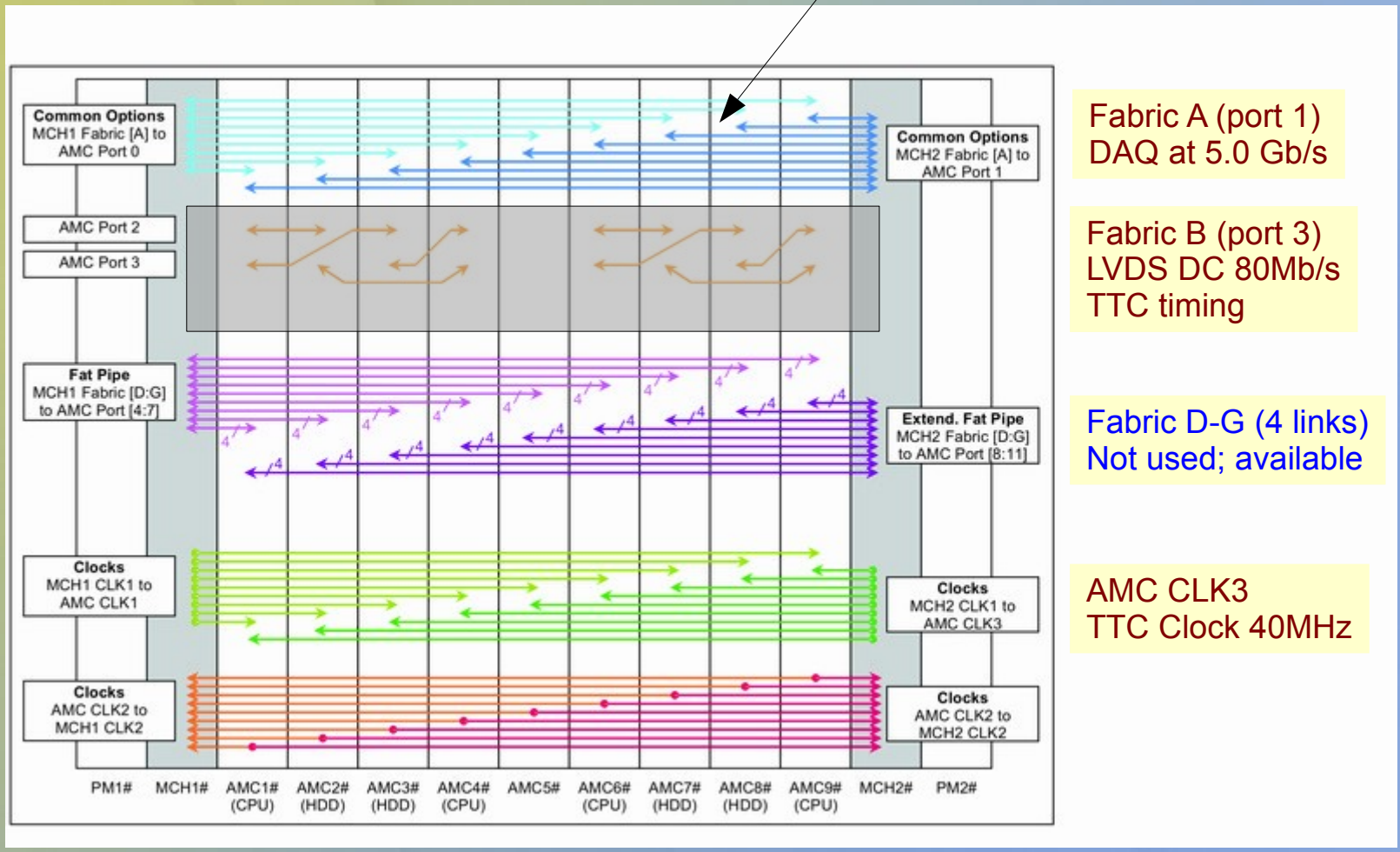
µTCA Dual-Star Backplane

Note: Interconnections can be customized by the backplane manufacturer inexpensively.

Bi-directional serial (up to 10Gb/sec) point-to-point links from each AMC to MCH (redundant links to each MCH)

Fabric A (port 0)
Gigabit Ethernet

Fabric D-G (4 links)
Not used; available



Fabric A (port 1)
DAQ at 5.0 Gb/s

Fabric B (port 3)
LVDS DC 80Mb/s
TTC timing

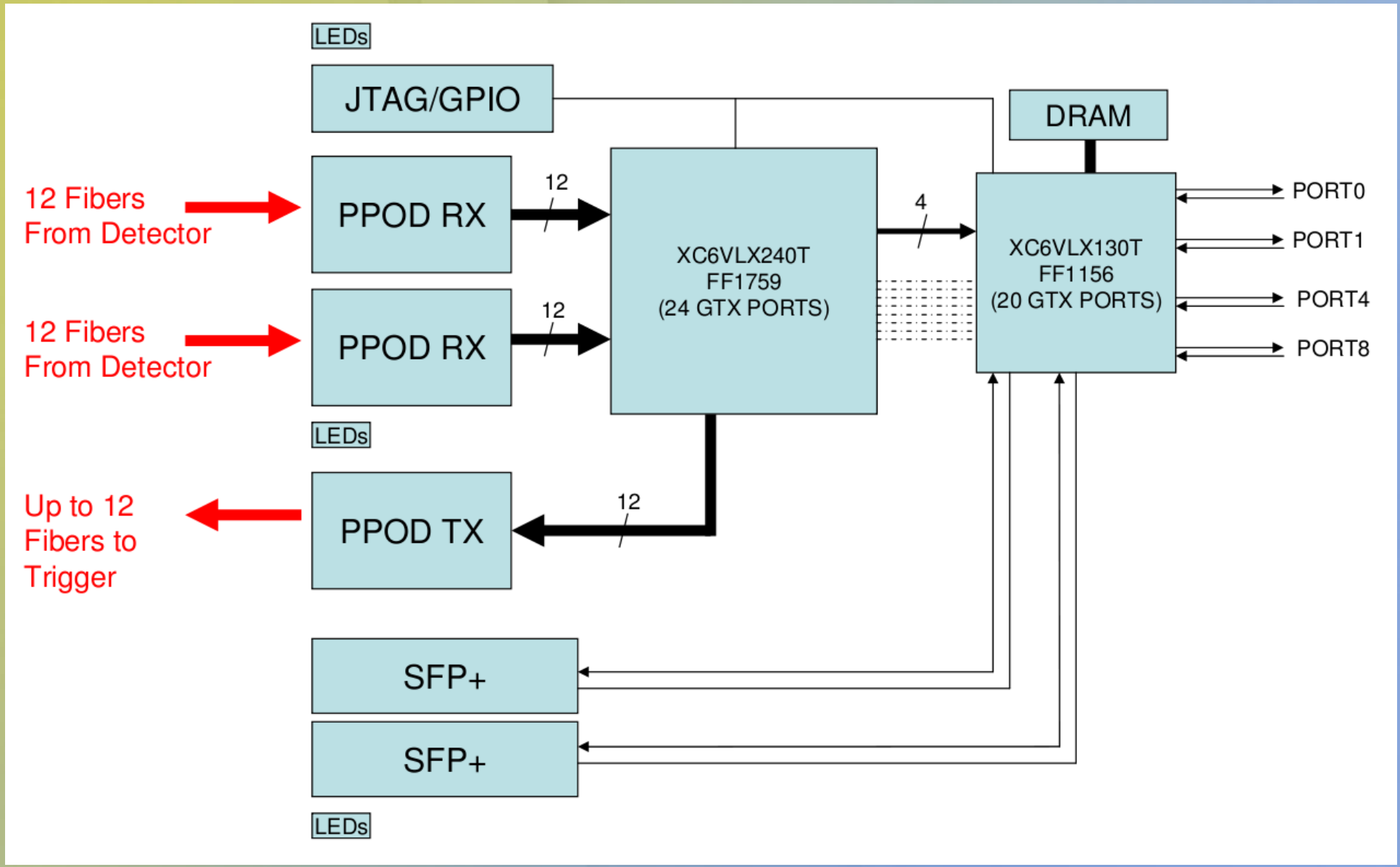
Fabric D-G (4 links)
Not used; available

AMC CLK3
TTC Clock 40MHz

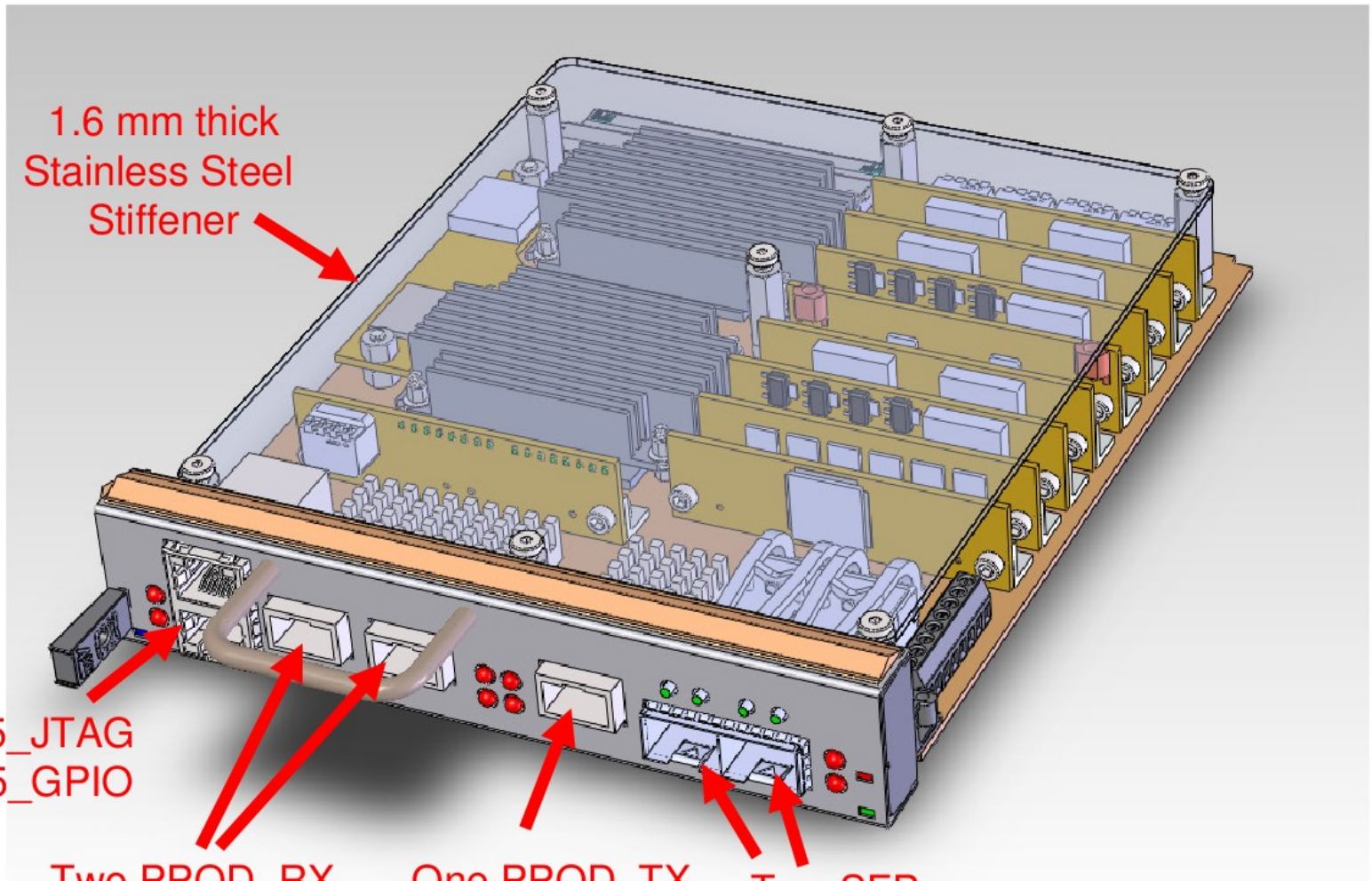
MCH 1 site
Commerical MCH

MCH 2 site
Our AMC13

uHTR – HCAL Trigger/Readout Card

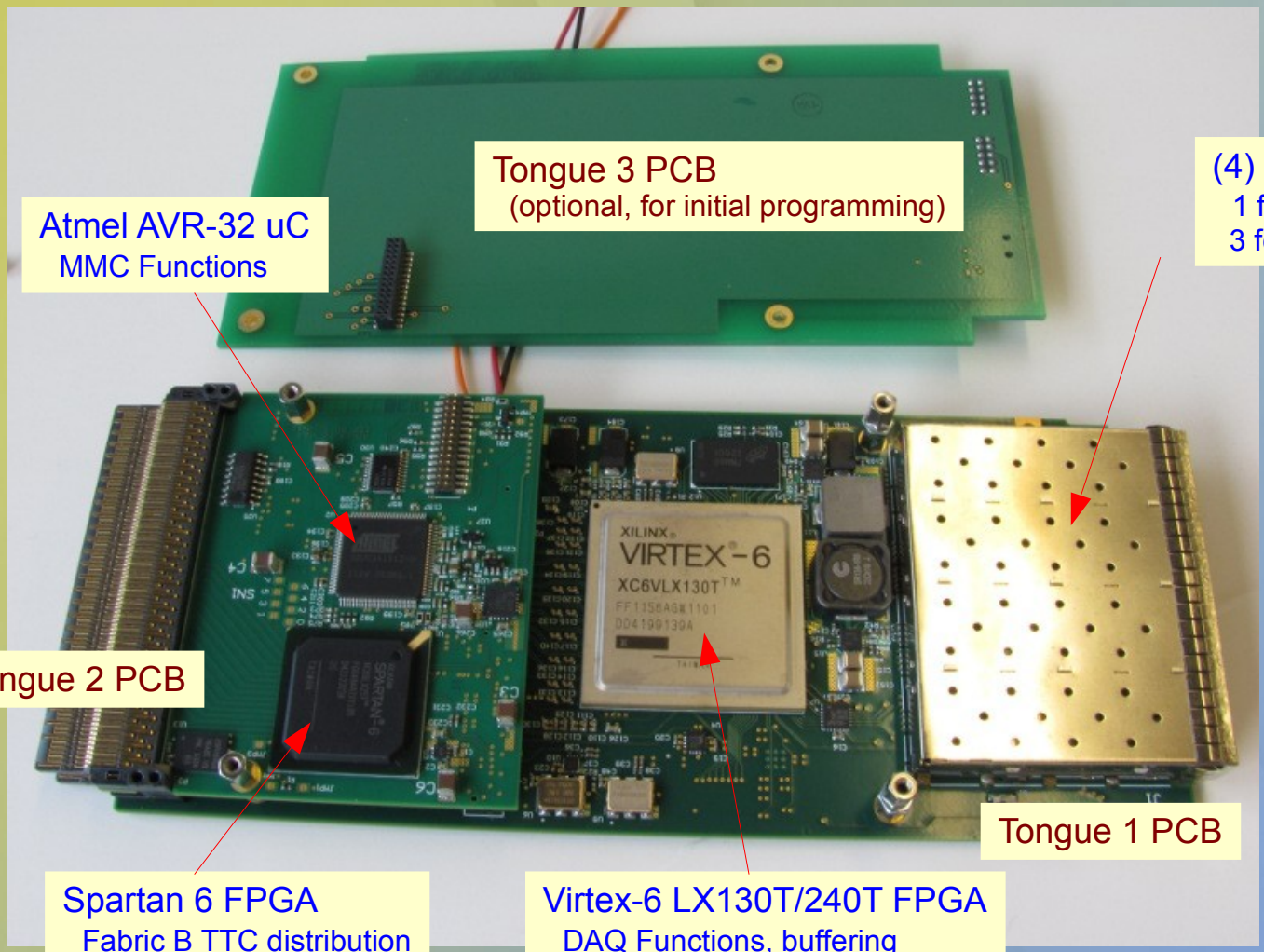


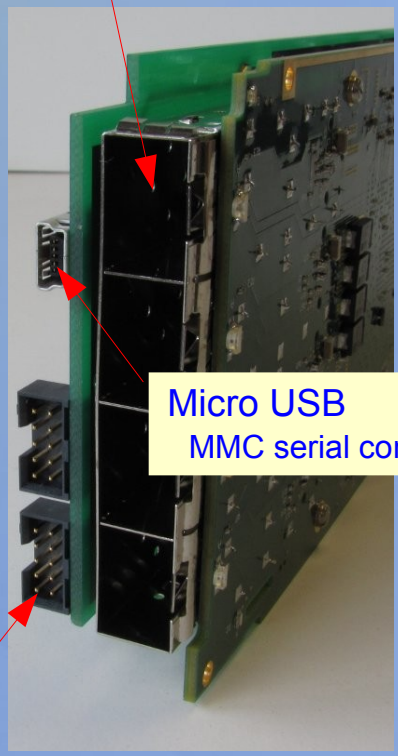
uHTR 3D Model
(layout is underway)



CMS AMC13 Module – Rev 1 (2010)

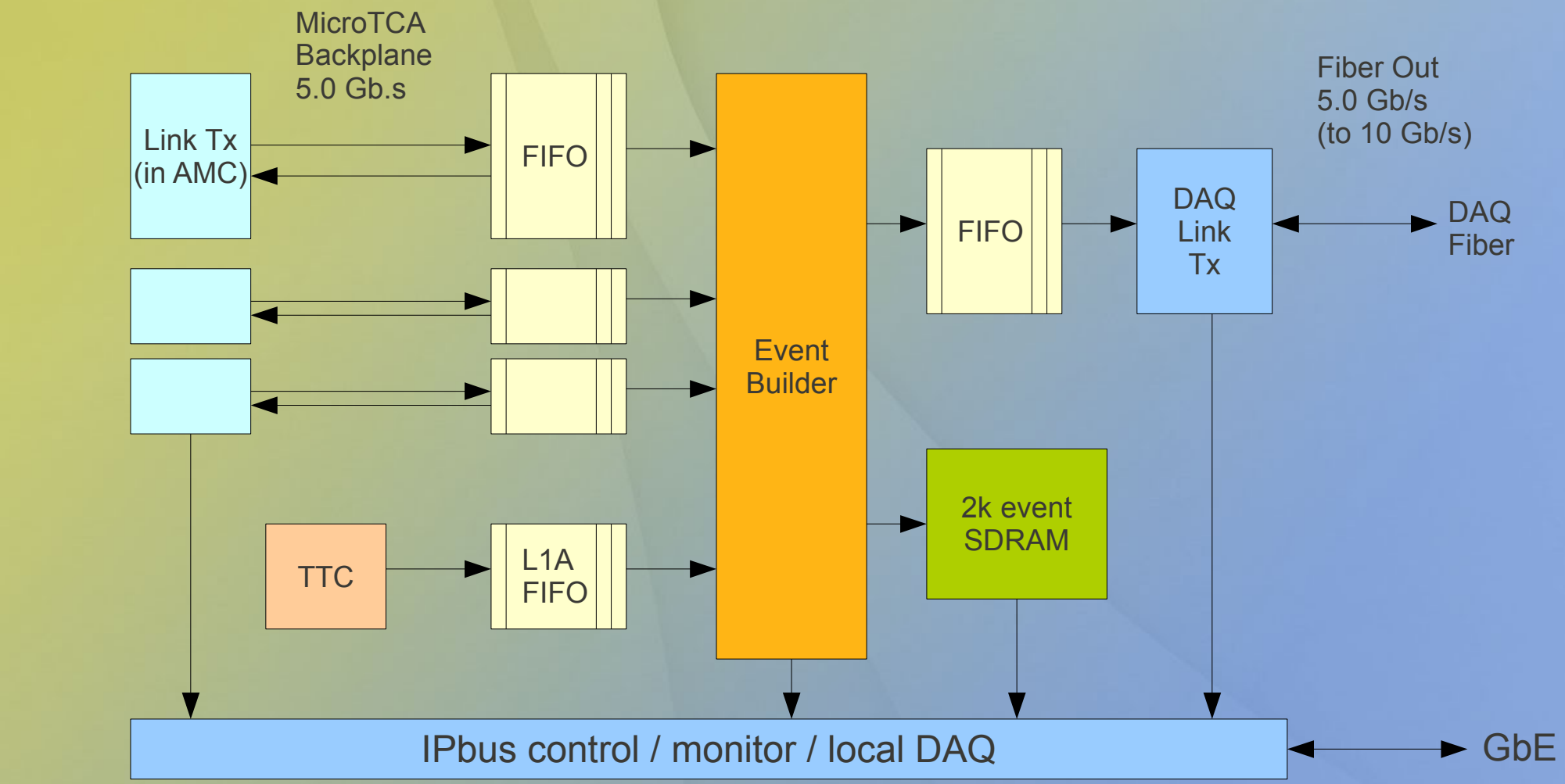
AMC13 Rev1 Hardware





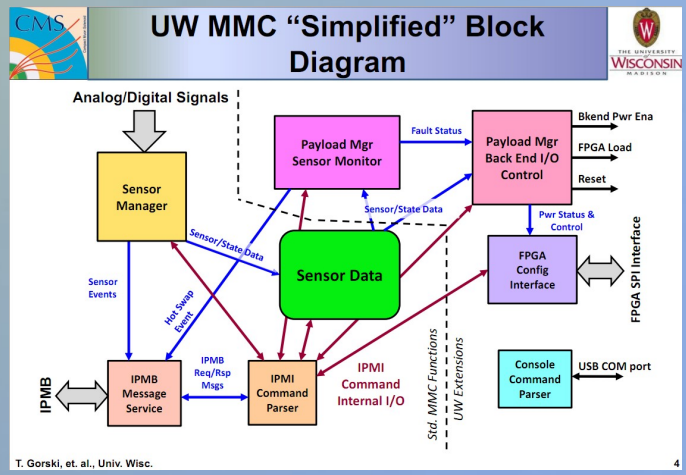
CMS AMC13 Module – Rev 2 (2012)

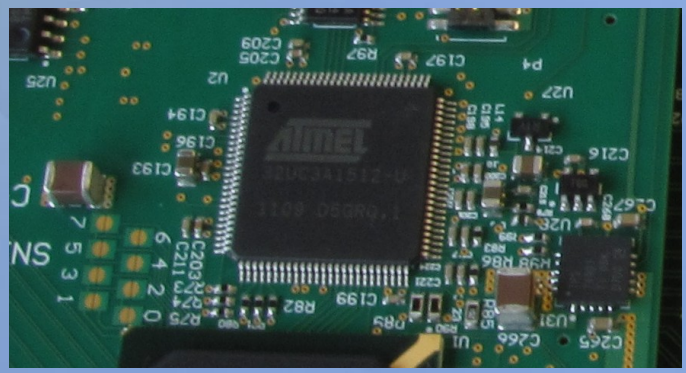
AMC13 Data Paths



AMC13 Technologies - I

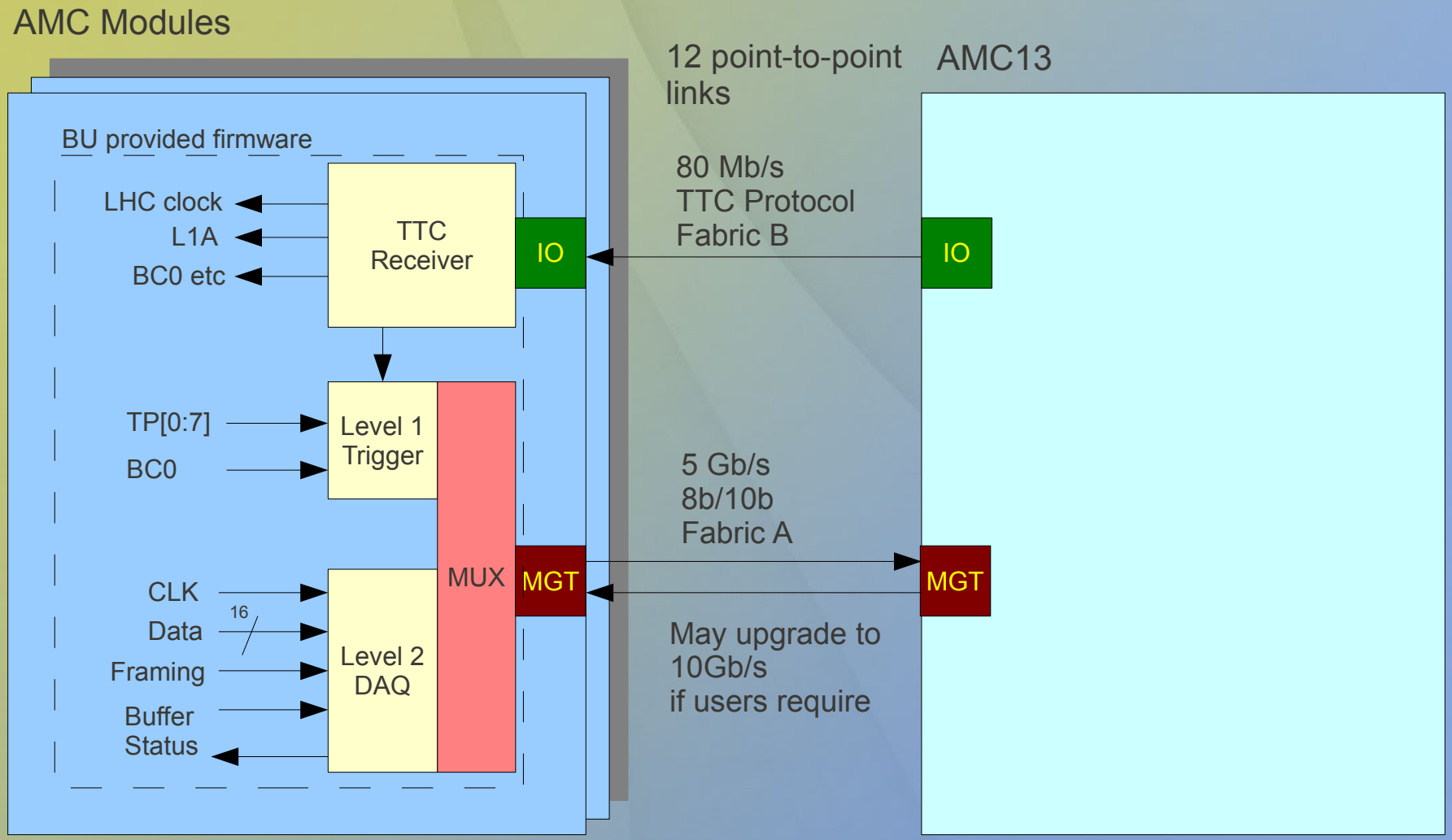
- MMC – Module management controller
  - Reference design provided by U. Wisconsin group
  - Features added to support CMS users:
    - Total of 16 analog sensors (V, T)
    - Digital inputs for Power Good, FPGA load done, FPGA Request
    - FPGA SPI Configuration path
    - Multi-stage Back-End Power Enable
    - IP address assignment scheme
  - MMC developed by a responsive collaborator is a huge win…





AMC13 Technologies - II

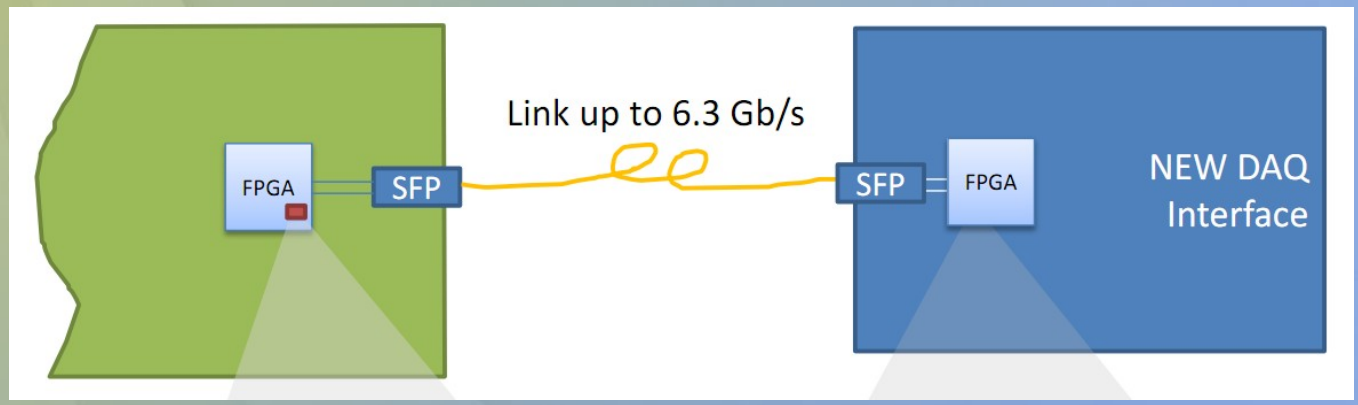
Backplane Link for TTC / DAQ from AMC to AMC13
Reference design including both ends of link provided

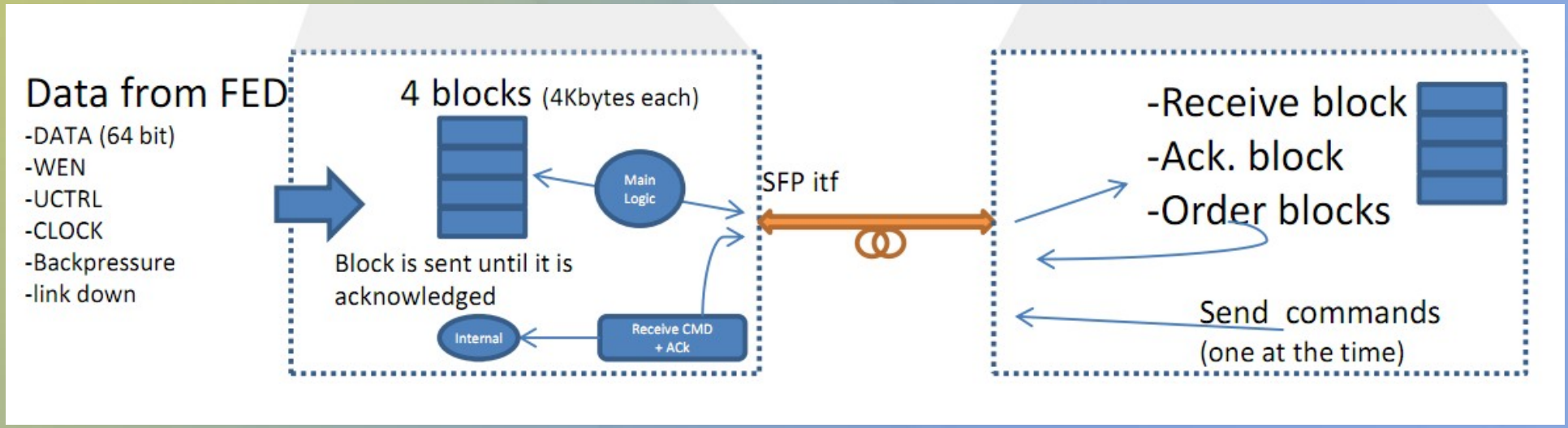


AMC13 Technologies – III

Fiber Link from AMC13 to CMS Central DAQ
S-Link work-alike link with error checking and retransmission
Both ends firmware developed by CMS CDAQ group

Under test, partially working as of conference date!





CMS xDAQ Support: HyperDAQ

Selectable level of detail

DTC Intermediate View

Other Views: Basic View Expert View Register Dump

Additional Filters: ☑ Nonzero Counters Only ☑ Enabled AMCs Only

Apply Filters

Date and Time	Ready Time	Run Time	Busy Time
Fri Sep 14 17:17:43 2012	00:00:30	00:00:30	00:00:00

Firmware Versions

Chip	Virtex	Spartan
Version	0x17	0xb

CONTROL0

Register	Value
DAQ Link Down	Y
DAQ Link Almost Full	Y
TTC BCNT Error	Y

CONTROL1

Control Bits	Value
Run Mode	1

EVB Counters

Counter	Value
SDRAM Word Ct	00000000 0000001a
Unread SDRAM Evts	00000000 000003ac
uHTR CRC Errors	00000000 00000004
LSCDAQ status	00000000 0000c1ac
TTC BC0 err	00000000 00000003
L1A Ctr	00000000 000003ac
Run time	00000001 0d7b4592
Ready time	00000001 0d7ae414
Busy time	00000000 00000001
L1A ovfl warn time	00000000 00000001
Tot evs monitored	00000000 000003ac

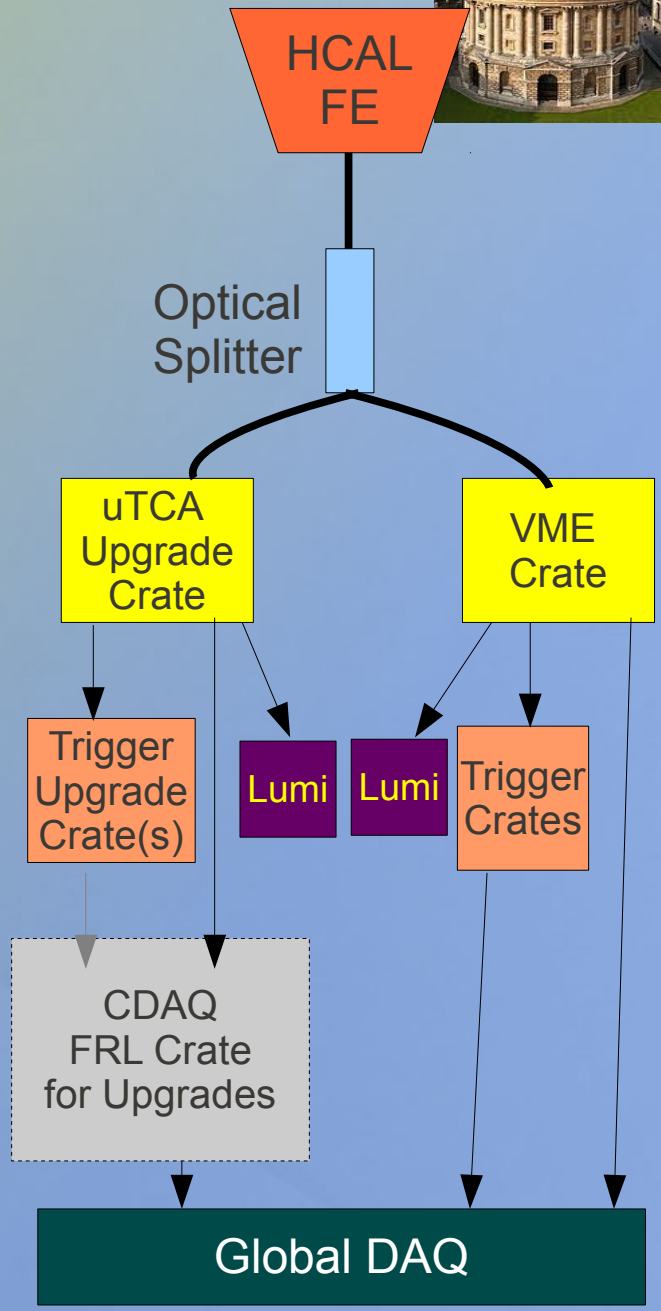
This page provides an overview of the operation of one AMC13. Color highlights various warning and error conditions in real time

First MicroTCA System at Point 5

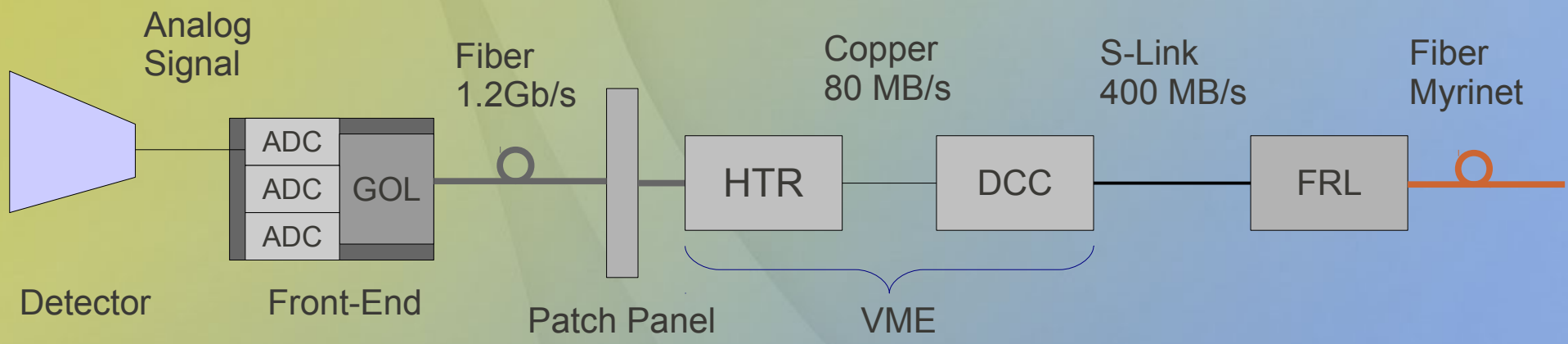
HCAL Slice Test

HCAL Parasitic Slice Test

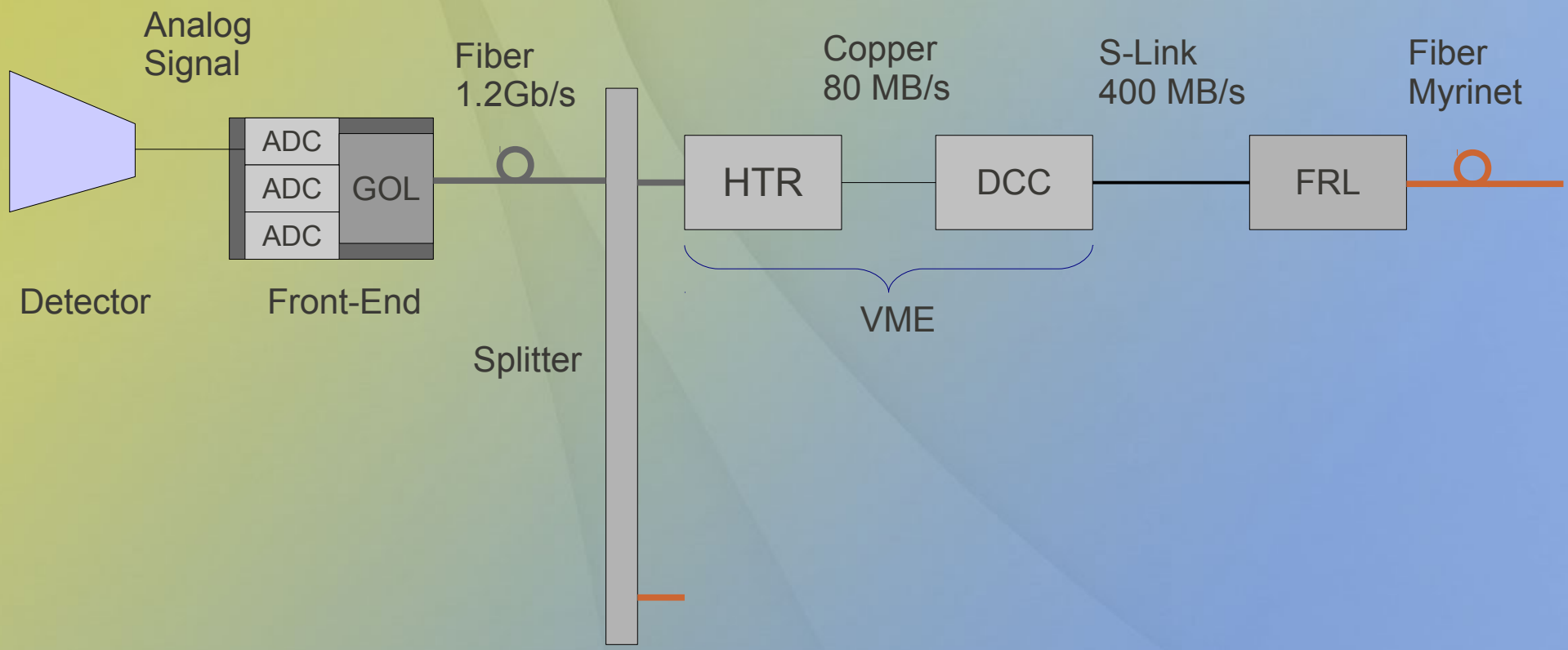
- Overall goal is to demonstrate uTCA electronics with full FE-CDAQ readout
- Use optical splitting on optical signal from the front-end (384 channels) to provide parallel current and upgrade branches
  - Cross-compare for validation
  - Trigger validation (P5 or B.904) for link stability tests
  - cDAQ validation at 100 kHz



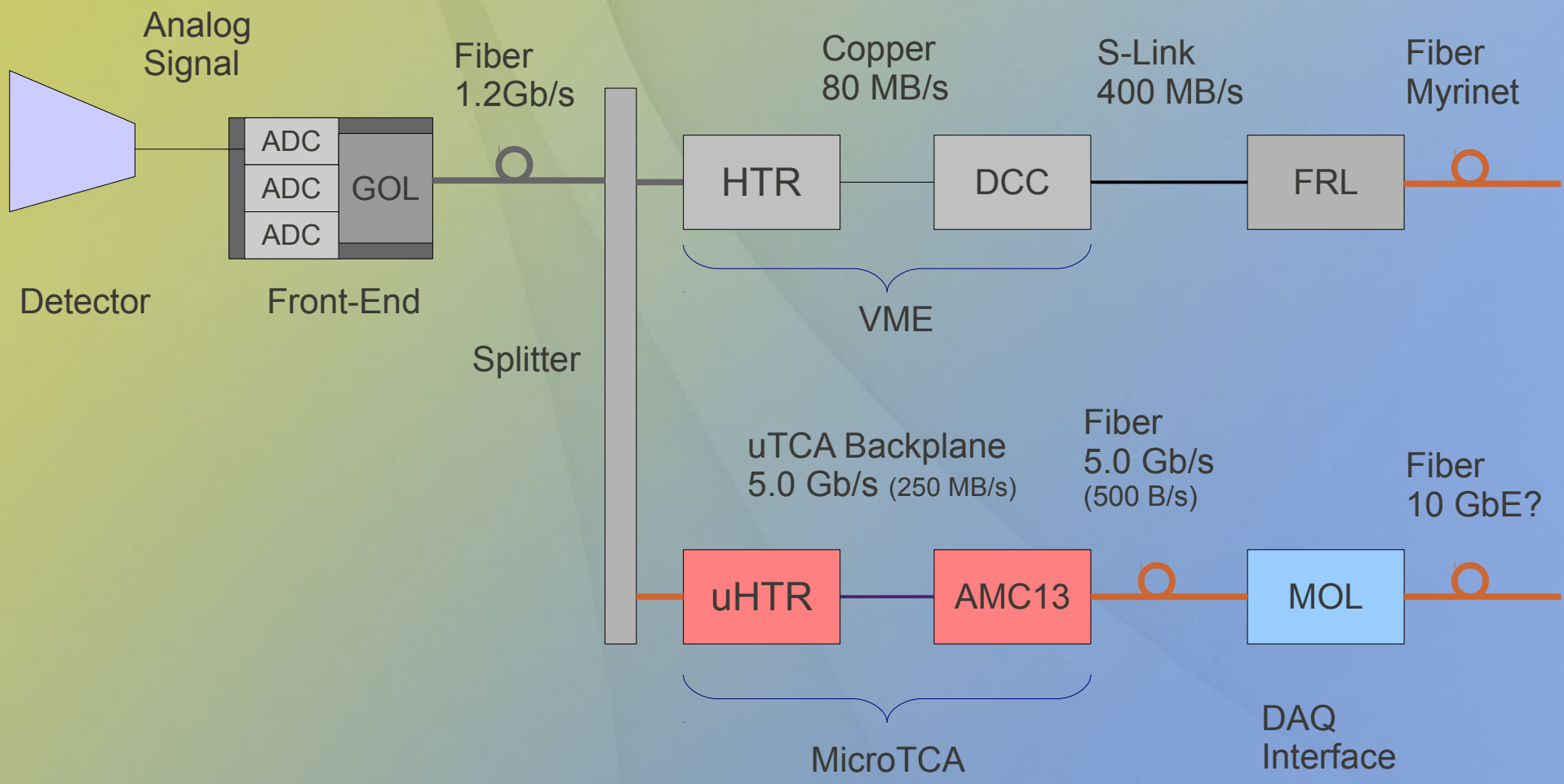
HCAL Readout – Original VME



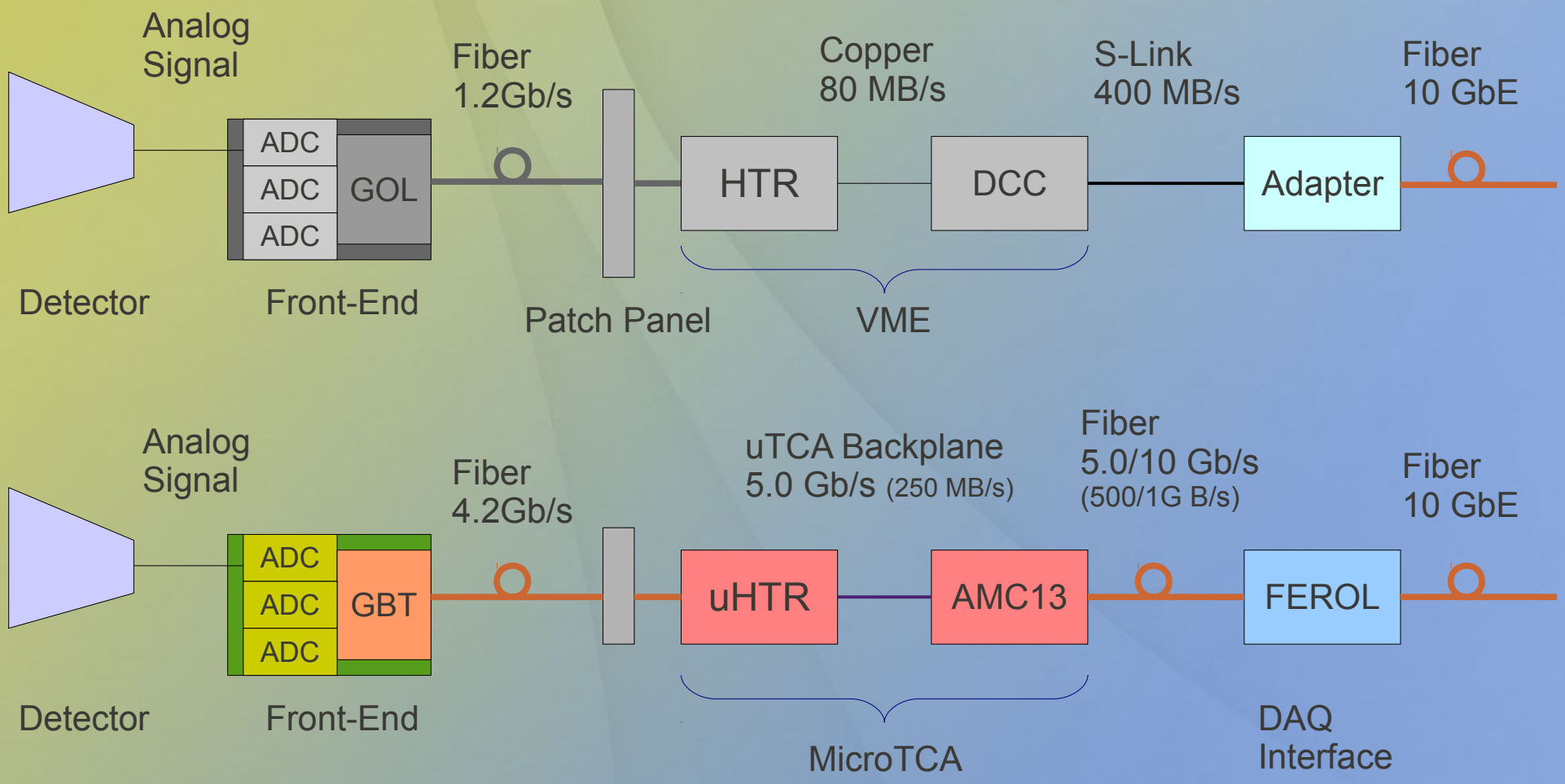
HCAL Readout – Add Splitter



HCAL Readout – Slice Test (now)

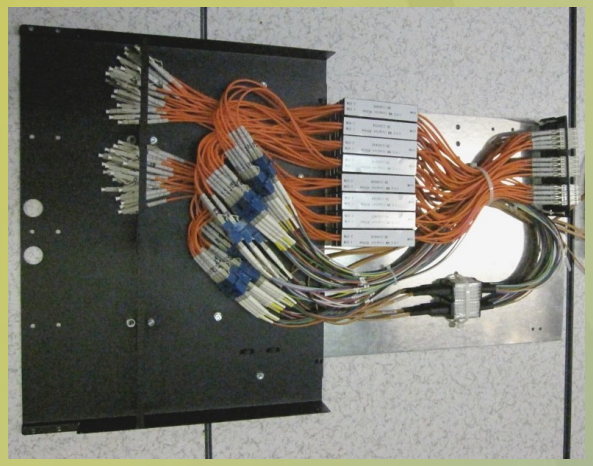


HCAL Readout – After LS1

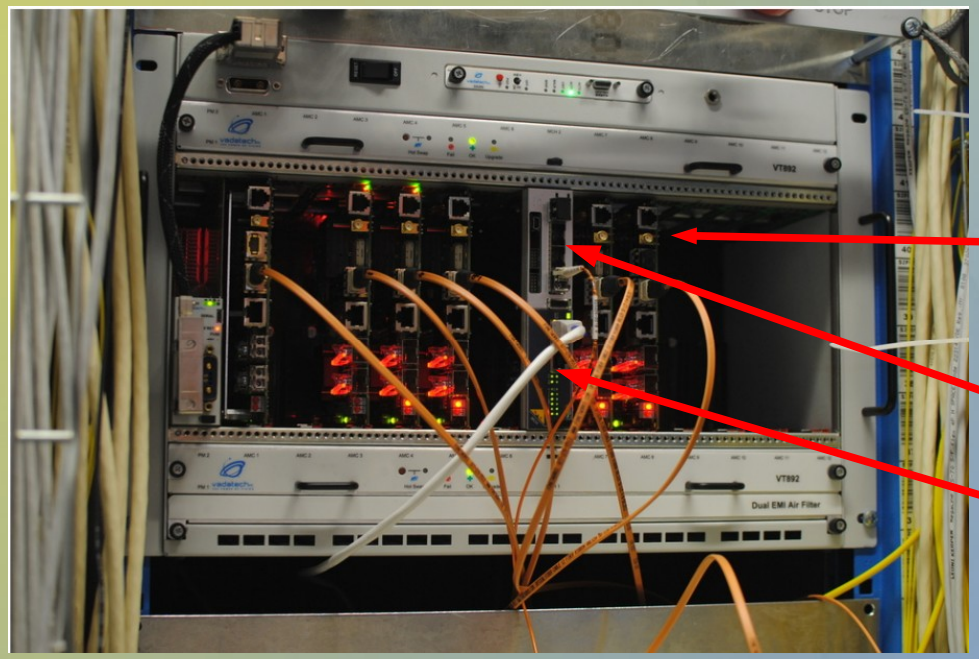


Disclaimer: Only HF – 3 crates out of 16 upgraded during LS1

Hardware Running at P5

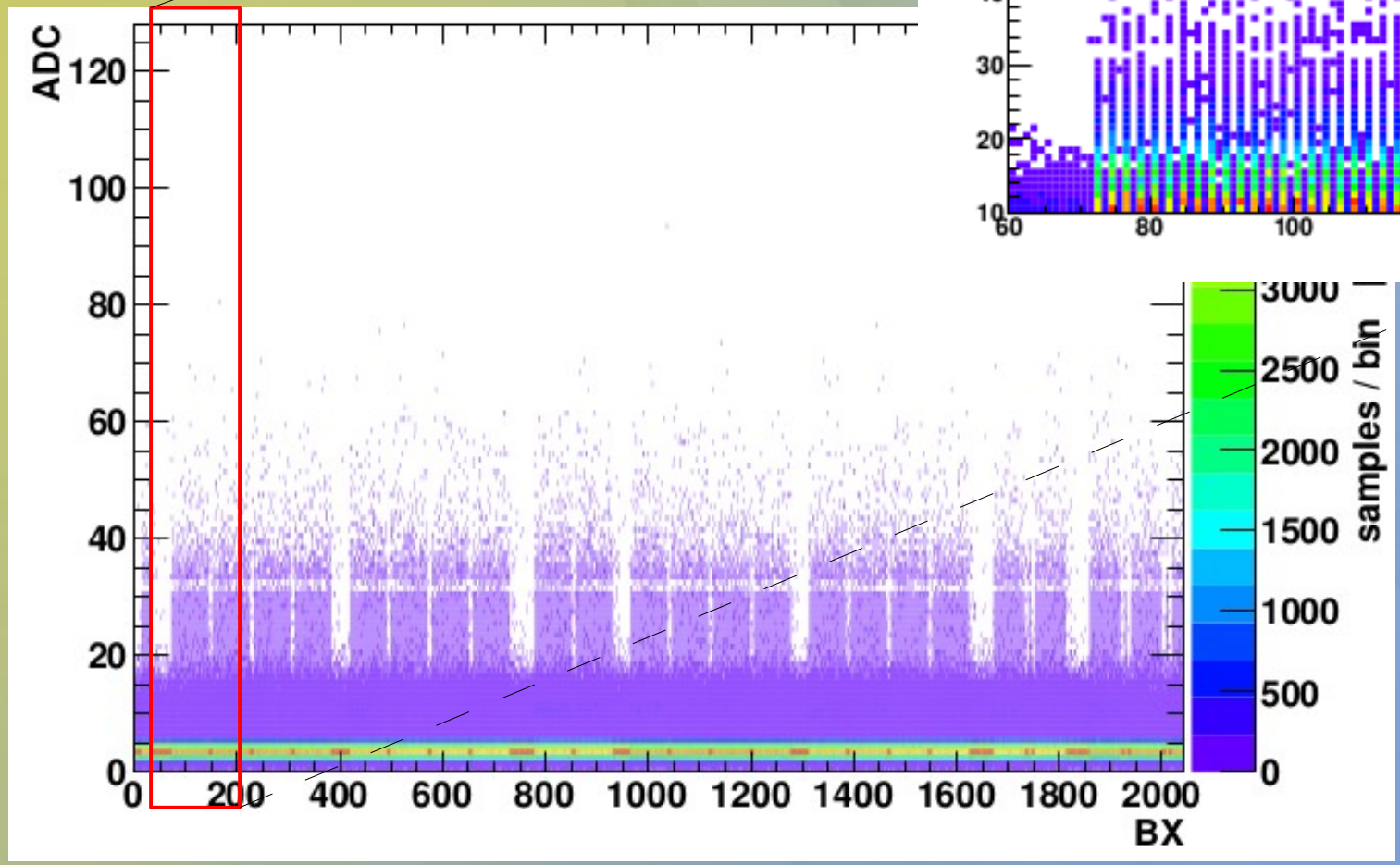


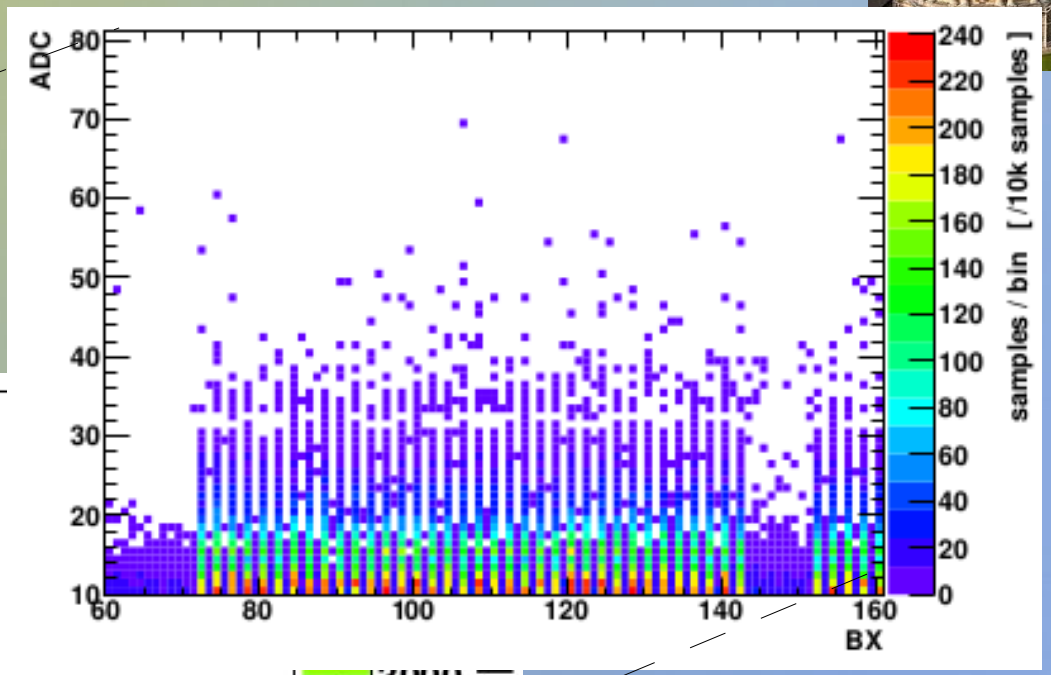
- 128 Optical splitters (384 channels) installed



- MicroTCA crate installed
  - 5 (soon 8) MiniCTR AMC modules
  - One AMC13 module
  - Commerical MCH

Early Success: Bunch structure seen in HCAL MicroTCA (HF data from fill 2627)





50ns structure clearly visible

Slice Test… so far

- Results so far:
  - Front-end link to uHTR – working
  - uTCA backplane link to AMC13 – working*
  - Fiber link to FEROL – working*
- Next Steps:
  - Debug uHTR/AMC13 firmware and link - underway
  - Implement DAQ test receiver in Xilinx – underway
  - Integrate at least one FED in CMS CDAQ
- Goal: full readout through CDAQ by end of 2012 run!

* The data is correct some of the time!

AMC13 Status and Plans

- Current Status
  - Working MicroTCA system installed at P5 in CMS (development continues)
  - 15 Rev 1 AMC modules produced and distributed
  - Layout of Rev 2 AMC13 design by end Sept (10Gb)
  - Firmware tested and working for TTC/clock distribution and basic DAQ with local DAQ over IPbus
  - Software support:
    - C++ class and command-line tools
    - CMS xDAQ HyperDaq web pages
    - Python (PyChips) diagnostic tools

Plans and Summary

- Plans:
  - Fabricate Rev 2 boards (10Gb links) – End of 2012
  - Finish commissioning end-to-end slice test at P5
  - Create xDAQ-free version of C++ support software

- Summary:
  - MicroTCA system installed at P5 under test
    - on track to read out collider data during current run
  - AMC13 generic timing/daq module produced
    - 2nd revision with 10Gb capability under design

Reserve

Towards a "Standard"

- Requirements document drafted in 2010
- Most CMS subdetectors will eventually upgrade to MicroTCA
- A common platform is proposed for most

CMS MicroTCA crate concepts & AMC card requirements.

Gregory Iles, Magnus Hansen, Tom Gorski and Eric Hazen
31 January 2011 Version 0.9 (Draft)

1 General concepts

This document describes a proposed CMS-specific configuration of a MicroTCA crate. It describes requirements for crate mechanics, backplane interconnections and some prescriptions for signal protocols on a few of the interconnections. It does not describe any software requirements, nor prescribe any particular implementation except as examples.

We have chosen to explore MicroTCA as a crate system to replace VME for the next generation of electronics cards inside the CMS experiment at CERN. MicroTCA offers a flexible, high density, high performance backplane that is based on the serial standards in use today (GbE, PCIe, SRIO, SATA, etc). It is relatively inexpensive for both the card manufacture and the customisation of the backplane if required.

MicroTCA is based on the AMC (Advanced Mezzanine Card) standard developed by the PICMG group for ATCA cards. Up to 12 AMC cards can be inserted directly into a MicroTCA backplane. A MCH (MicroTCA Carrier Hub) provides connectivity between slots, although direct connections between slots are also allowed. The system can operate in redundant mode with a second MCH (MCH2) connected to each AMC card and to the primary MCH (MCH1). For CMS we focus exclusively on this redundant type of "dual star" crate.

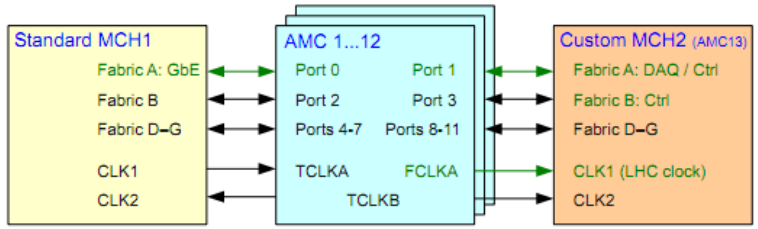


Illustration 1: Typical "Dual-Star" MicroTCA Backplane.
Note that each interconnection shown represents a "star" connection from each MCH to up to 12 AMCs. The Fabric connections are bidirectional (one pair each direction).

TTS Adapter and Test Module

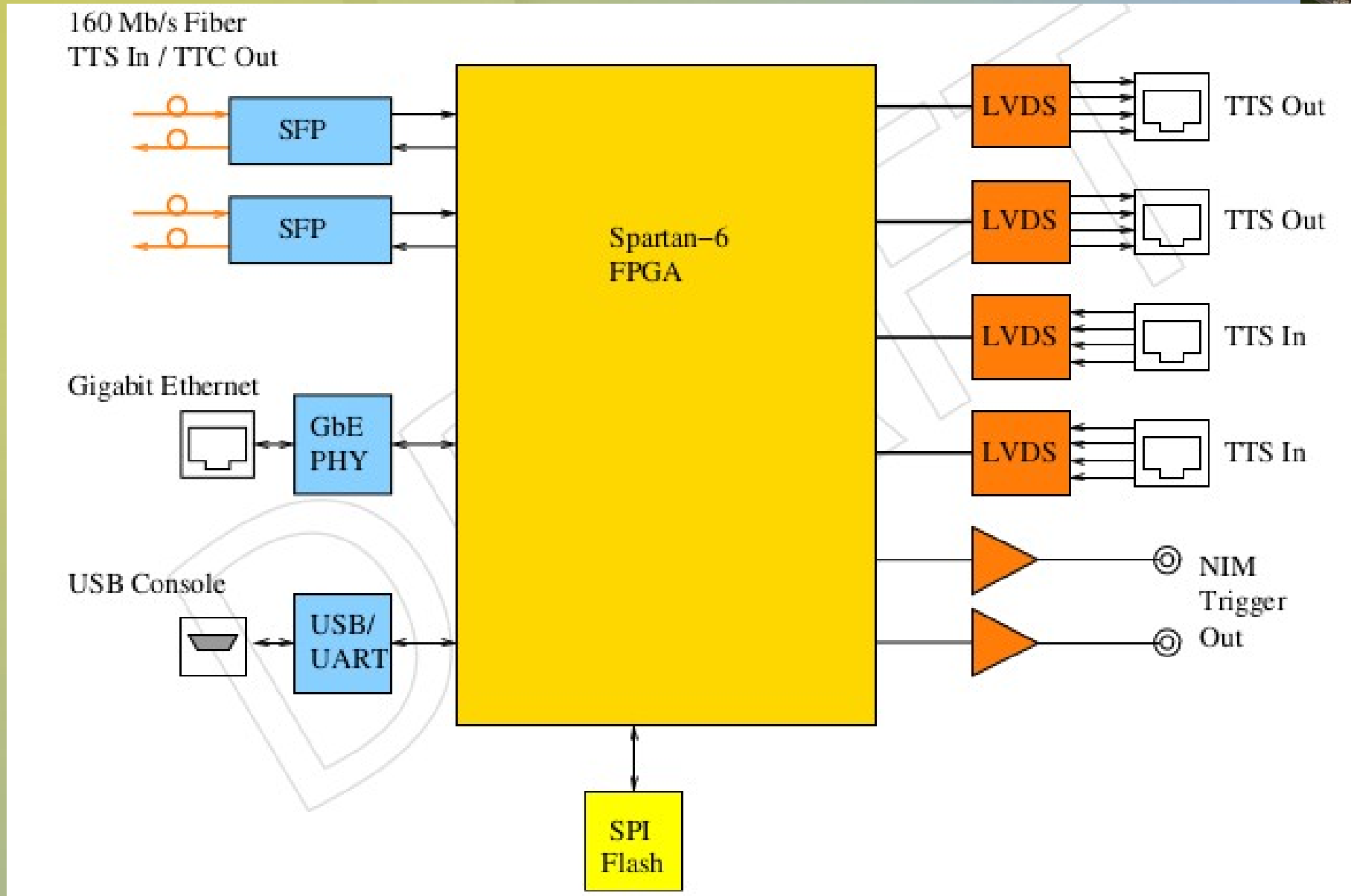
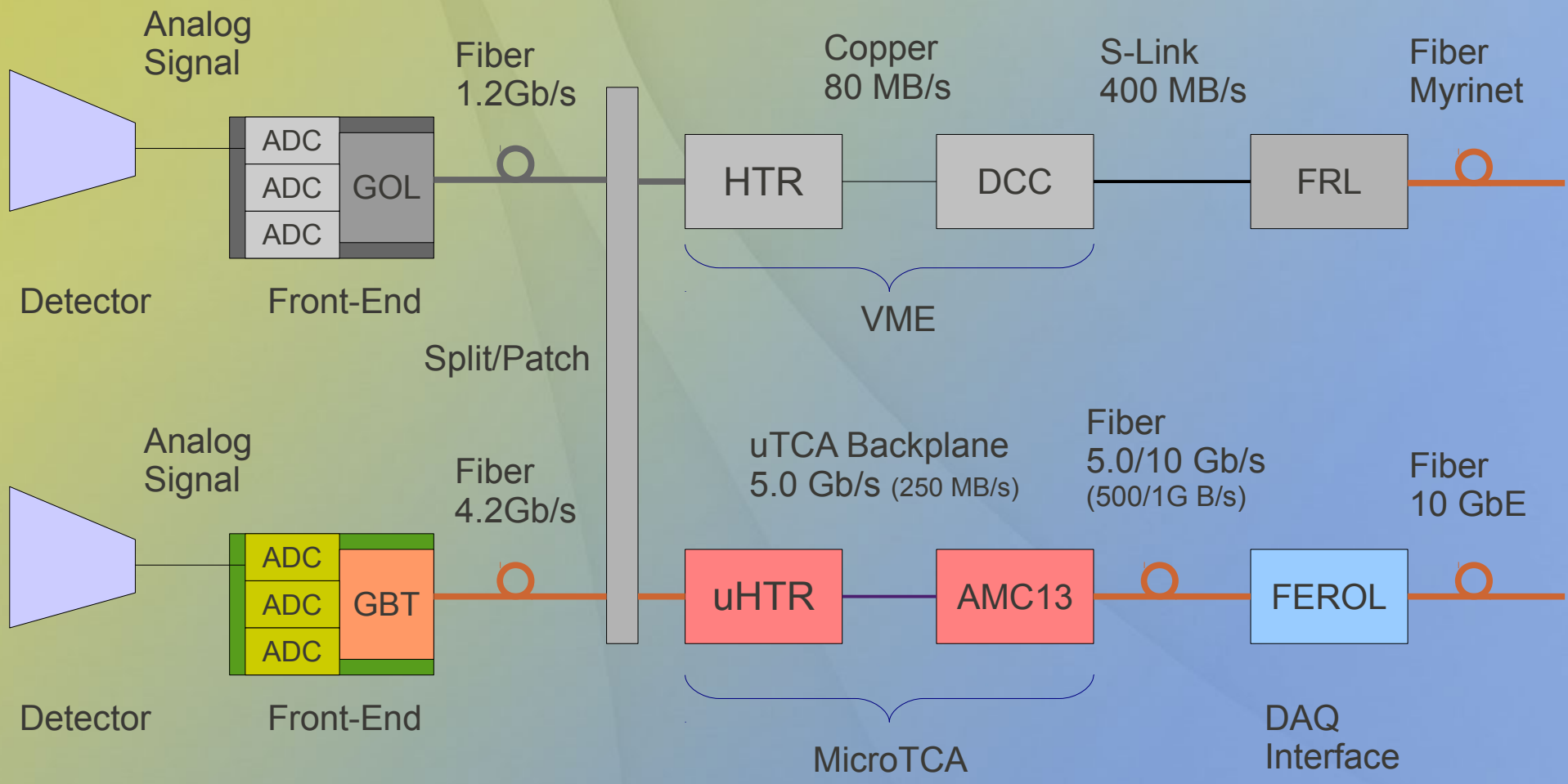
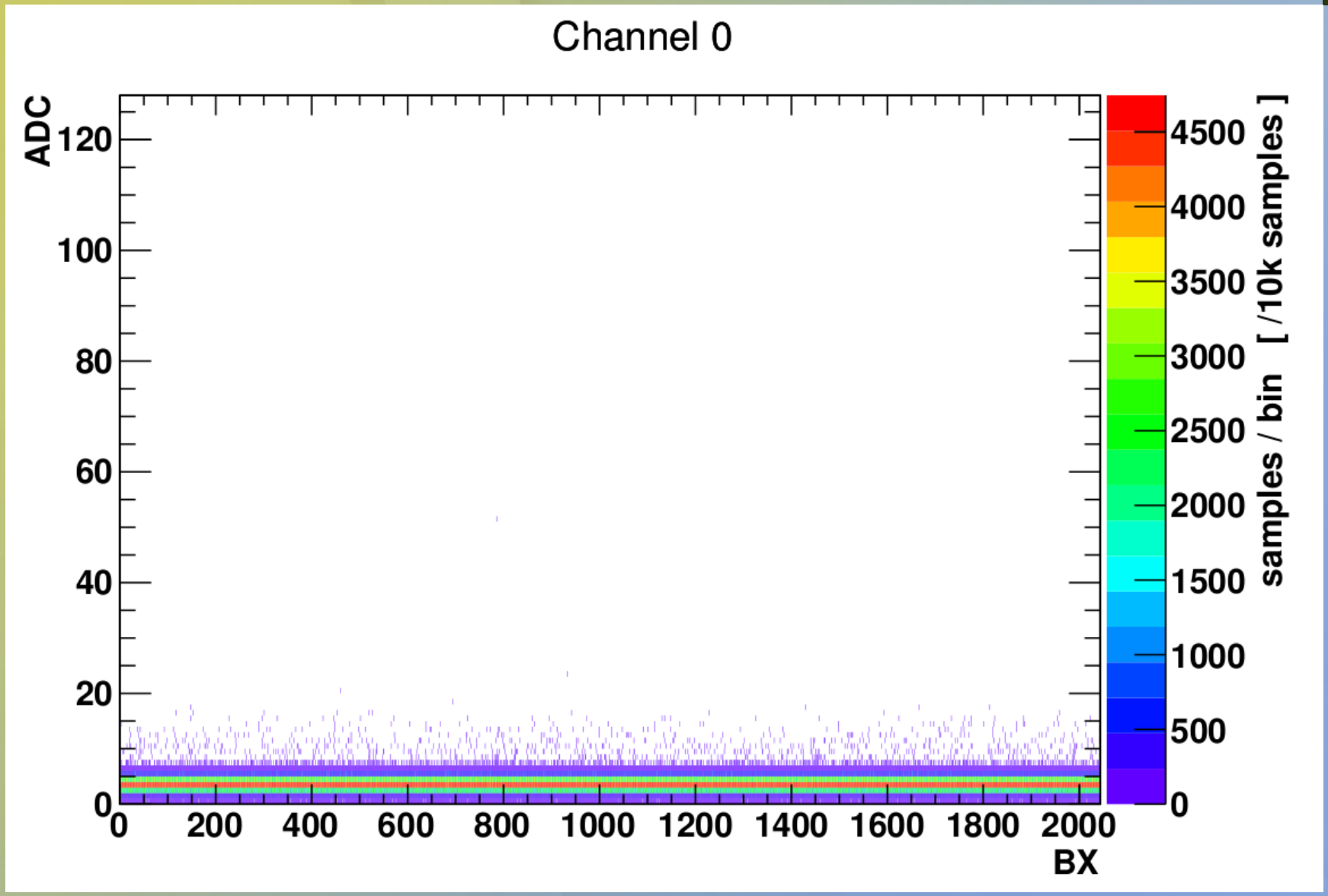


Figure 6.8: AMC13 TTS Adapter and Test Module

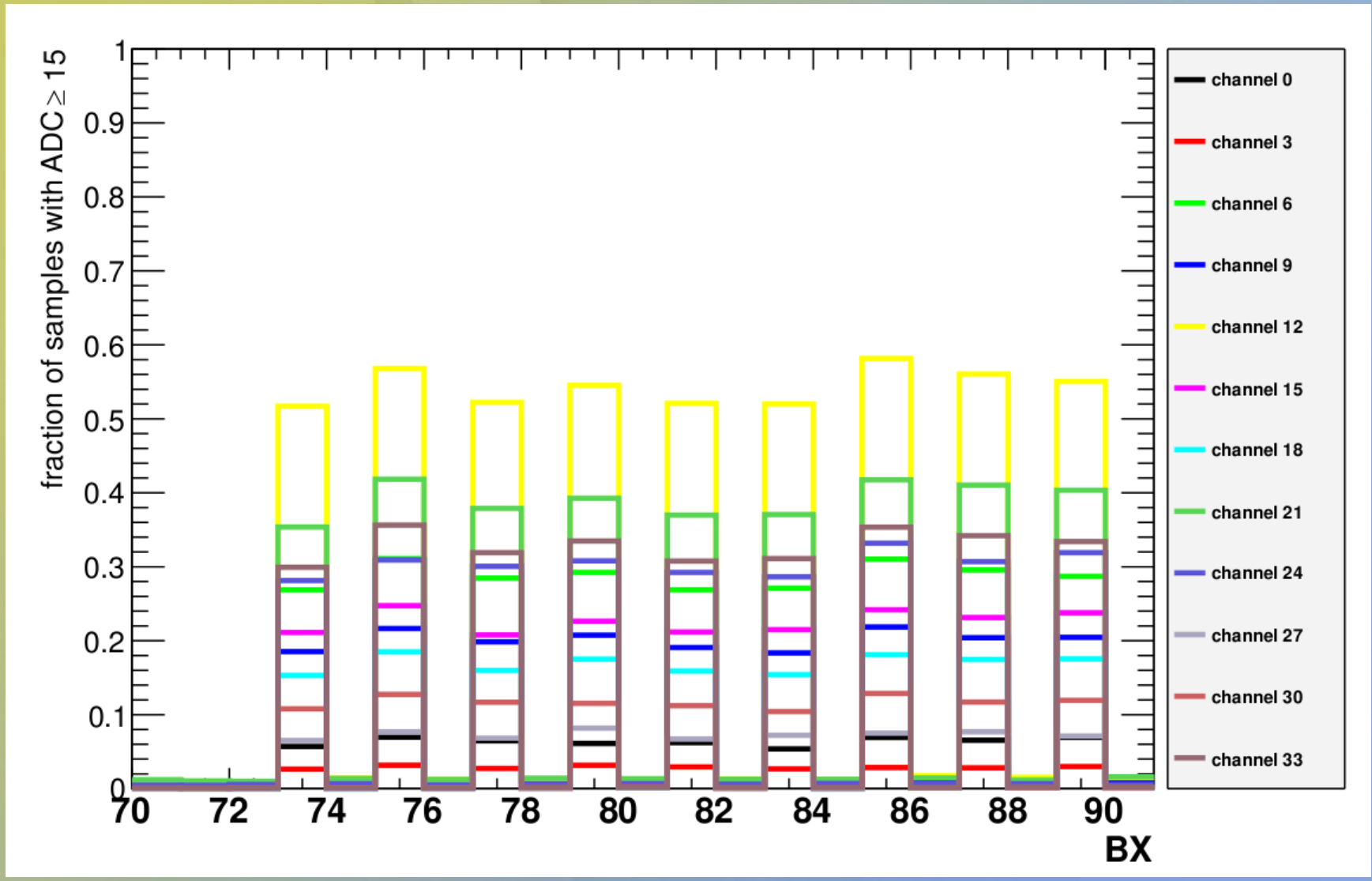
HCAL Readout Chain Upgrade



Control: Non-colliding beams (HF data from fill 2629)



Individual front-end fiber data are aligned within the MiniCTR MicroTCA module



Detailed diagnostic counters implemented for each AMC card link.

Mouse-over provides detailed description for each item

AMC Counters

AMC	04	10
Enabled	Y	Y
Link Working	Y	Y
Link Ver Bad	N	N
Port Not Synced	N	N
AMC Accept	00000000 000003ac	00000000 000003ac
AMC ACK	00000000 000003ac	00000000 000003ac
AMC EvN Mismatch	00000000 000003ac	00000000 000002d9
AMC OrN Mismatch	00000000 0000035b	00000000 00000200
AMC BcN Mismatch	00000000 00000001	00000000 00000001
AMC Received Ev	00000000 000003ac	00000000 000003ac
AMC Ctr ACK	00000000 00021844	00000000 00021899
AMC Ev CRC Error	00000000 00000004	00000000 00000000
AMC EvTrail EvN Mismatch	00000000 00000005	00000000 00000001
AMC Ev Buf near full time	00000000 17abb053	00000000 1809ecdf
Total Words	00000000 00002c30	00000000 00002c10
Resend	00000000 00000001	00000000 00000001
AMC13 Accept	00000000 000003ac	00000000 000003ac
Ctr Accept	00000000 00021848	00000000 0002189d
AMC13 ACK	00000000 000003ad	00000000 000003ad
Received Evts	00000000 000003ac	00000000 000003ac
Read Evts	00000000 000003ac	00000000 000003ac

Number of packets accepted by AMC13 from AMC (should be no. L1A)