FSP LHCb MEETING · YOUNG RESEARCHERS TALK

Quality-Assurance Test Stand for LHCb Mighty Tracker Fibre Mats

SiPM readout with oscilloscope, SPIROC and FastIC at RUB

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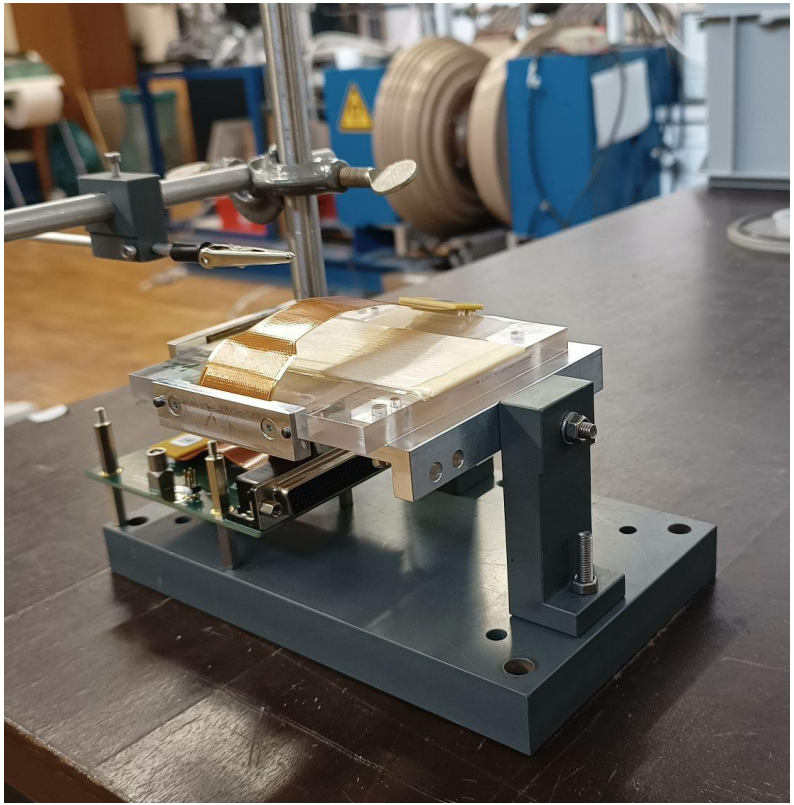
Overview

1. **Motivation**
   LHCb Upgrade II and the Mighty Tracker
2. **Stage 1: Oscilloscope reference**
   Black box, EPFL detector, light pulser, analysis
3. **Stage 2: SPIROC readout**
   Setup, software and the adapter problem
4. **Stage 3: FastIC readout**
   Why FastIC and current status
5. **Summary & outlook**



EPFL fibre-mat detector in the RUB test setup

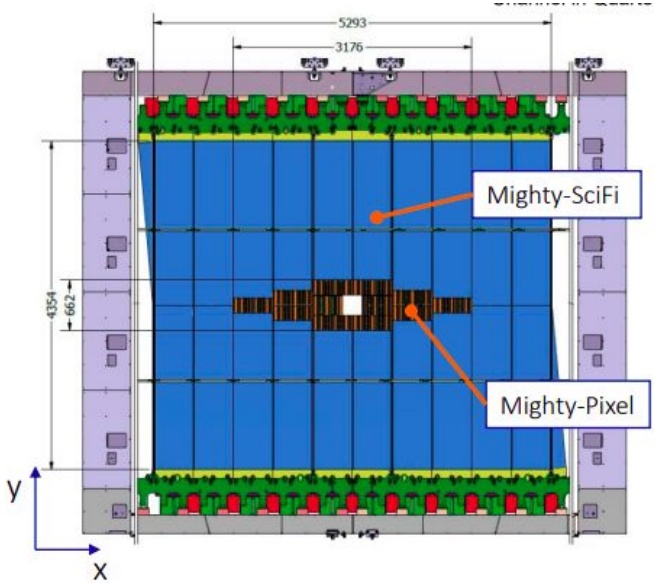
Motivation: LHCb Upgrade II

1. **Long Shutdown 4:** LHCb Upgrade II prepares for up to 1.5×10^{34} $cm^{-2}s^{-1}$

2. **SciFi → Mighty Tracker:** silicon pixels in the high-occupancy inner region, new scintillating-fibre mats outside

3. **New fibre mats** must be qualified and quantified before installation

4. **At RUB:** a QA test stand for fibre mats. My master thesis starts this effort.

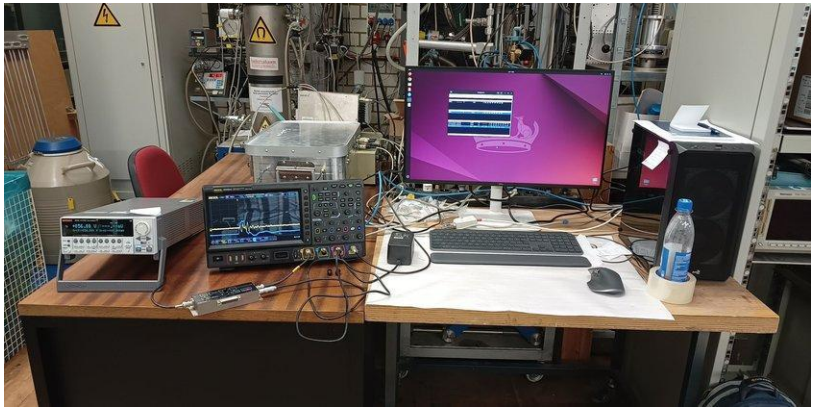


One tracking layer, schematic (not to scale)

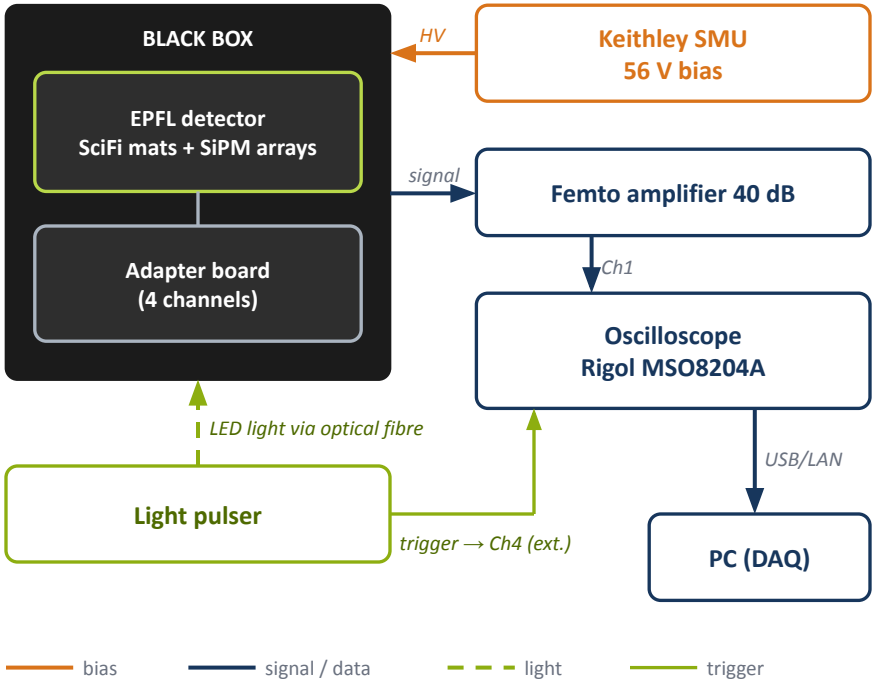
New fibre mats → QA test stand at RUB

Stage 1: readout with an oscilloscope

Stage 1 · Setup



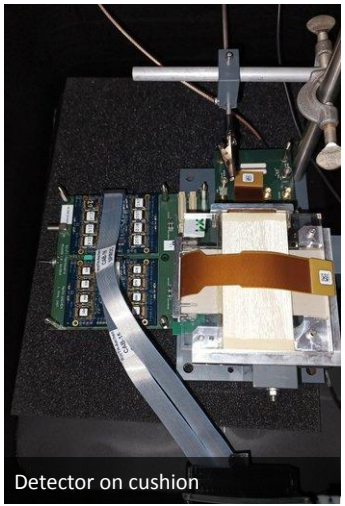
- EPFL detector biased at 56 V (Keithley) through the adapter board
- 4 channels can be read out individually
- Signal ⟶ Femto amplifier (40 dB) ⟶ oscilloscope
- LED pulses reach the mat via optical fibre; the pulser trigger is the external scope trigger
- PC reads out the scope: ~20 000 waveforms per run

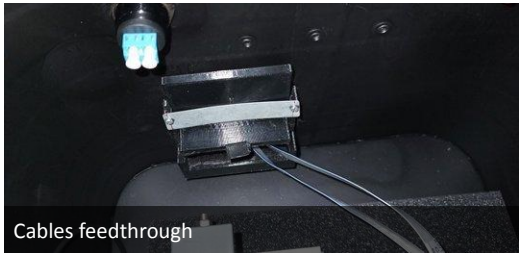


The black box

Closed, cables via window

Opened


Detector on cushion


Cables feedthrough

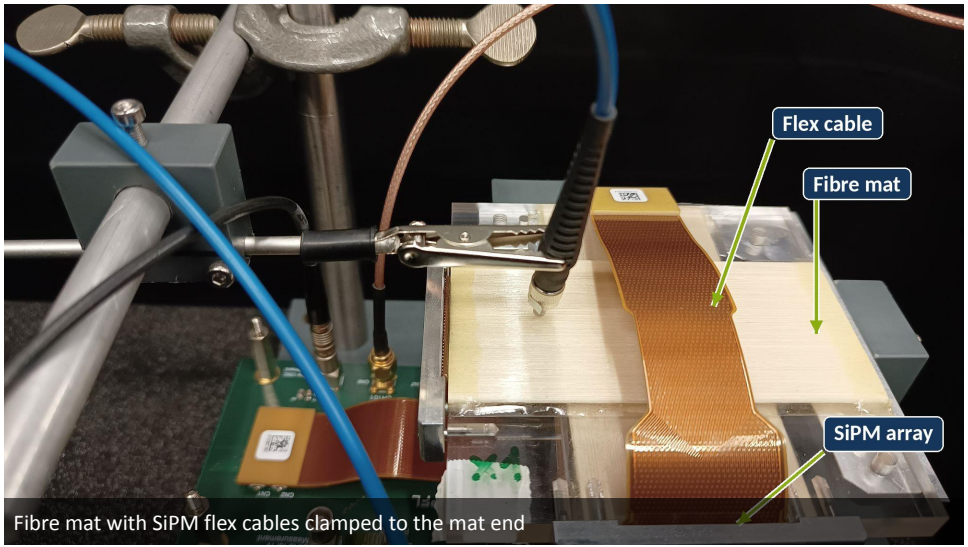
Corners sealed with black sealant

44 × 30 × 23 cm

aluminium box, keeps the SiPMs in the dark

Feedthroughs: LEMO, SMA and optical-fibre adapter
Cable window closed by a light-tight 3D-printed part
Inside: matte black paint; small corner gaps sealed with black light-tight sealant
Black cushion holds the detector setup steady

The EPFL detector



Fibre mat with SiPM flex cables clamped to the mat end

Mounted detector

EPFL adapter card (IV + single channel)

10 × 4.5 × 0.3 cm

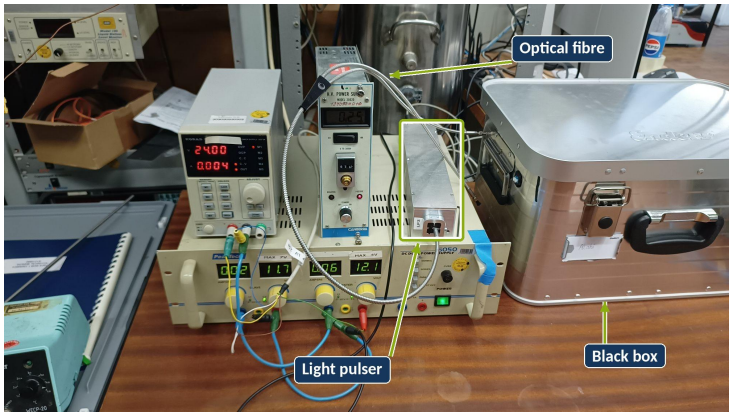
per scintillating-fibre mat

Provided by EPFL

Two fibre mats glued on both faces of a square acrylic plate
SiPM arrays with flex cables, fixed to the mat ends with clamps and screws
Adapter card for IV measurements and single-channel readout

Light pulser system

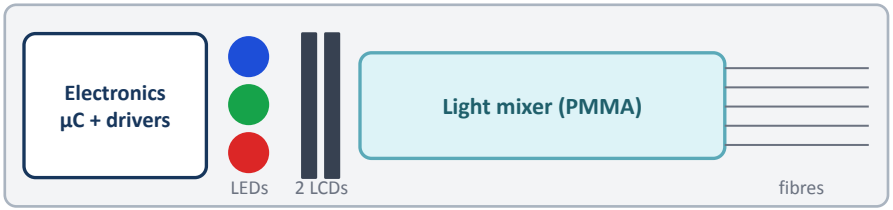
Stage 1 · Setup



Light pulser with supplies next to the black box

Pulser electronics and LED board (from PANDA thesis)

Inside one pulser module



Built at RUB (EP1) for the PANDA calorimeter, to monitor radiation damage of the crystals
Three LEDs (blue, green, red) with fast drivers, controlled by a microcontroller
Two crossed LCDs tune the intensity (contrast ≥ 1 : 1000)
Light mixer (18 × 18 × 150 mm³) spreads the light evenly into many optical fibres

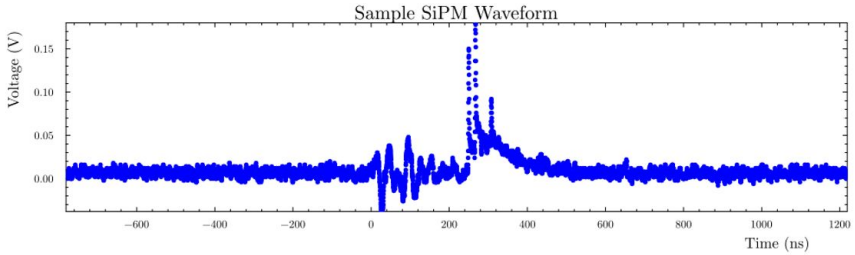
SiPM signal: from scope to dataset

Stage 1 · Analysis

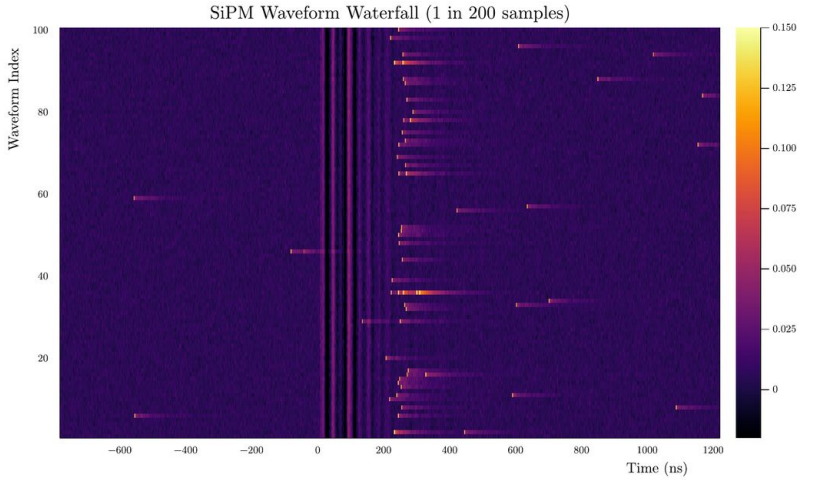
Live on the scope

Ch1 (yellow): amplified SiPM signal

Ch4 (blue): pulser trigger



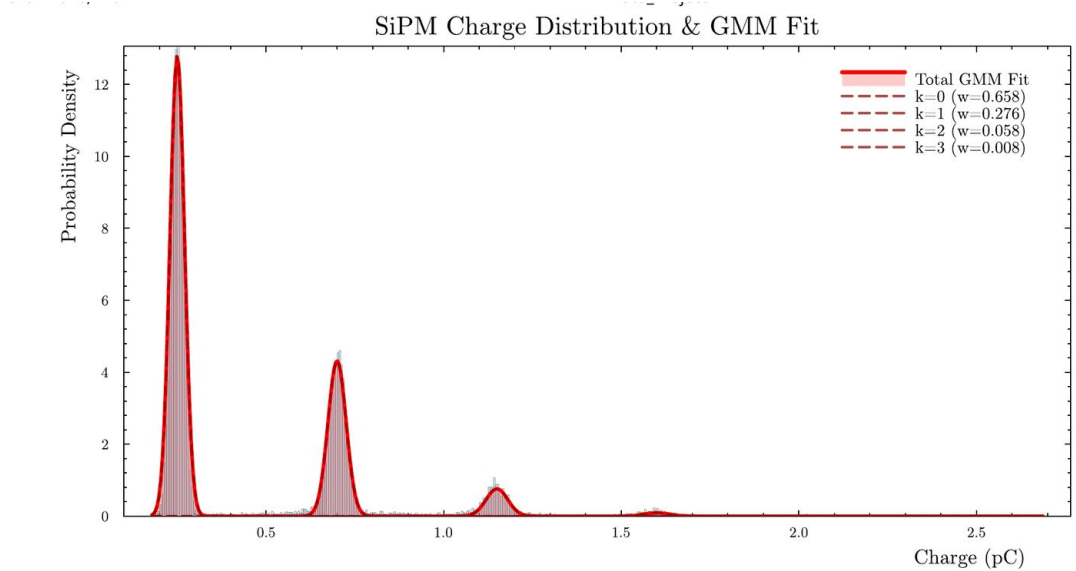
One recorded waveform (random pick out of 20 000)



- Stable baseline and electronic noise
- Pulses arrive ~250 ns after the trigger at a consistent time
- Little pile-up: integration window 200–400 ns

Charge spectrum: single-p.e. resolution

Stage 1 · Result



$P(Q) = \Sigma_k \, \mathrm{Pois}(k; \lambda) \cdot N(\mu_0 + k\Delta\mu, \sigma_0 + k\Delta\sigma)$

peak k = number of photoelectrons

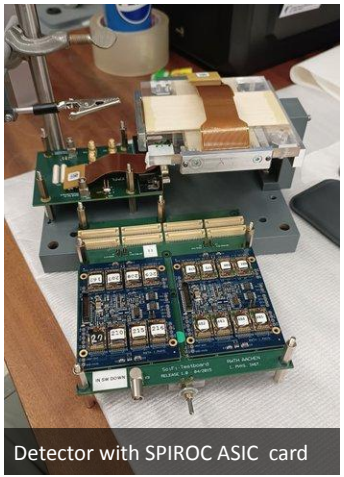
$\lambda \approx 0.42$ mean p.e. per pulse	$\Delta\mu \approx 0.45$ pC charge per p.e.
$G \approx 2.8\times10^6$ SiPM gain ($\Delta\mu$ / e)	$\sigma_0 \approx 0.02$ pC pedestal width

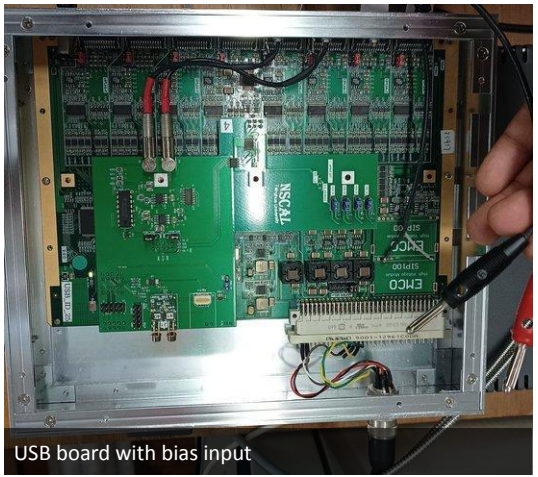
V / 100 (40 dB amp.) › I = V / 50 Ω › $Q = \int I\,dt$ 200–400 ns › Poisson-weighted Gaussian fit

Evenly spaced peaks with Poisson weights → the reference for SPIROC and FastIC

20 000 waveforms, 56 V bias; fit parameters tuned interactively

Stage 2: SPIROC readout and software


Detector with SPIROC ASIC card


USB board with bias input

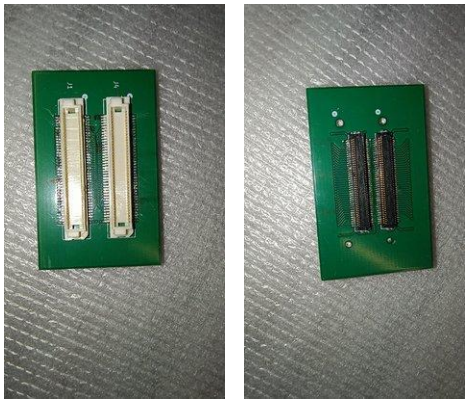
Software

Legacy C++ DAQ code built in a Docker container, so it runs on a modern OS

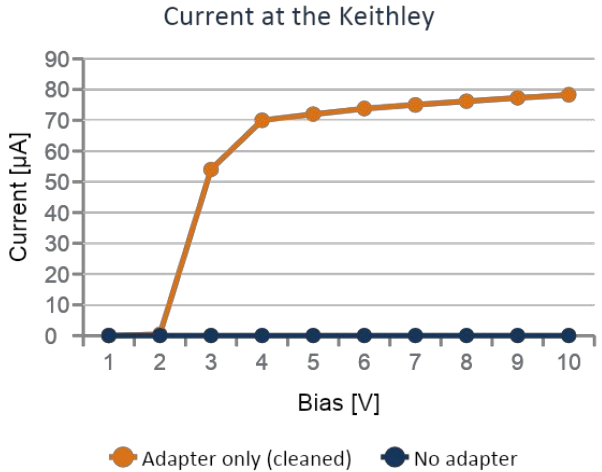
Slow control works: DACs set on all 8 chips, AVDD = 3.3 V, temperature sensors read out

Adapter: unexpected leakage current

Stage 2 · SPIROC



Adapter, front / back: old SPIROC footprint → new 128-ch array connector

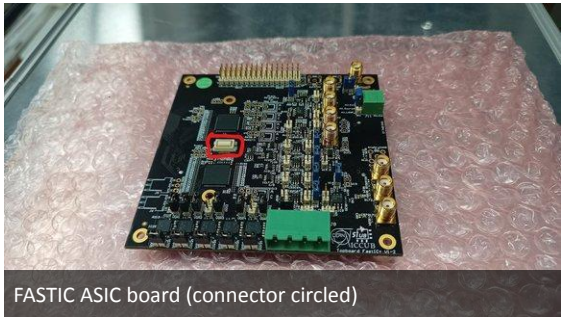


Leakage follows the adapter: ~75 µA by 4 V; < 0.05 µA without it
Not the SiPM array: same curve with the array disconnected
Not dirt: isopropanol + ultrasonic cleaning changed nothing
Shape not conclusive yet: Keithley compliance was 100 µA, so the flat part above ~4 V is limited by the supply

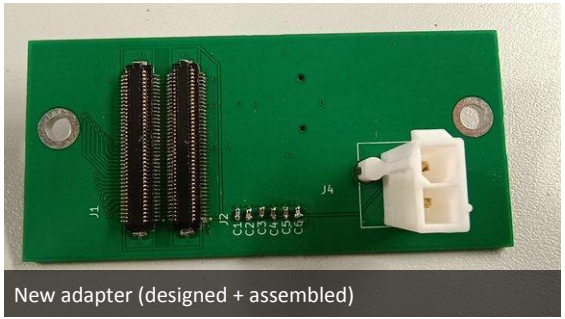
Cause: pin mismatch between the adapter and the SPIROC card connector. Next: corrected adapter, then repeat the IV scan before biasing the array.

Status: nothing damaged (< 1 mW), bias kept ≤ 12 V, array not yet biased on SPIROC. The rest of the chain is verified.

Stage 3: FastIC readout


FASTIC ASIC board (connector circled)

Readout / FPGA board (MAX10)


New adapter (designed + assembled)

Why FastIC if we have SPIROC?

- SPIROC is old and has not been manufactured for a long time
- Components are obsolete and hence not replaceable
- Only a few working setups are left
- Very old software makes operation messy
- FastIC: a modern SiPM front-end ASIC that is still supported

Status

✓ Software and hardware integration tested

✓ Adapter designed and assembled

… **Next: tests with the EPFL detector**

Summary and outlook

Stage 1 · Oscilloscope

DONE

Light-tight test stand with light pulser; single-p.e. resolution, G ≈ 2.8 ×10^6 at 56 V

Stage 2 · SPIROC

IN PROGRESS

Legacy DAQ running in Docker; adapter leakage being debugged

Stage 3 · FastIC

HARDWARE READY

Integration tested, adapter assembled; detector tests next

Outlook

- Fix the SPIROC adapter mapping and repeat the reference measurement with SPIROC
- FastIC measurements with the EPFL detector
- Compare readouts quantitatively: gain, noise, p.e. resolution; bias scans
- Obtained results will be further used in developing the test stand

Thank you!

Questions and discussion are welcome

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