CWRF'2012
Brookhaven, 8-11 May 2012

Development at the ESRF of advanced solid state amplifiers for accelerators

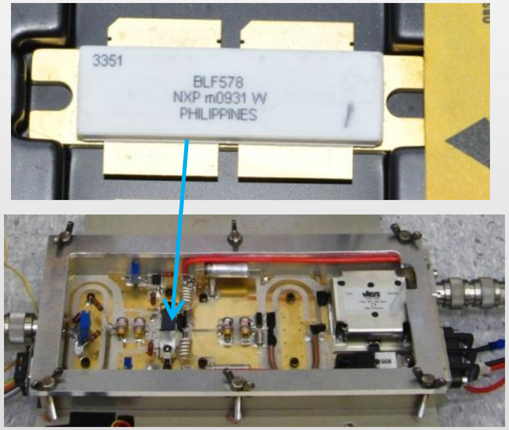
Michel Langlois & Jörn Jacob
ESRF

** This work, carried out within the framework of the CRISP project, has received research funding from the EU Seventh Framework Programme, FP7.*

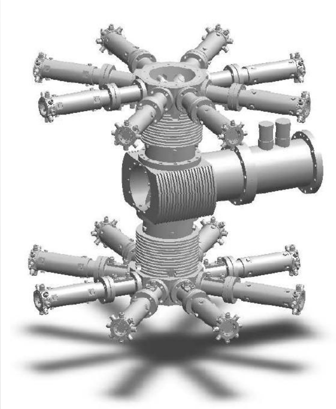
Existing 150 kW RF SSA at 352.2 MHz

- Initially developed by SOLEIL
- Transfer of technology to ELTA / AREVA

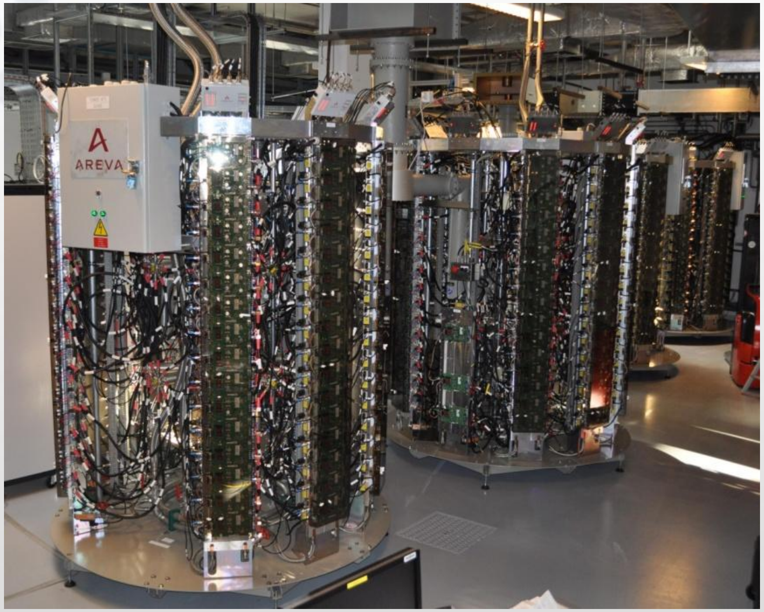
Pair of push-pull transistors



x 128



x 2



650 W RF module

- 6th generation LDMOSFET (BLF 578 / NXP), V_{ds} = 50 V
- Efficiency: 68 to 70 %

75 kW Coaxial combiner tree

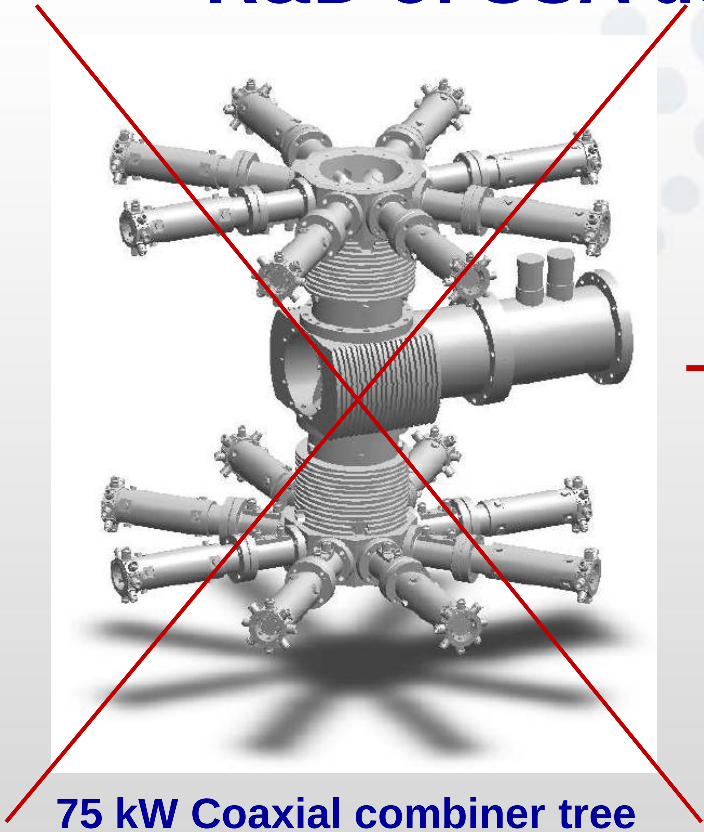
with λ/4 transformers

150 kW - 352.2 MHz Solid State Amplifiers for the ESRF booster

Efficiency: > 55 % at nominal power

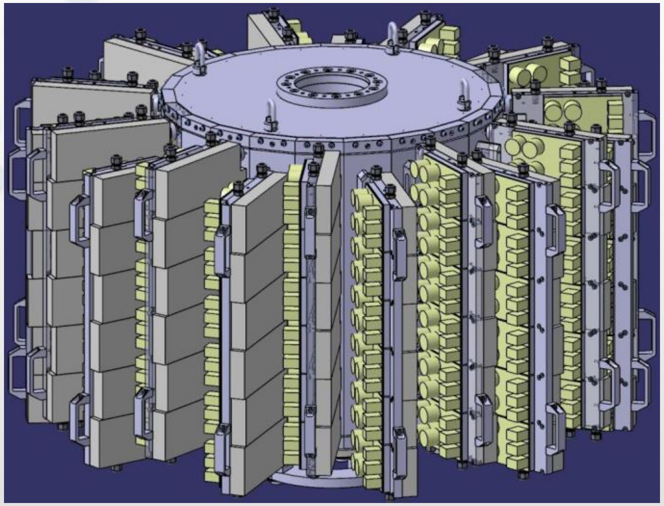
- 1st batch of 4 x 150 kW SSAs from ELTA in operation on ESRF booster since March 2012
- 2nd batch of 3 x 150 kW SSAs in fabrication, will power 3 new cavities on ESRF storage ring

R&D of SSA using Cavity Combiners



75 kW Coaxial combiner tree

with $\lambda/4$ transformers

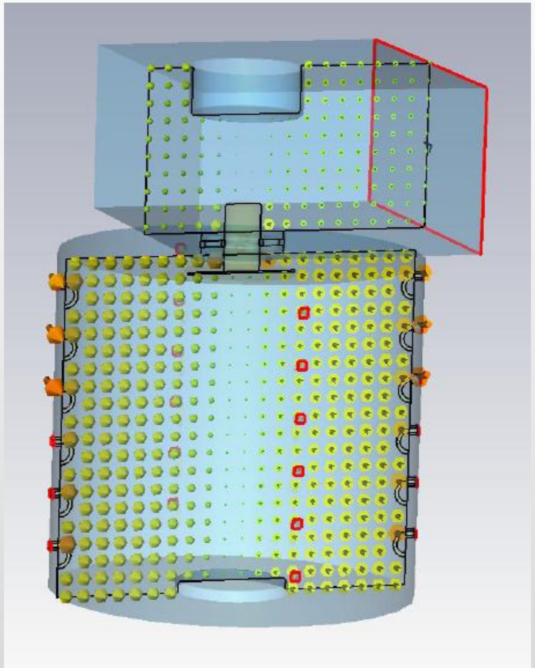


75 … 100 kW Cavity Combiner

Work package WP7 of EU/FP7/ ESFRI/CRISP:

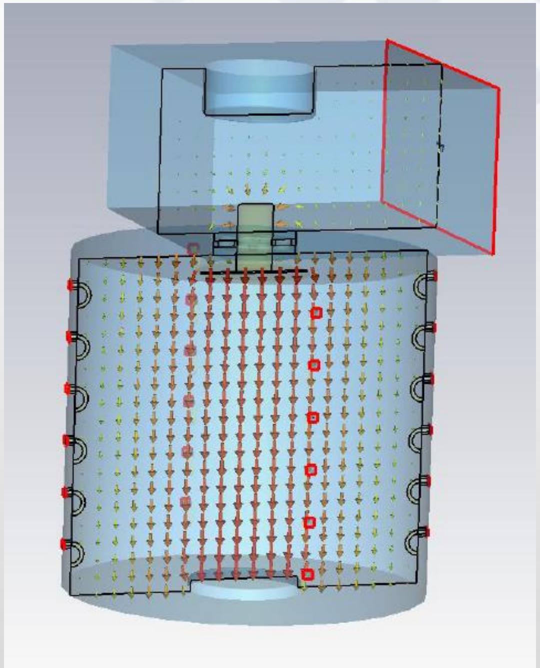
- Development of SSAs using cavity combiners
- Feasibility studies for project partners:
  - CERN/SLHC *[Eric Montesinos]*
  - ESS *[Rebecca Seviour]*
  - GSI/FAIR *[Wolfgang Vinzenz]*

Cavity Combiners: principle



H field

Homogenous magnetic coupling of all **input loops**



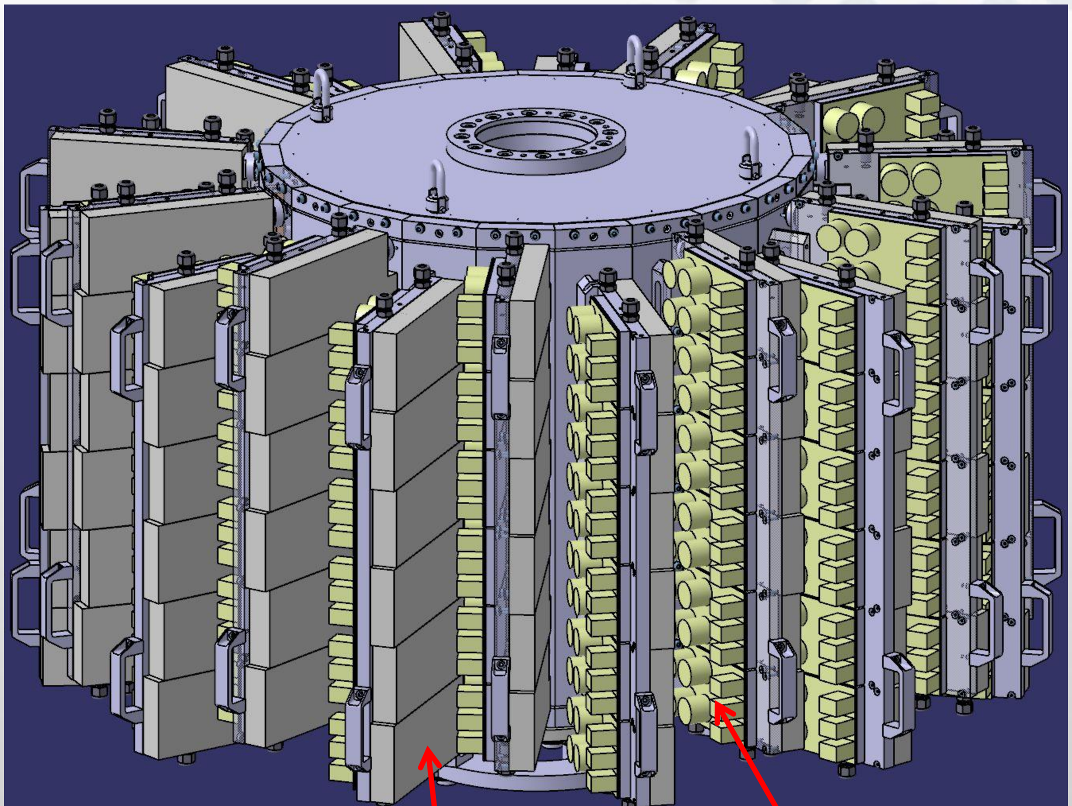
E field

Strong capacitive coupling to **the output waveguide**

Strongly loaded E_{010} resonance

- Modest field strength
- Cavity at atmospheric pressure
- 1 dB - Bandwidth ≈ 500 kHz

SSA using Cavity Combiner: design



RF module

AC/DC converter

For ESRF application:

- **6** rows x **22** Columns x **600 … 800 W** per transistor module

  $\Rightarrow$ 75 … 100 kW

- More compact than coaxial combiners

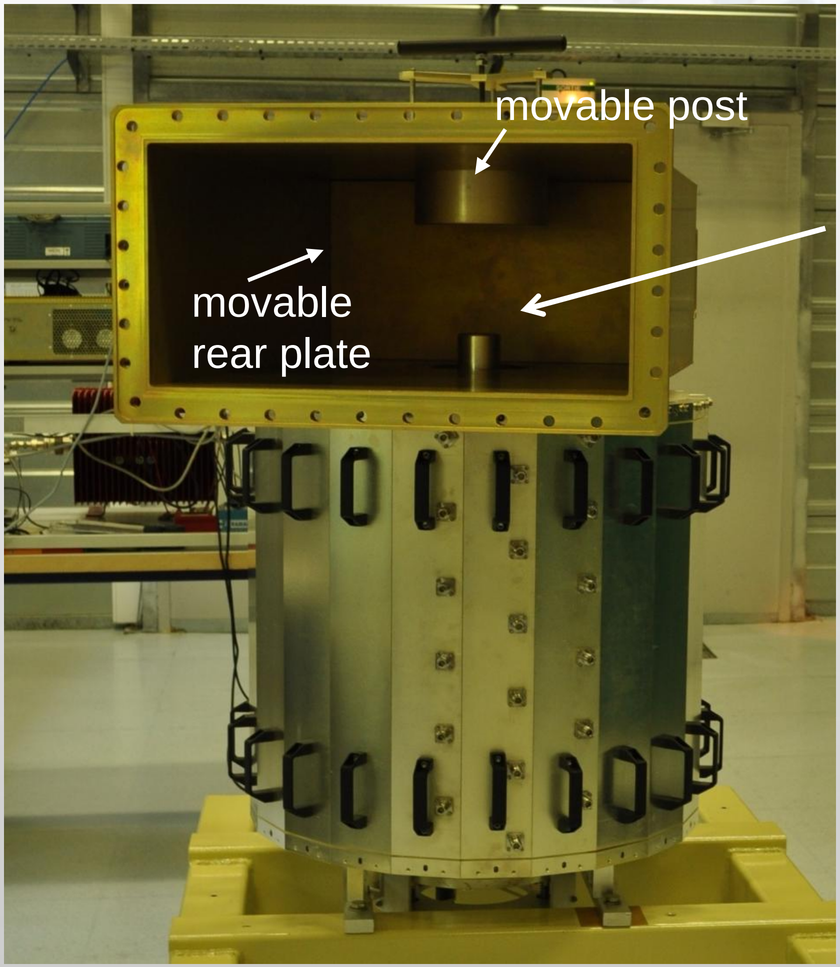
  $\beta_{waveguide} \approx n_{module} \times \beta_{module} >> 1$

- Easy to tune if n_{module} is varied
- Substantial reduction of losses $\Rightarrow$ higher η

[M. Langlois, F. Villar, ESRF]

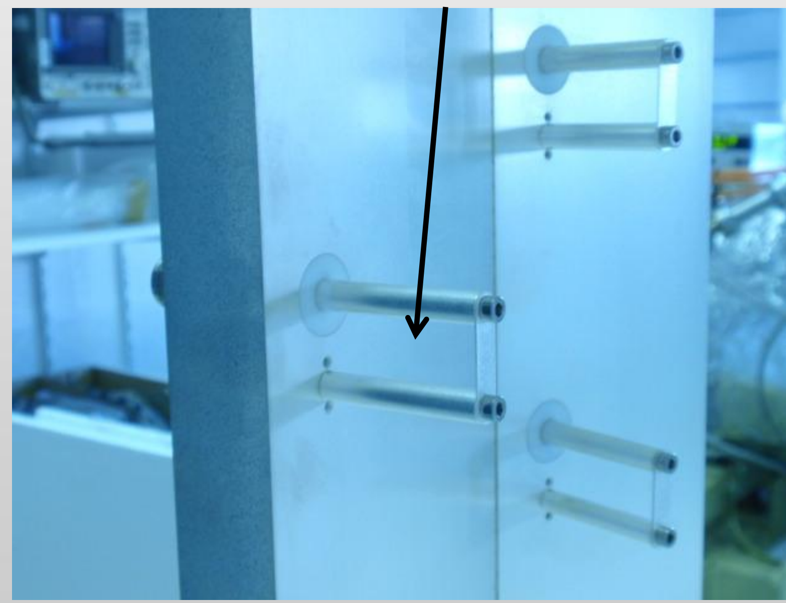
Cavity Combiner: the 10 kW prototype

The full size model has been built in the RF lab. The waveguide output has been integrated. Only 3 active columns are implemented.

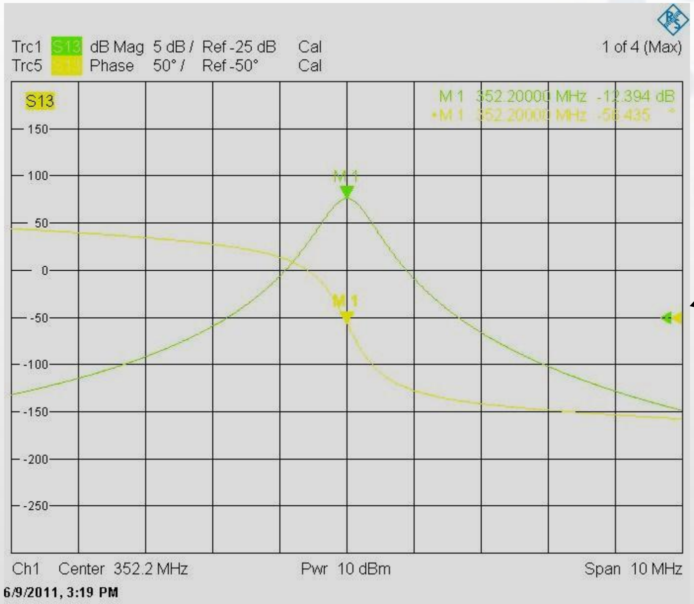


Output coupling

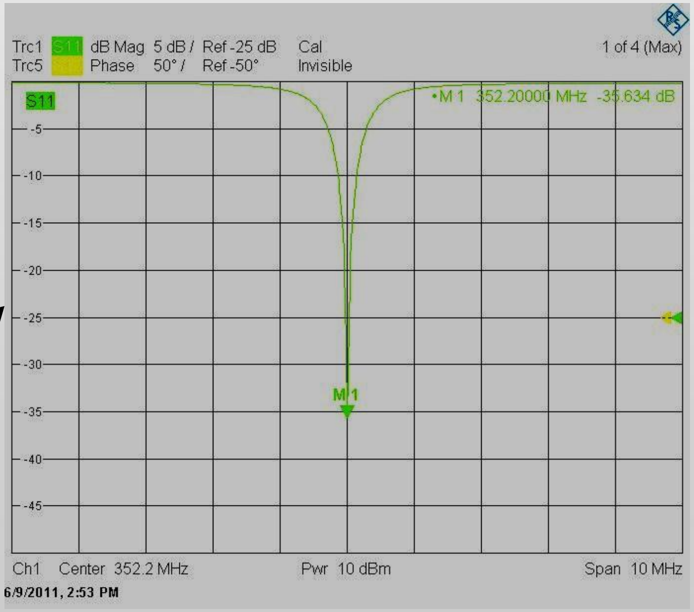
Input coupling



Cavity Combiner: low level results



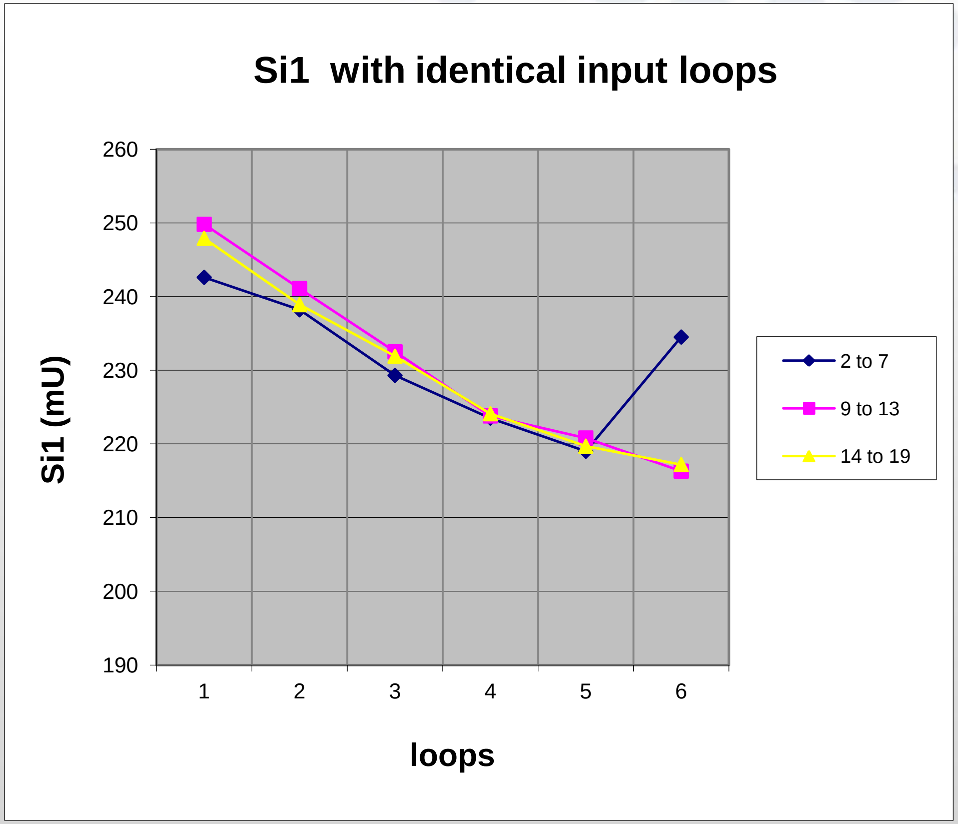
S31 plot measured with a NWA
Port 1 = waveguide output port



S11 plot measured with a NWA:

☞ The output can be matched with 7 to 18 inputs without changing the loop size (by means of movable short and post).

Cavity Combiner: issues



S1i:

i: Input loop number i

1: Output waveguide port

- The behaviour with power has not yet been tested.
- There is a small systematic dependency of Si1 on the i loop position:
  $\Rightarrow$ the loop size must slightly vary with position.

RF module development for Cavity Combiner

Targets

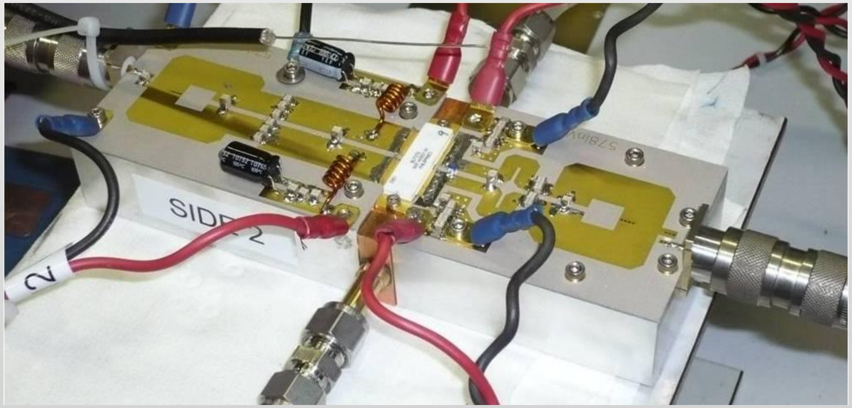
- Frequency: 352.2 MHz
- Power: 800 W cw at -1dB compression
- Cost effective
- Protected against V.S.W.R
- Bandwidth: 2MHz at 0.2 dB
- Drain efficiency: 70% at full power
- Low quiescent current

Avoidance of components needing manual intervention

- No variable capacitors
- Suspended planar baluns
- No trimmer except for gate bias
- No chokes

Transistor choice: LDMOS 50V

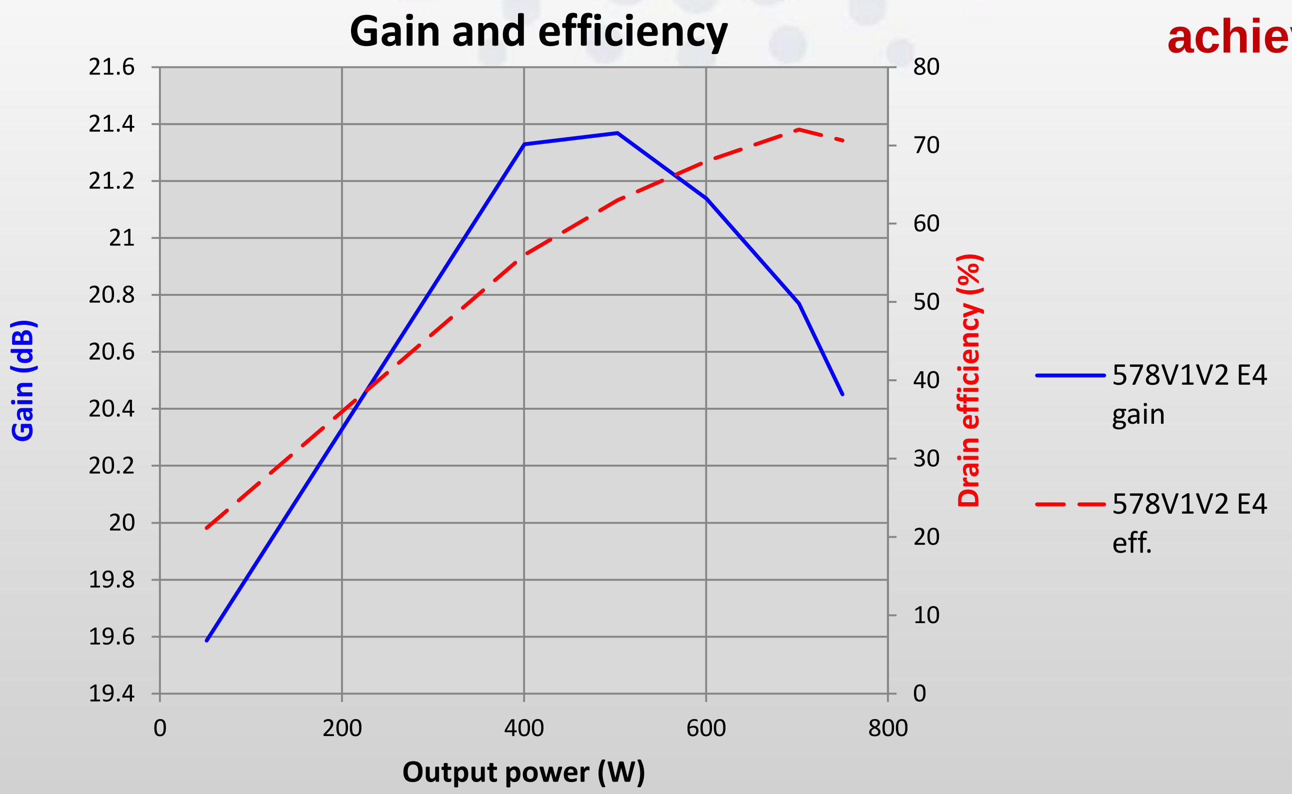
- NXP BLF578
- FREESCALE MRF6VP41KH
- Ruggedized version of the formers



Prototype RF module with planar balun transformer (still hand made chokes)

[M. Langlois, ESRF]

RF module development: results

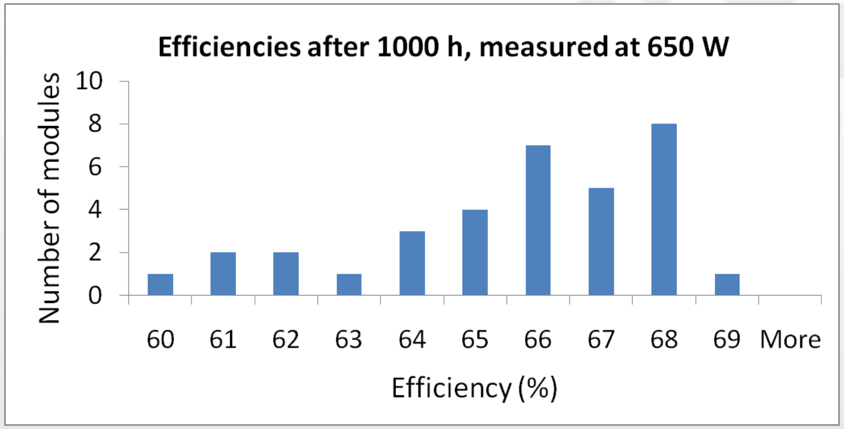


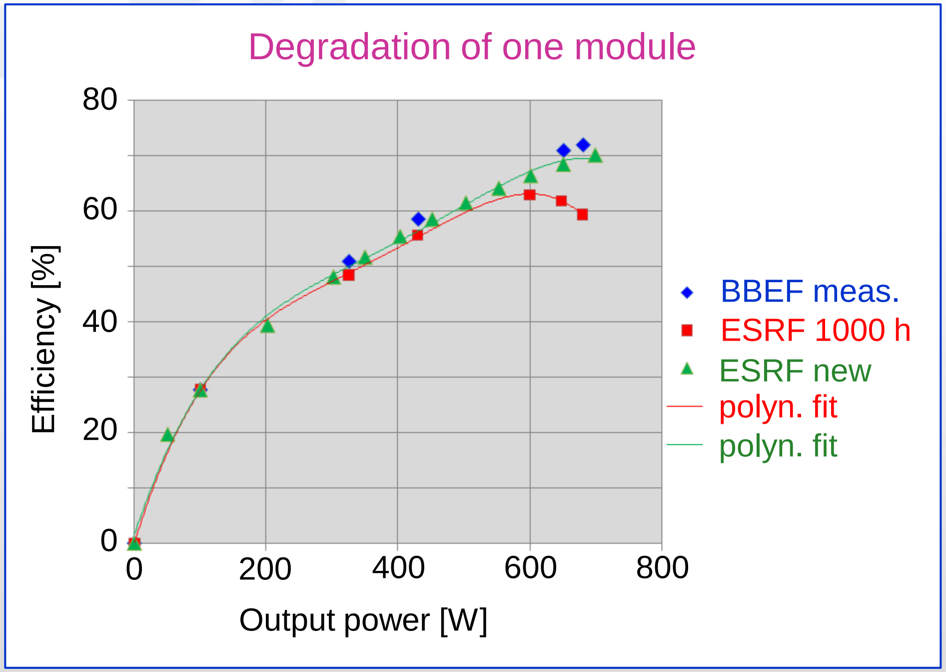
750 W achieved !

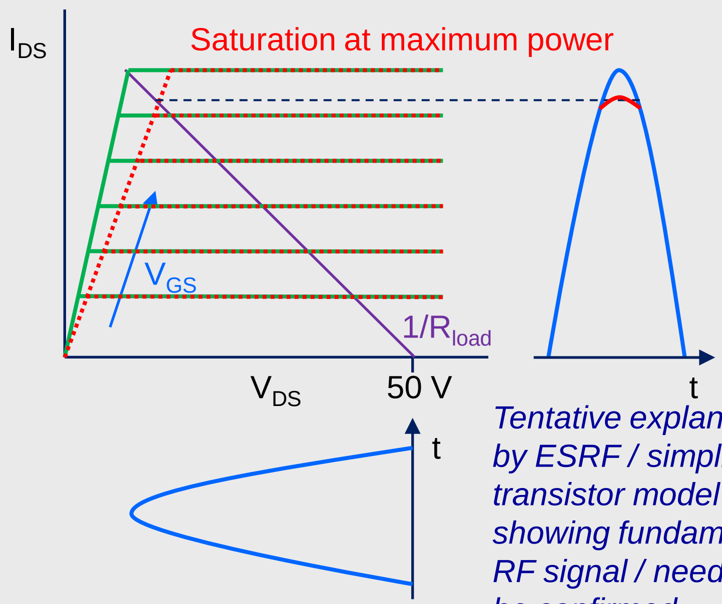
RF module development: issues

- The results shown were obtained with the NXP transistor. It has to be repeated with the FREESCALE MOSFET.
- The power limitation comes from the transistor ESD protection diode, which conducts as soon as the input power reaches 6.4 W. This was seen on 2 transistors.
- The reproducibility needs to be checked.
- The circuit still has drain chokes. Other implementations are under study.
- The electrolytic capacitors used for drain and gate bias cannot be easily picked and placed.
- The output balun and the output matching capacitor are hot. Long runs have to be performed to make sure these temperatures are acceptable.

Efficiency degradation / 1st ELTA tower [see JM Mercier's talk]





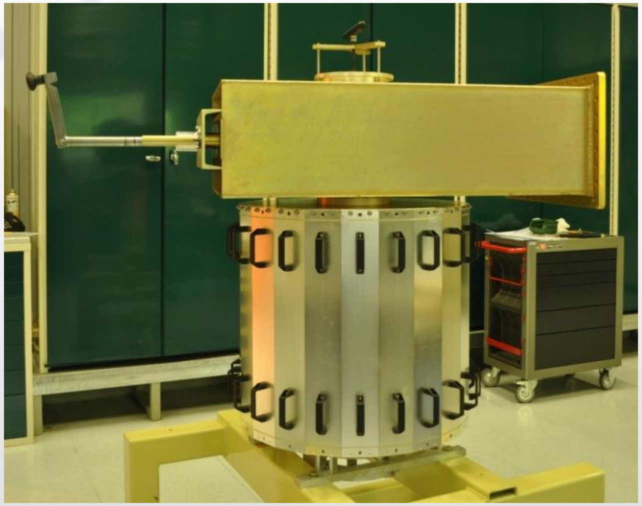


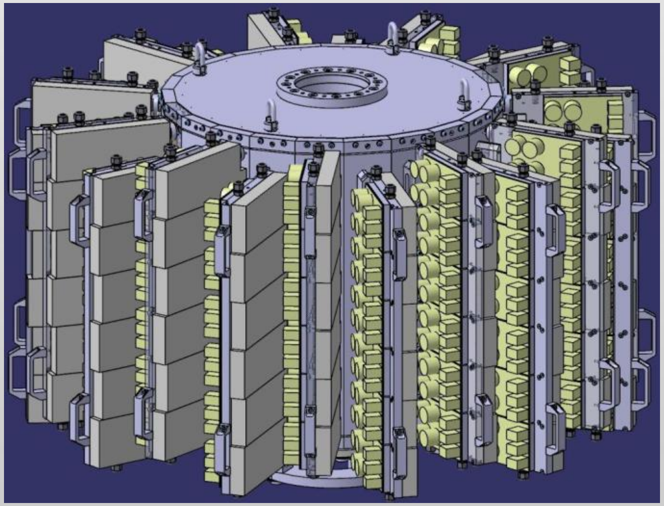
Tentative explanation by ESRF / simplified transistor model showing fundamental RF signal / needs to be confirmed

- ✓ NXP: checked transistors are still in spec
- ✓ ESRF experiment: Partial cure by UV radiation ☞ indicates electron trapping in crystal defects of LDMOSFET channel, but not only explanation
- ✓ ELTA & NXP are investigating this phenomenon
- ✓ Only little degradation on SSA efficiency, since nominal module power around 610 W, i.e. at the limit of the observed effect

Next steps in the ESRF R&D

- Finalize the RF module
- Fabricate a series of 18 units to equip 3 combiner wings
- Assemble and power test the 10 kW prototype cavity combiner
- Build and power test a 75 … 100 kW cavity combiner with 132 RF modules
- In parallel: carry out feasibility studies for applications at the partner labs of the European CRISP project





Tentative SSA specifications / CRISP partners

Lab	Project	Frequency	Pulsed or cw?	Average power	Peak power	Num-ber	Alternative to transistors
CERN	LIU-SPS	200 MHz	both cw and 10 µs - 5 s / 43 kHz-0.1 Hz	75 kW	150 kW	x 32	Tetrodes, Diacrodes (under CFT)
CERN	Linac 4	352 MHz	2 ms / 50 Hz	1300 kW 2800 kW		x 13 x 6	Klystrons
CERN	LHC	400 MHz	both cw and 45 µs / 11 kHz	350 kW	350 kW	x 16	Klystrons
CERN	SPL	704 MHz	2 ms / 50 Hz		600 kW 1100 kW	x 62 x 184	Klystrons, IOTs
CERN	SPS upgrade	800 MHz	Both cw and 10 µs - 5 s / 43 kHz-0.1 Hz	350 kW	350 kW	x 2	Klystrons, IOTs
GSI	FAIR	108.4 MHz	cw and 1 - 4 ms/ 1- 50 Hz	2.5, 10 , 50 kW/unit	2.5, 10 , 50 kW	x 2...4	Tetrodes
GSI	FAIR	216 MHz					
ESRF	ESRFUP	352.2 MHz	cw and pulsed 50 ms / 10 Hz	150 kW	150 kW	x 22	Klystrons

Mismatch of unpowered modules: over-load of individual circulator loads

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ \dots \\ b_N \\ b_{N+1} \end{bmatrix} = \begin{bmatrix} (1-N)/N & 1/N & 1/N & \dots & 1/N & 1/\sqrt{N} \\ 1/N & (1-N)/N & 1/N & \dots & 1/N & 1/\sqrt{N} \\ 1/N & 1/N & (1-N)/N & \dots & 1/N & 1/\sqrt{N} \\ \dots & \dots & \dots & \dots & \dots & \dots \\ 1/N & 1/N & 1/N & \dots & (1-N)/N & 1/\sqrt{N} \\ 1/\sqrt{N} & 1/\sqrt{N} & 1/\sqrt{N} & \dots & 1/\sqrt{N} & 0 \end{bmatrix} \times \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ \dots \\ a_N \\ a_{N+1} \end{bmatrix}$$

input arms: $a_1 \dots a_N$, $b_1 \dots b_N$,
output arm: a_{N+1}, b_{N+1}

Simplified S-matrix of an ideal " x N" combiner

- *λ/4 coaxial combiner: some phase factors and different S_{ij}, $i \neq j \in [1 \dots N]$*
- *however, similar conclusions as sketched here below*

Example 1: x8 combiner,
$|a_i|^2$ = 650 W, no losses
☞ Example 2: x132 combiner

Input arms: strongly mismatched but,

$$\forall i, j \leq N, a_i = a_j \quad \Rightarrow \quad b_i = b_j = 0 \text{ and } b_{N+1} = \sqrt{N} \times a_i$$

b_i = 0: difference of large numbers
$|b_{N+1}|^2$ = 8 x 650 W = 5.2 kW
☞ 85.8 kW for x 132 combiner

If any input arm i is unpowered:

$$a_i = 0 \quad \Rightarrow \quad b_i = \frac{N-1}{N} \times a_j \quad , \quad j \neq i$$

$|b_i|^2 = (7/8)^2$ x 650 W = 498 W
☞ 640 W for x132 combiner

Under worst phase conditions, for any output reflection of, say, 1/3 in power, the unpowered input arm i will receive

$$|b_i| = \left\{ \frac{N-1}{N} + \frac{1}{\sqrt{3}} \right\} |a_i|$$

$|b_i|^2 = (1.45)^2$ x 650 W = 1371 W
☞ 1602 W for x132 combiner

What can be done?

This problem can be solved partially or fully in different ways:

- Over-dimensioning of the circulators and loads on the individual RF modules
- Addition of a high power circulator and load at the SSA output
- Optimization of phases

Consequences for the SSAs delivered by ELTA [see also JM Mercier's presentation]:

- For batch 1 installed on the ESRF booster, thanks to the pulsed operation and a peak factor above 3, it was checked that there is no over-load situation
- A solution is being worked out by ELTA for batch 2, which will operate in CW on strongly beam loaded RF cavities of the ESRF storage ring, with possible mismatch at high power

THANK YOU !