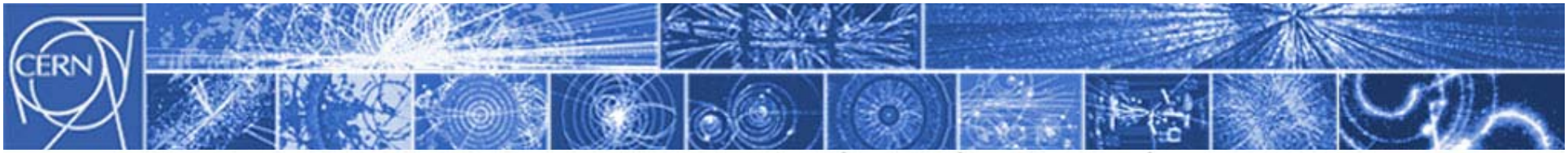

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Fast and low noise active feedback preamplifier with the stabilization of the DC potential at the output

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31 May 2007

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Background of the presented front end developments

Primary applications:

Front End amplifiers for readout of silicon strip detectors (SSD) at LHC experiments

Architecture determined by optimization of noise and power consumption for given detector capacitance and timing parameters.

- Single ended stage for preamplifiers and shapers
- Differential discriminator stages AC coupled to shapers in order to improve PSRR at low frequencies

Background of the presented front end developments

Example of key specifications for FE amplifier for SSD :

Input signal (Minimum Ionizing Particle) in the order of 3.5fC, dynamic range up to 12fC (300µm thick detector)

Peaking time 20 to 25ns

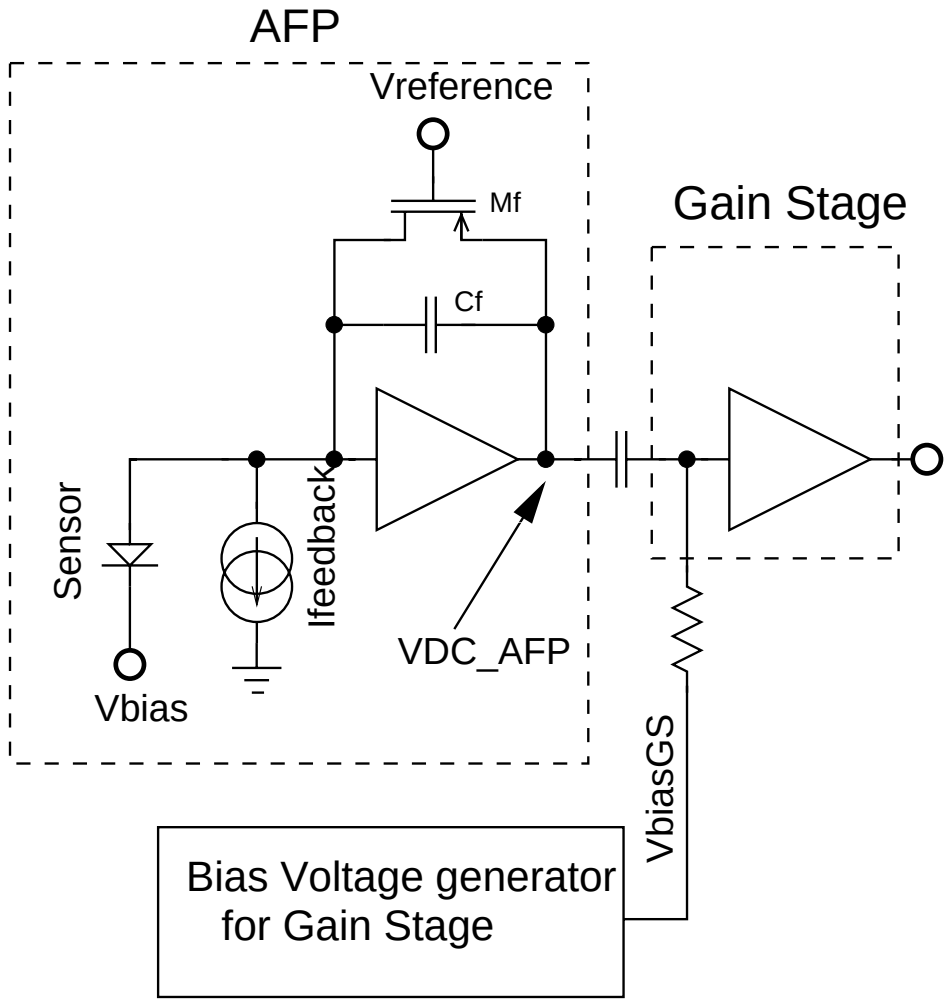
Double pulse resolution 50 – 100ns

Noise; ENC ≤ 0.25fC noise for nominal detector capacitances

Detector capacitances; 5 to 30pF

Timing parameters compatible with the timing requirements for high rate counting applications (imaging).

Architecture of the active feedback preamplifier



Principles of AFP:

- ***Charge sensitive preamplifier - integration of the collected charge signals from the detector on the feedback capacitance Cf***
- ***Discharge of the Cf by the feedback transistor Mf biased in the saturation by the current source***
- ***Value of the feedback current (gm) depends on the given application (charge vs. transimpedance mode of the preamp, FE speed, acceptable level of parallel noise, value of Cf which is correlated with Cinput)***

Motivation for DC coupling between signal processing stages

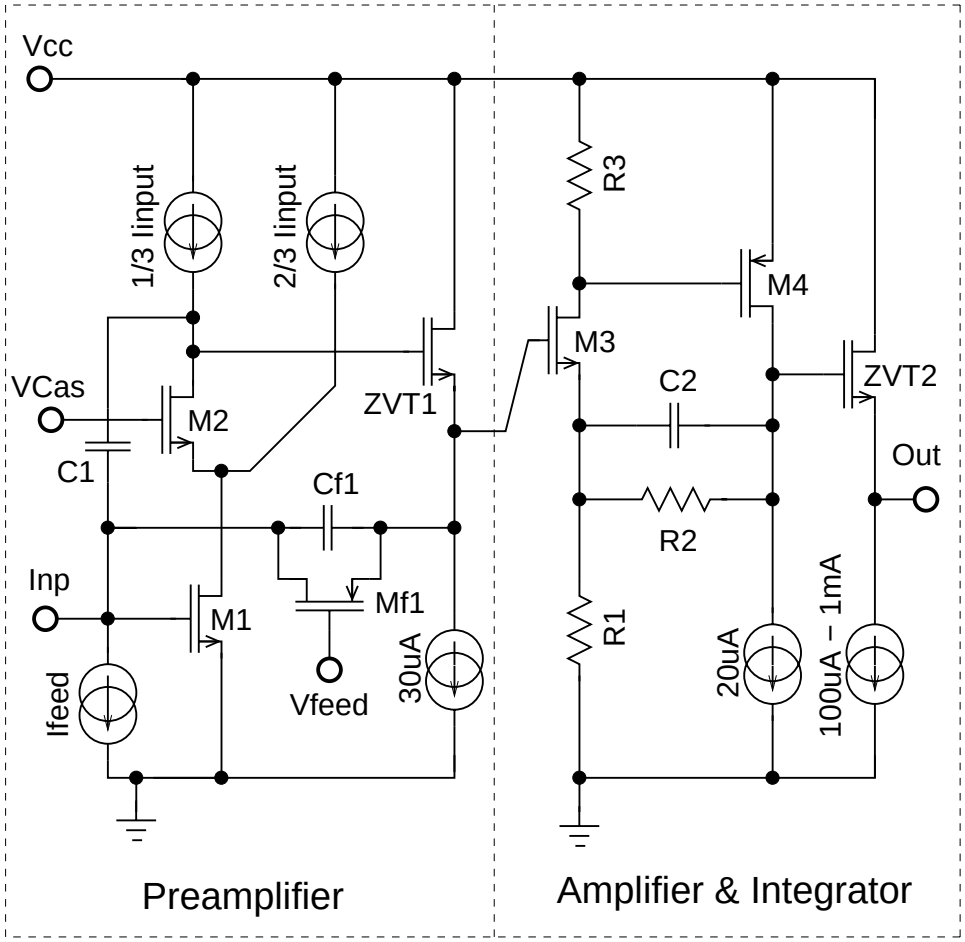
Variation of DC potential at preamplifier output due to the variation of feedback current and technological parameters

The standard solution avoiding the propagation of the DC variation from AFP output to the next stages is the AC coupling between the AFP and the gain stage

Disadvantage: undershoot on the signal response (differentiation of the signal)

- Limitation in double pulse resolution and counting rate
- Degradation of noise filtering efficiency

Architecture of the FEDC1 amplifier

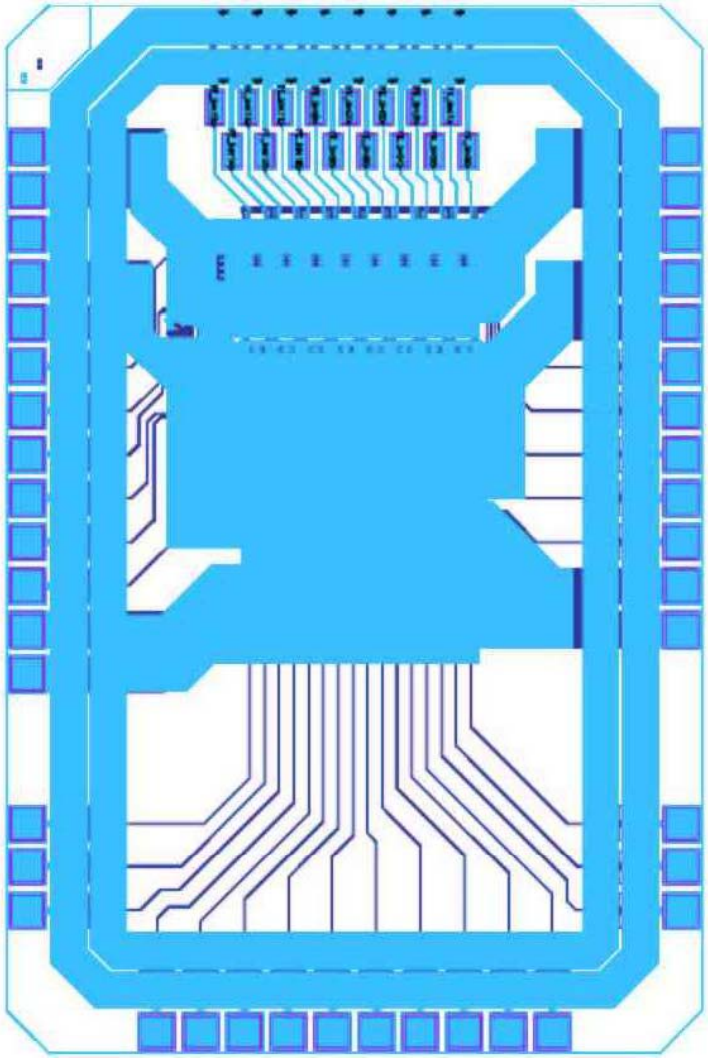


Cascode preamplifier working in transimpedance configuration with PMOS feedback transistor biased in saturation (AFP configuration).

Preamplifier stage DC coupled to amplifier/shaper stage.

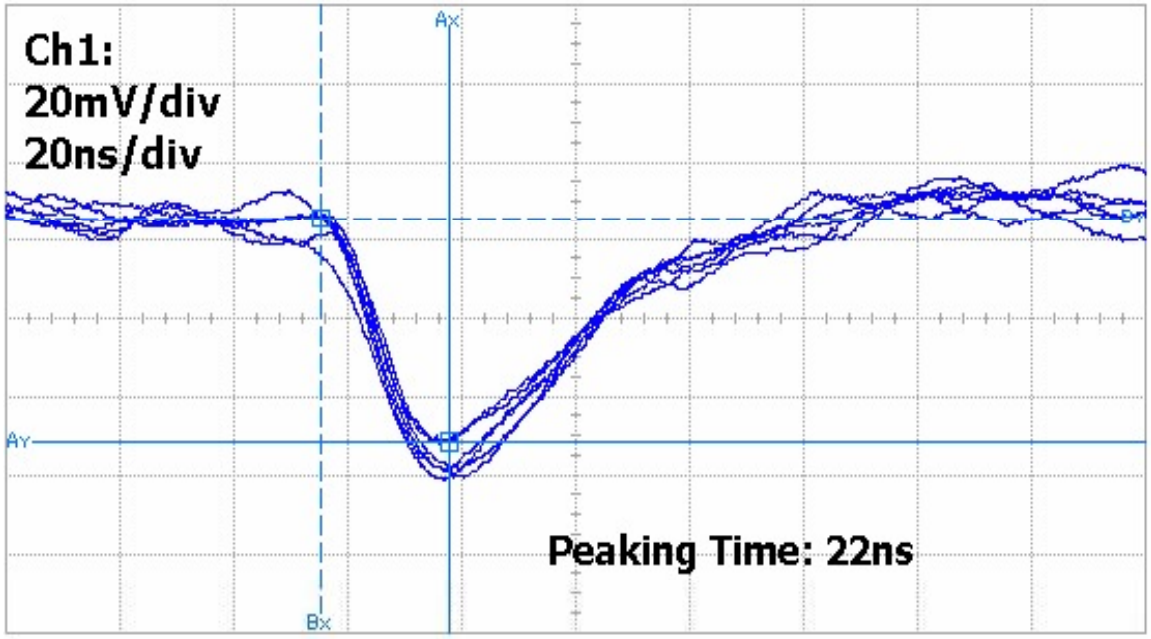
DC potential at the output of the preamplifier stage and overall operating point of second stage controlled by voltage at the gate of the feedback transistor (PCT/EP/2005/004986)

FEDC1 layout



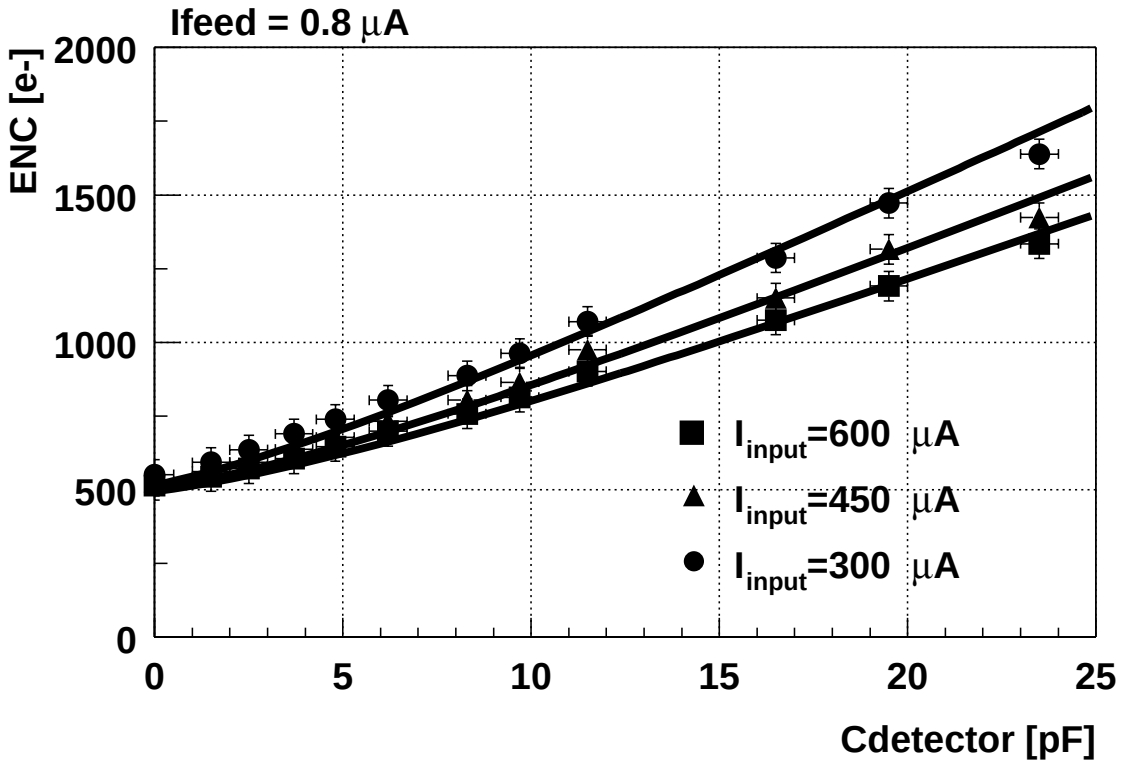
- *Technology: CMOS IBM 0.25um*
- *Chip physical dimensions: 2x3mm*
- *16 preamplifier/shaper channels with parallel outputs (buffers can drive up to 20pF load capacitance)*
- *External biases*
- *Calibration inputs (on-chip calibration capacitors)*

Performance of the FEDC1 amplifier



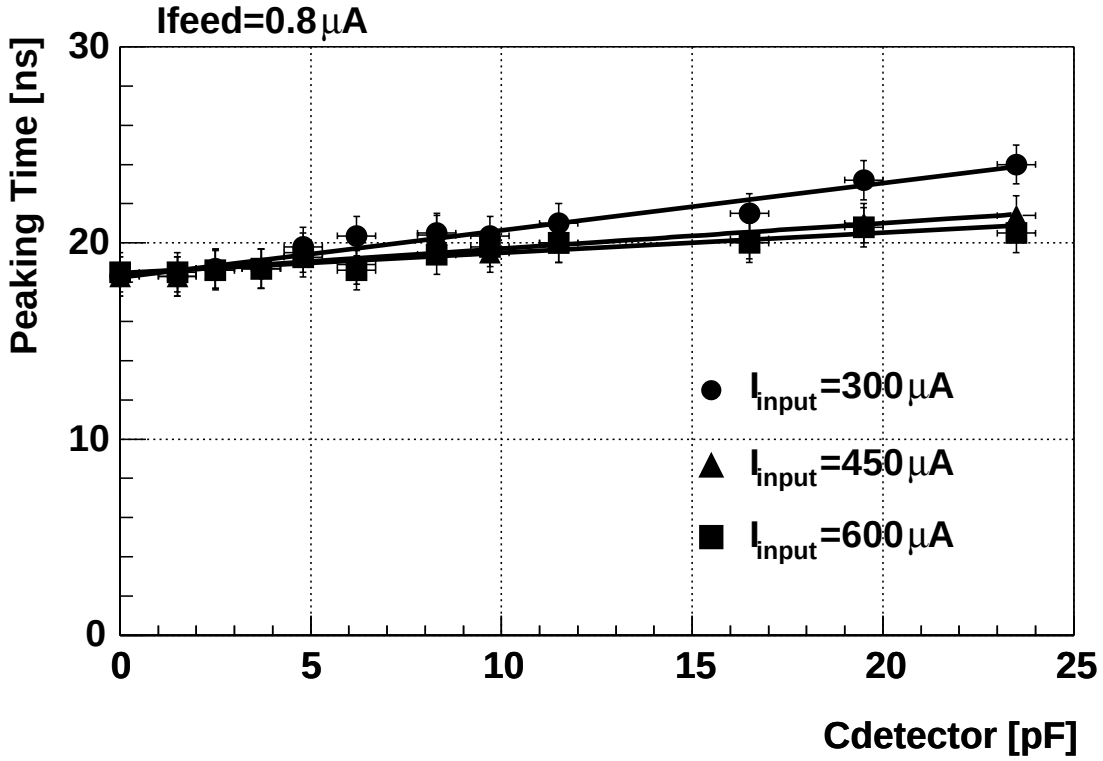
Response of the preamplifier/shaper loaded with 20pF input capacitance to 3.5fC input signal

Noise performance of the FEDC1 amplifier



Equivalent Noise Charge as a function of detector capacitance for nominal feedback transconductance and various input transistor bias. (1fC charge equivalent to 6250e-)

Timing performance of the FEDC1 amplifier



Peaking time as a function of detector capacitance for nominal feedback transconductance and various input transistor bias. Input impedance of the amplifier in the range of 120 to 160Ω.

Applications

FEDC1 type Front End presently used in:

- VFAT chip (readout chip for silicon detectors in TOTEM experiment)
- Readout chip for diamond detectors for beam monitoring in CMS experiment
- Front End in ABCN chip (readout of SSD for ATLAS SCT upgrade)
- BioCare PET-CT readout module (FEDC1 + NINO)

FEDC1 design is a good candidate for the new versions of front end for counting mode chips for CT applications (see talk by Danielle Moraes)