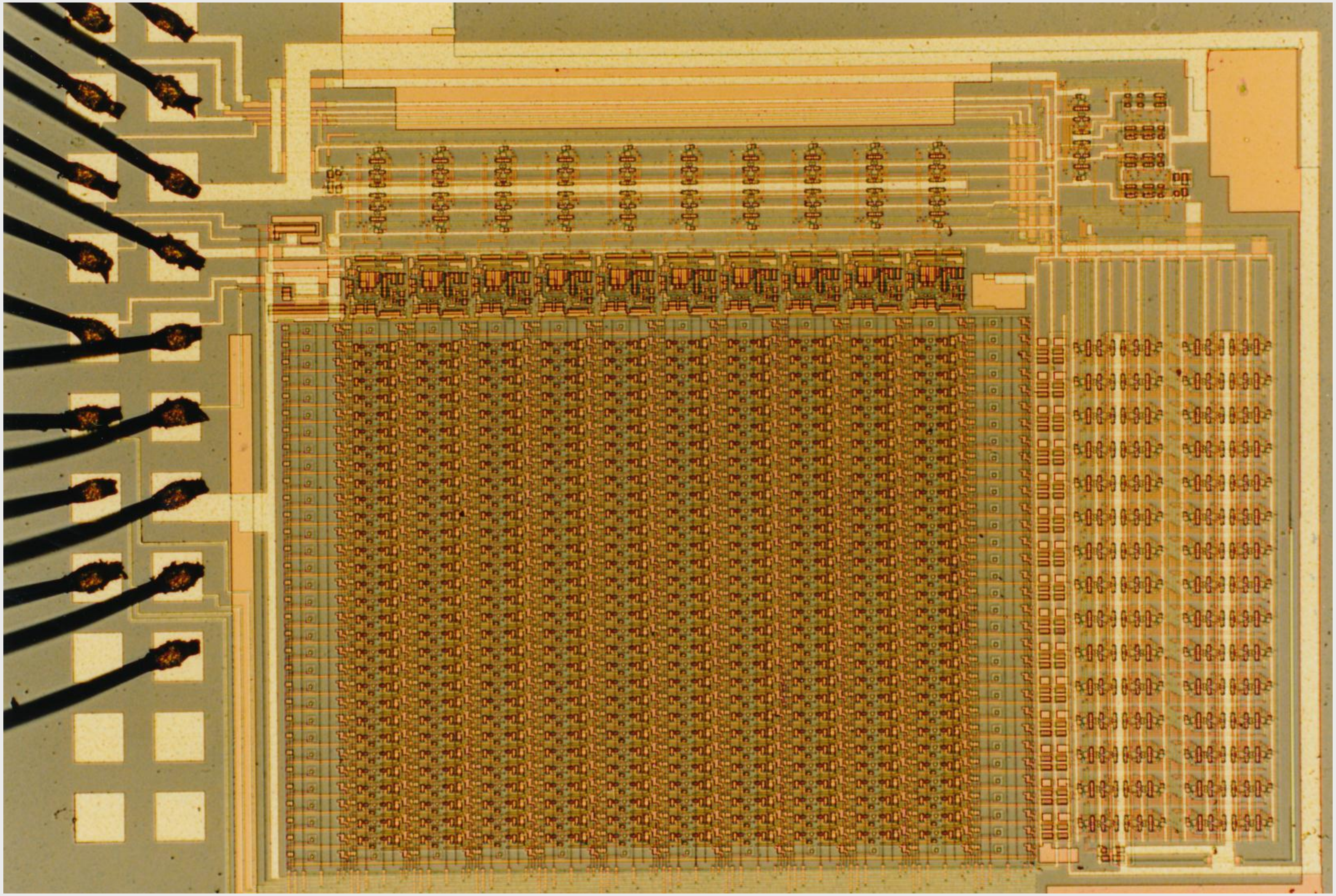
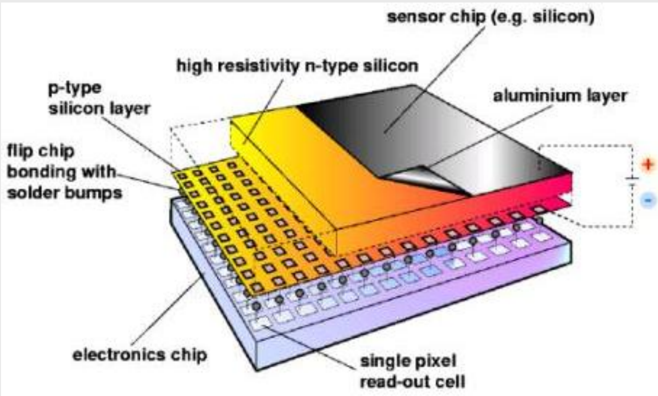
MONOLITHIC DETECTORS 1987-1992

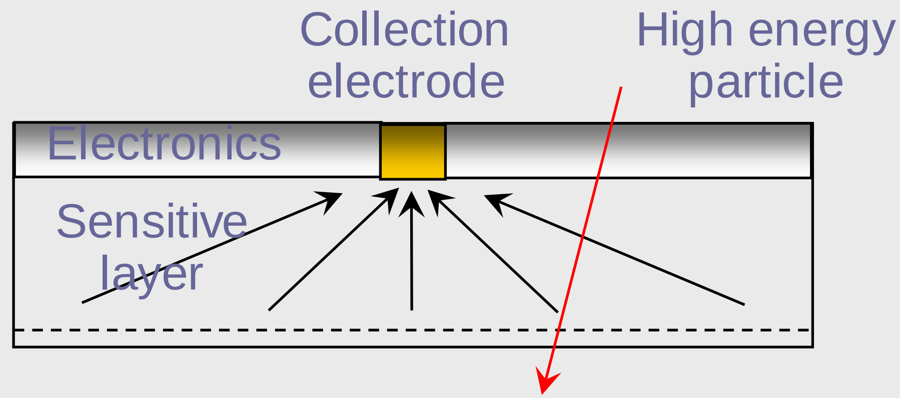


MONOLITHIC DETECTORS 1987-1992

- Graduate student with Prof. Plummer
- Sherwood Parker – U of Hawaii worked with Stanford and just had a new proposal for the development of a monolithic detector
- Started working with Sherwood and Jim on monolithic detector project early 1988

MONOLITHIC DETECTORS IN CMOS
Reverse bias for charge collection by drift

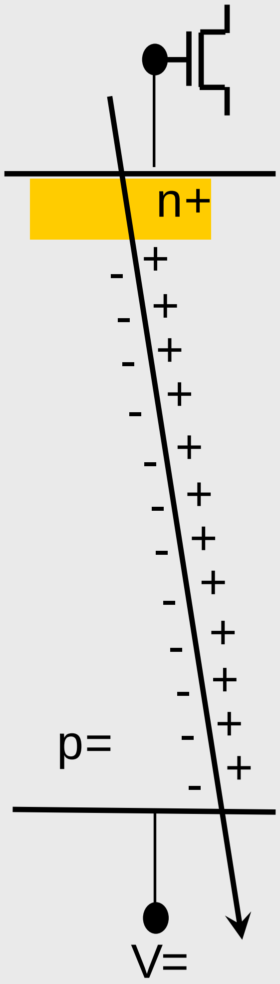




- Develop monolithic pixel detectors integrating readout and detecting elements by porting CMOS to higher resistivity substrates
- Motivation: very interesting for tracker and pixels !
  - Good radiation hardness (charge collection by drift).
  - Monolithic integration
    - Low capacitance for low power consumption = KEY TO LOW MASS

      Easier overall integration
    - Cost

LOW CAPACITANCE FOR LOW POWER
The importance of Q/C



Take transistor noise at 40 MHz BW for 1 uA
(1uA/100x100 um pixel = 10 mW/sq cm)

$$Veq \approx 0.16mV$$

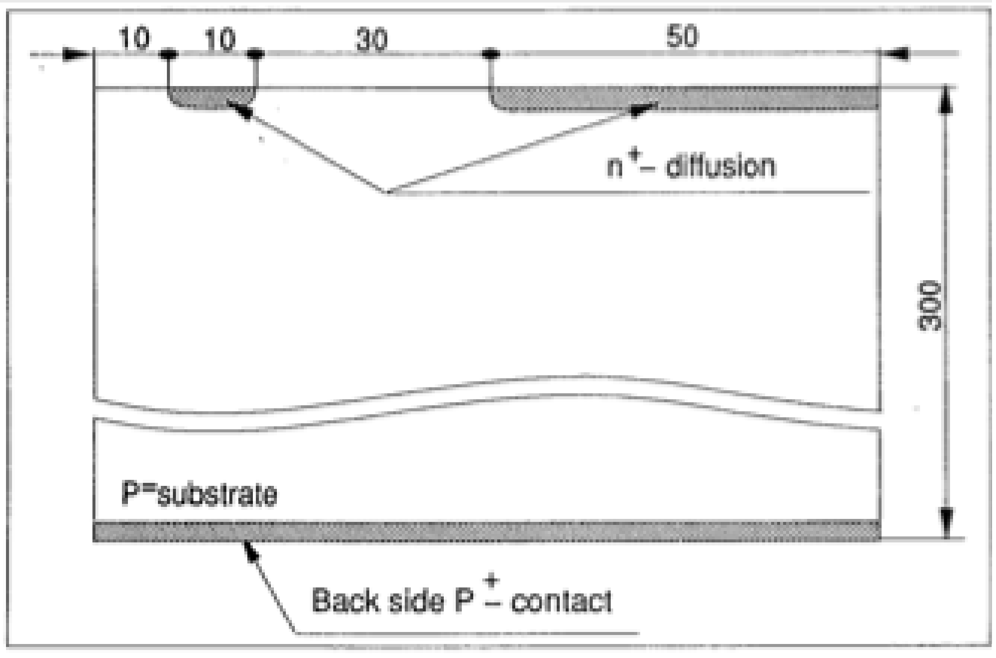
$$\frac{S}{N} = 25 \Rightarrow \frac{Q}{C} = 4mV = \frac{4\,fC}{1pF} = \frac{0.4\,fC}{0.1pF} = \frac{0.04\,fC}{10\,fF}$$

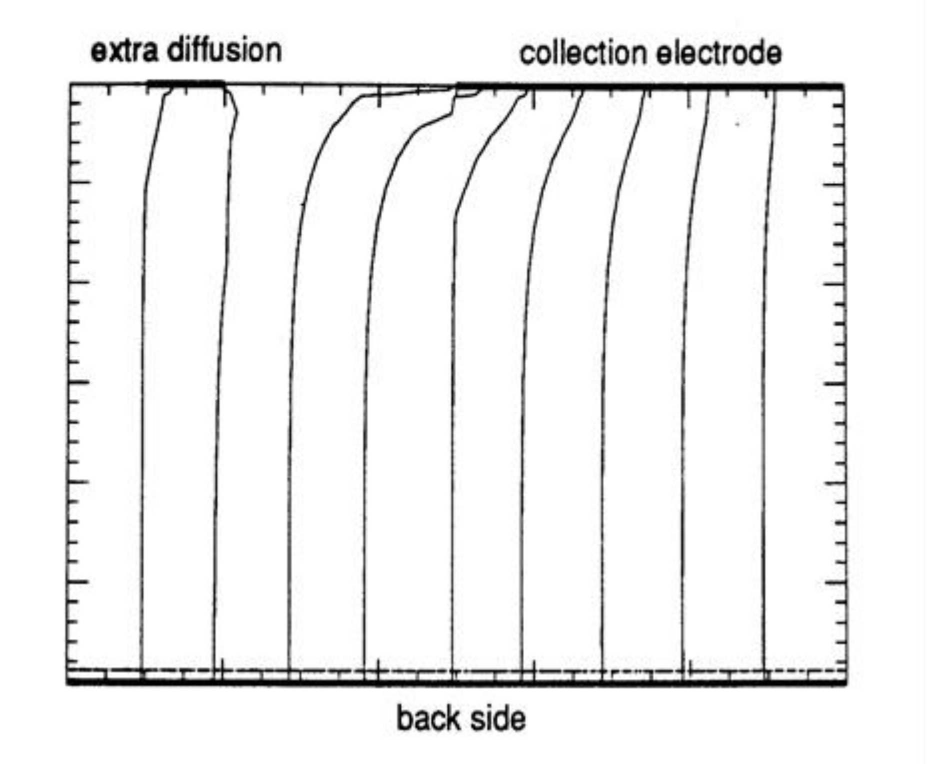
Collection depth 300 μm 30 μm 3 μm

Noise is only very weakly dependent on the current:
(Power~$(Q/C)^{-2..4}$) for same S/N
more Q/C allows very significant power reduction for same S/N (useful eg for smaller pixels)

Monolithic: want SMALL collection electrode for low C

CHARGE COLLECTION ONTO A DESIGNATED COLLECTION ELECTRODE



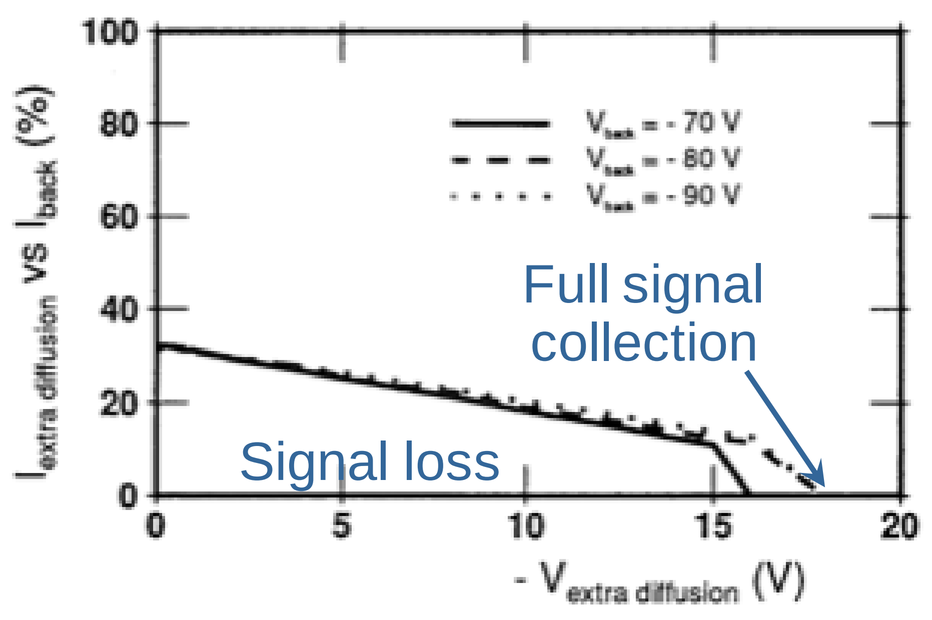


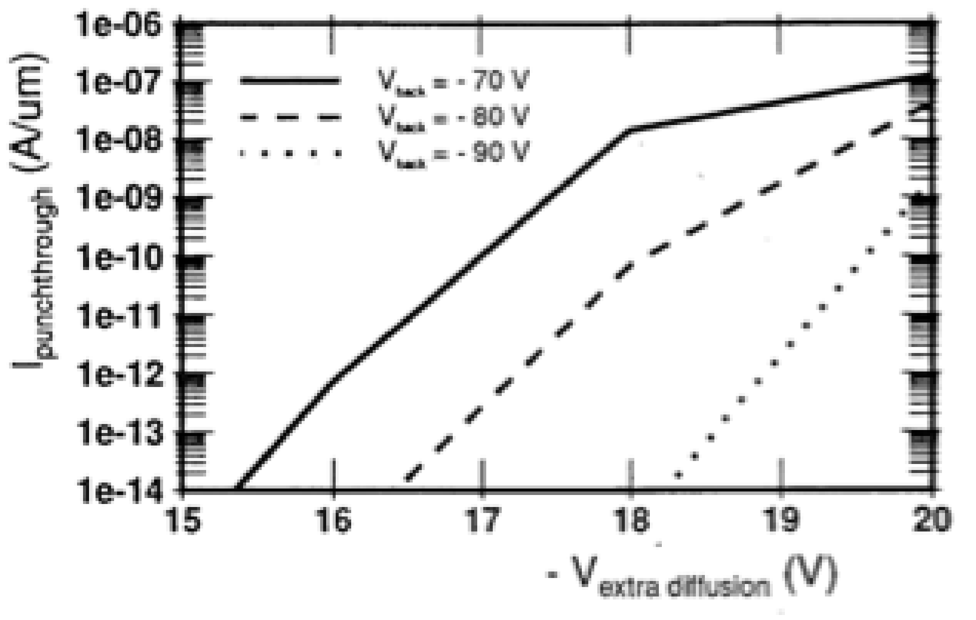
P– substrate N=10^{12} cm^{-3}

Collection electrode at gnd, Vextra diffusion = -5 V, Vback= -80V

Extra diffusion collects charge from a significant fraction of the depleted volume !!

CHARGE COLLECTION ONTO A DESIGNATED COLLECTION ELECTRODE





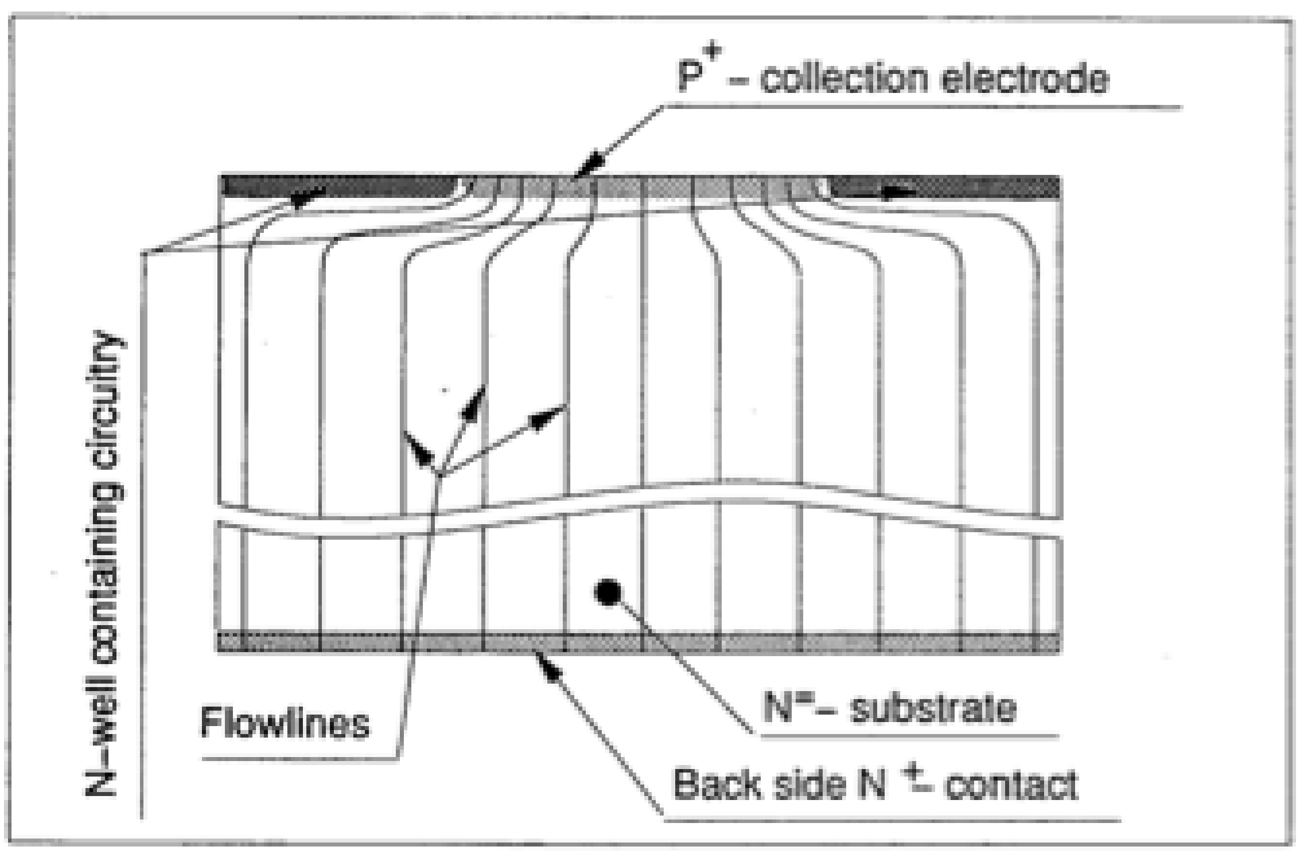
Need large voltage on extra diffusion to avoid signal loss

Beyond voltage limit for charge loss punchthrough between collection electrode and extra diffusion sets in…

=> Placing readout circuit directly in the substrate and connecting to the collection electrode is difficult

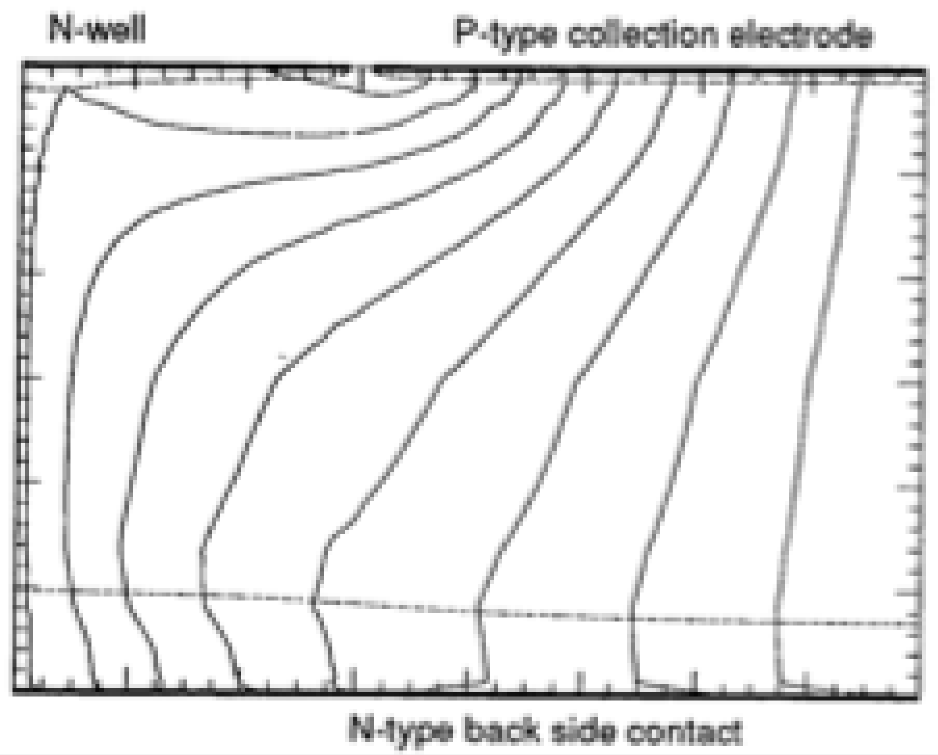
A WELL FOR THE READOUT CIRCUITRY

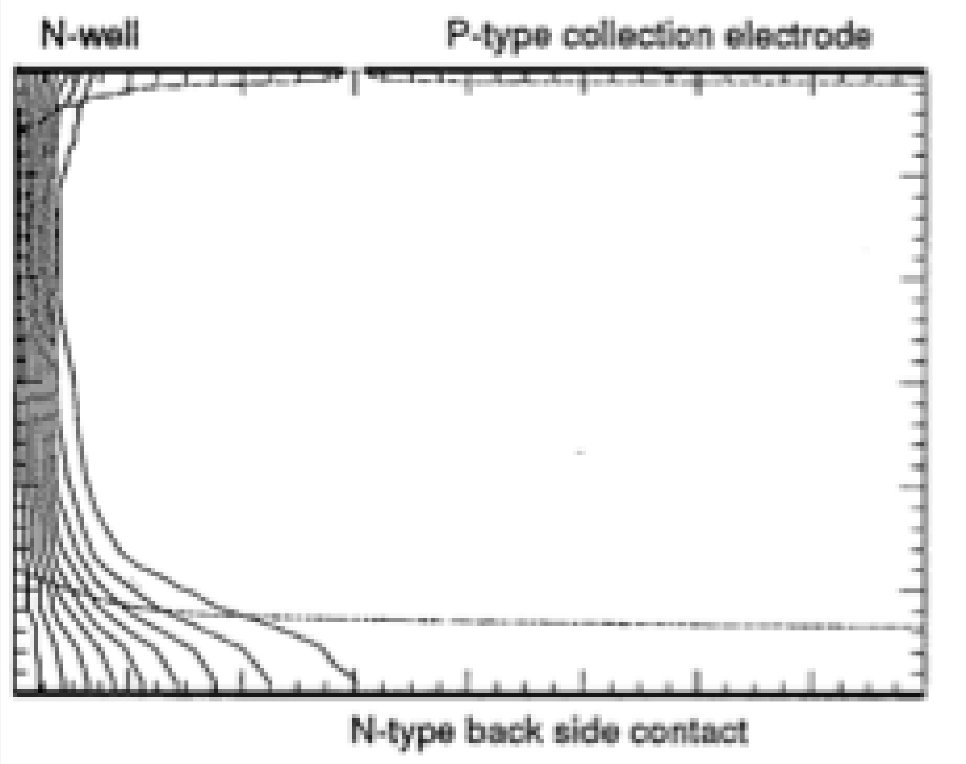
Proposed by S. Parker to shield circuit from detector part



A WELL FOR THE READOUT CIRCUITRY

Minimum well bias needed to avoid undepletion and large current



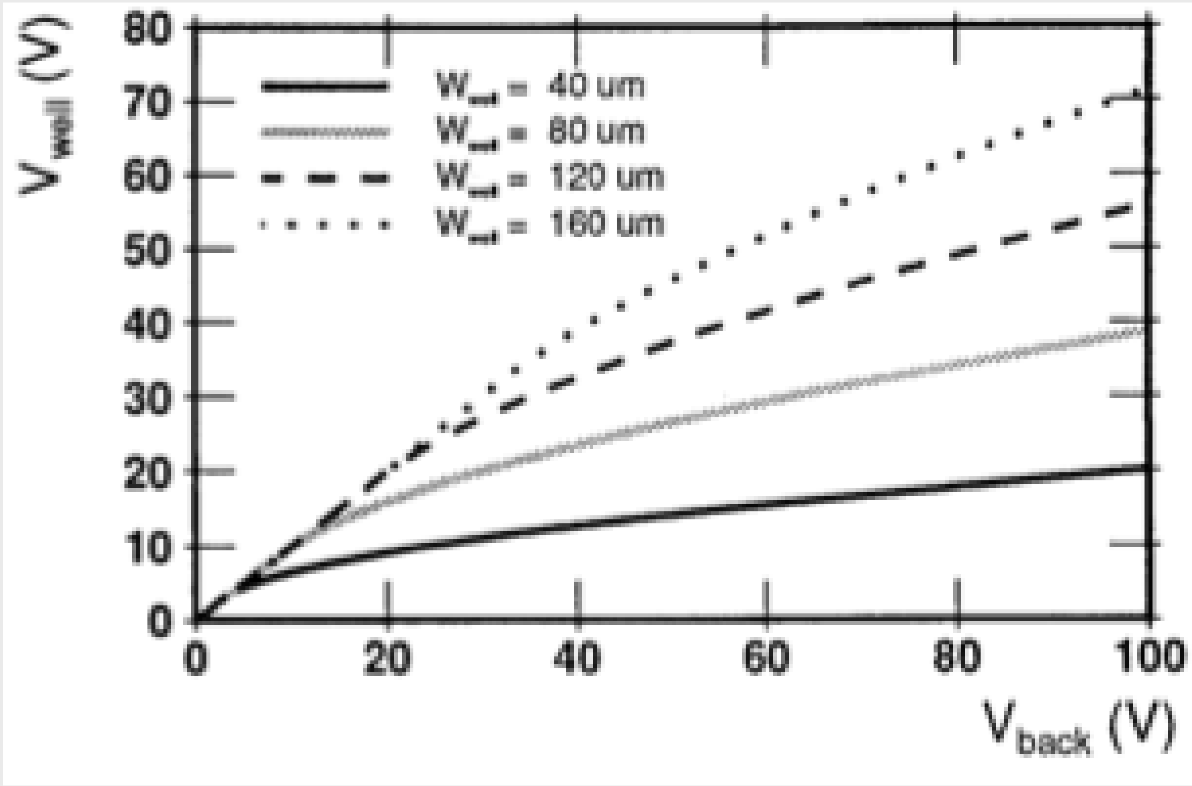


A few V above the limit.
Charge is collected on the collection electrode.

A few V below the limit.
A large current flows between Nwell and back side

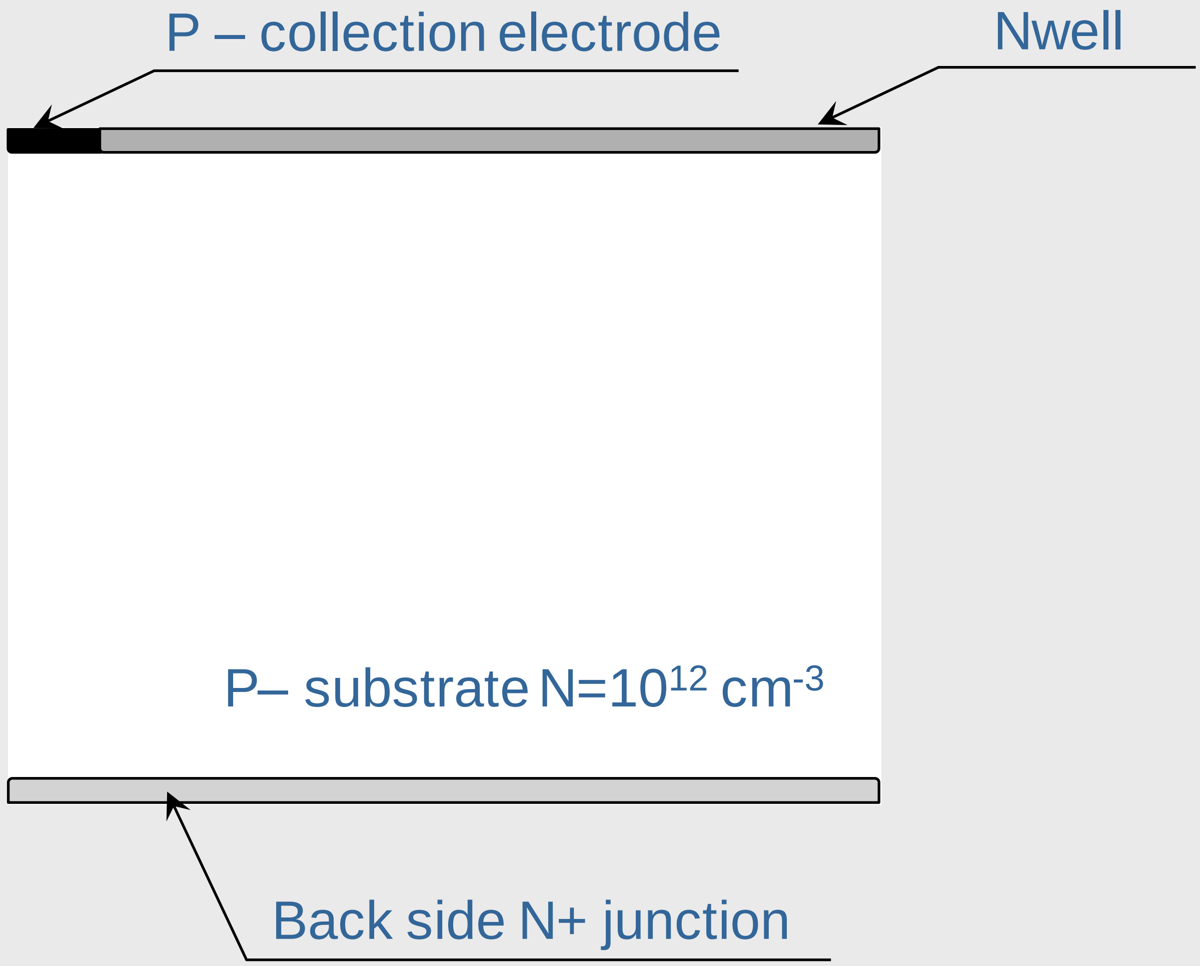
A WELL FOR THE READOUT CIRCUITRY

Minimum well bias for a 200 um wide collection electrode and various well sizes

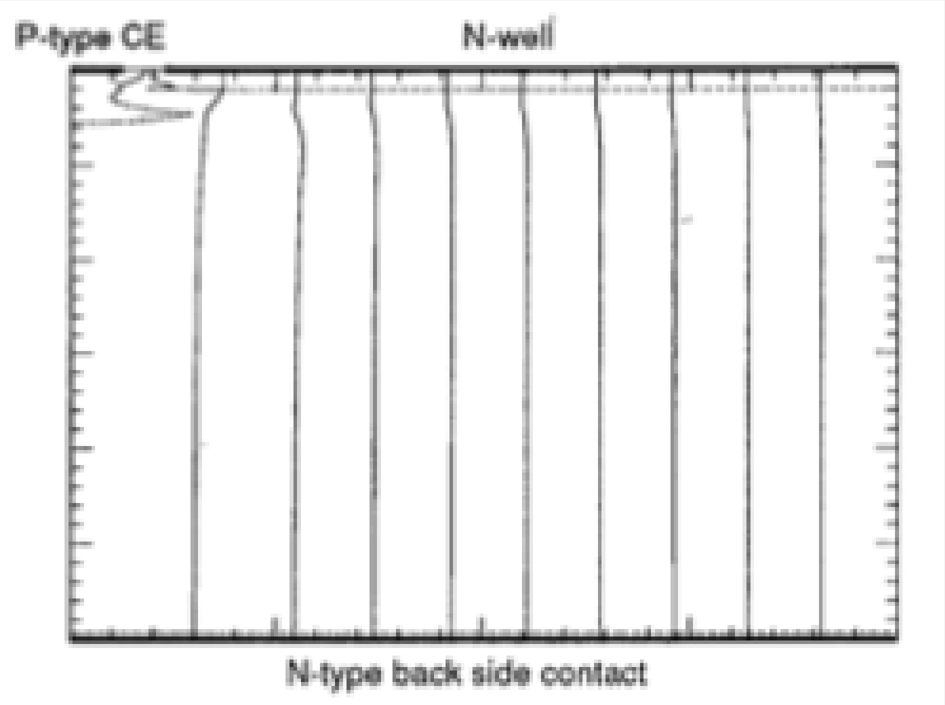


Large minimum well bias
even for a very large collection electrode !!

USE OF A WELL WITH BACK SIDE JUNCTION



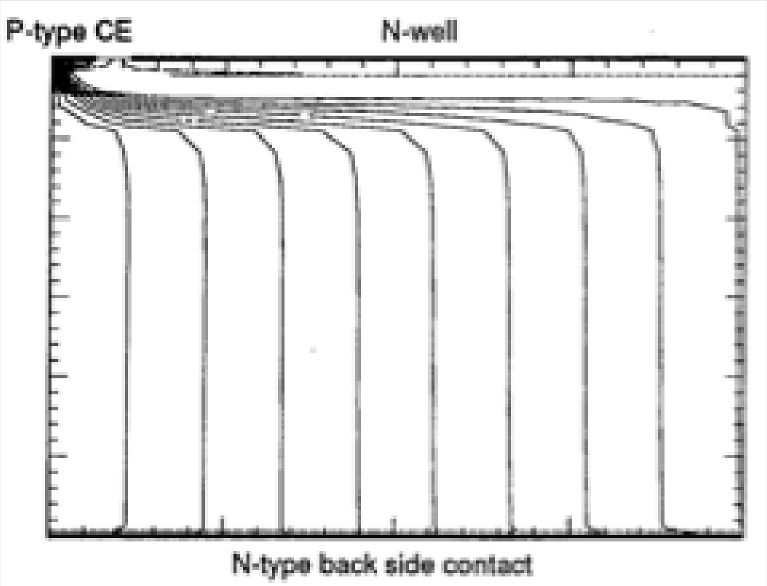
USE OF A WELL WITH BACK SIDE JUNCTION

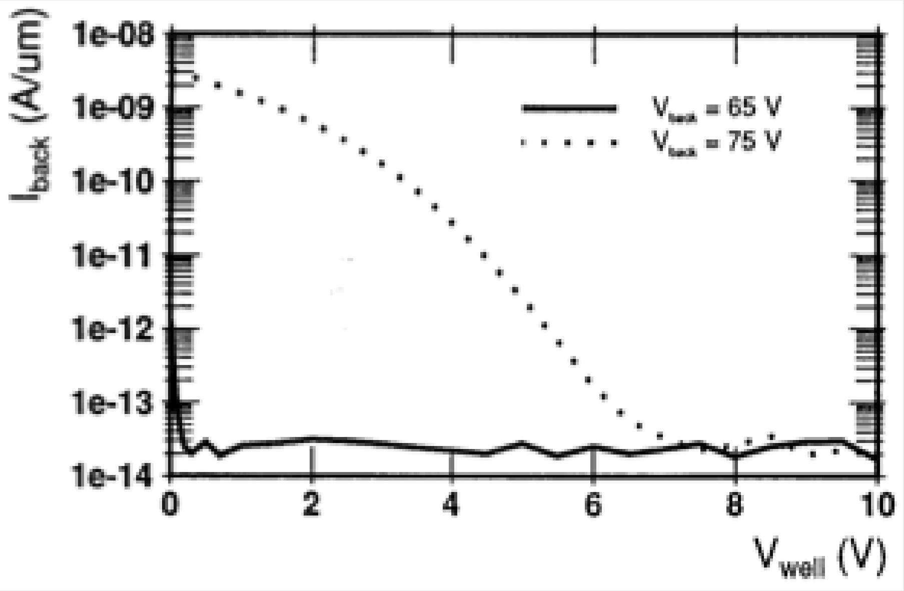


P-type collection electrode covers 1/10 of the width.
Full depletion required (otherwise short between collection electrodes)
At zero well bias and full depletion punchthrough between Nwell and N-diffusion on the back

USE OF A WELL WITH BACK SIDE JUNCTION

Minimum well bias to divert flow lines and eliminate punch through





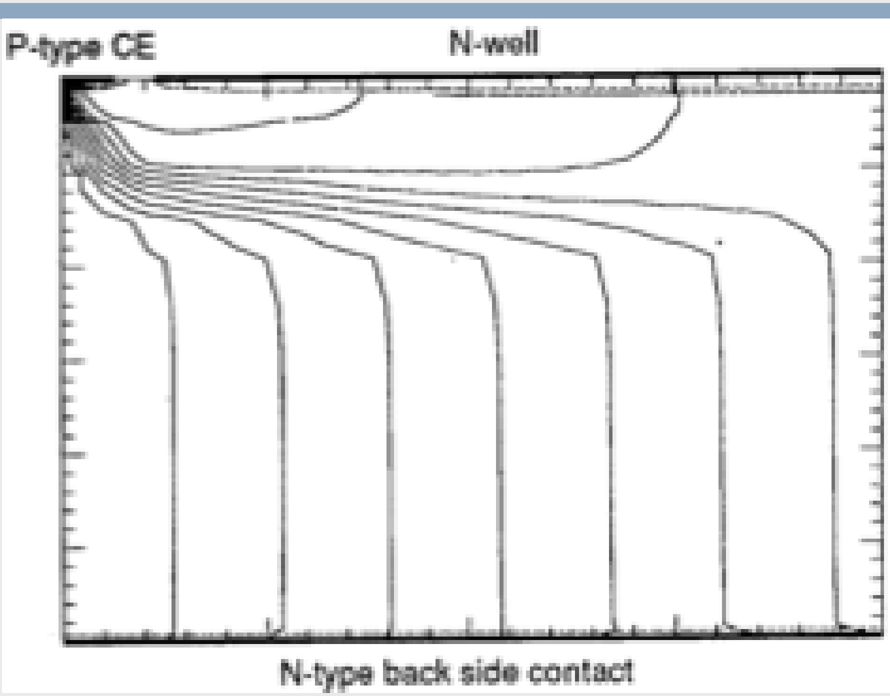
A few V on the well (with 65 V on the back) diverts all flow lines to the collection electrode.

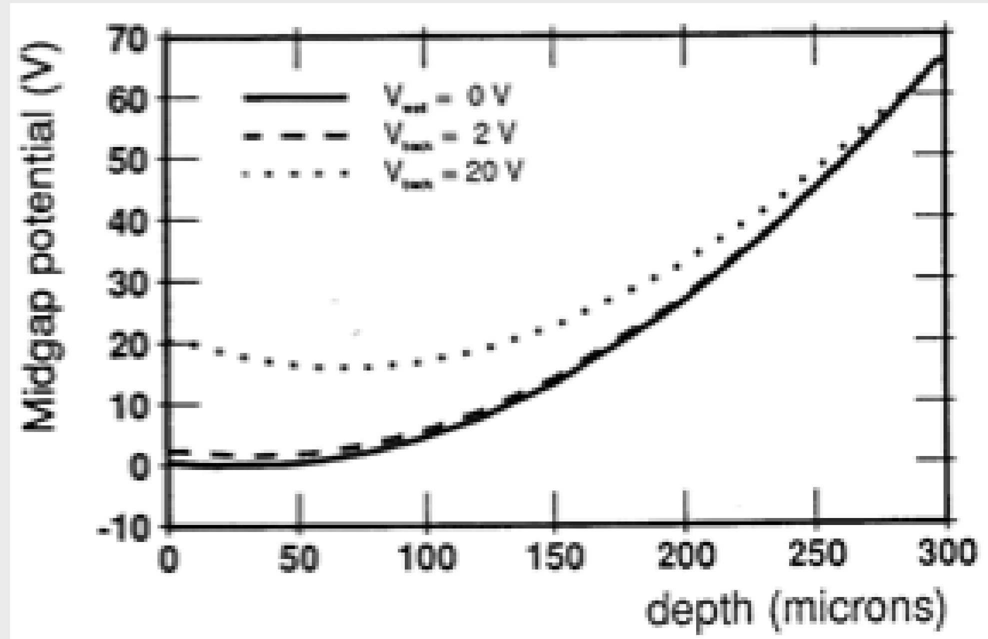
A potential barrier is formed underneath the well

The back side to Nwell current drops by orders of magnitude as the punchthrough is eliminated.

USE OF A WELL WITH BACK SIDE JUNCTION

Well bias and potential barrier



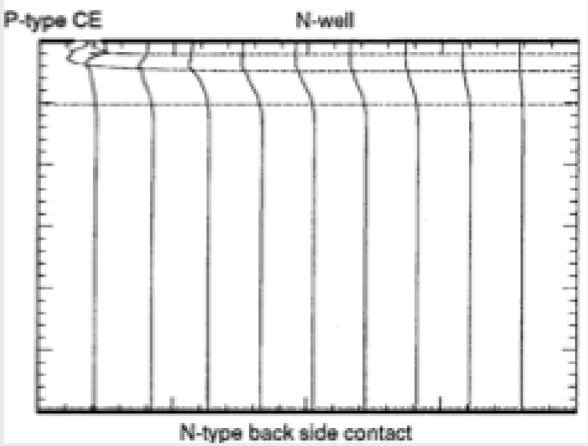


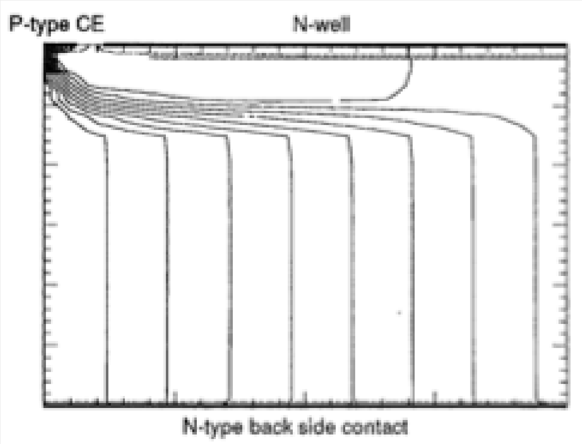
Increasing the well bias increases the potential barrier and moves the potential valley deeper into the substrate

USE OF A WELL WITH BACK SIDE JUNCTION

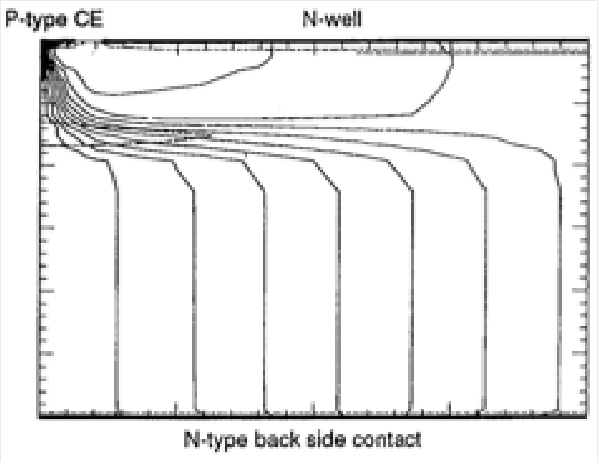
Well and back bias and depletion

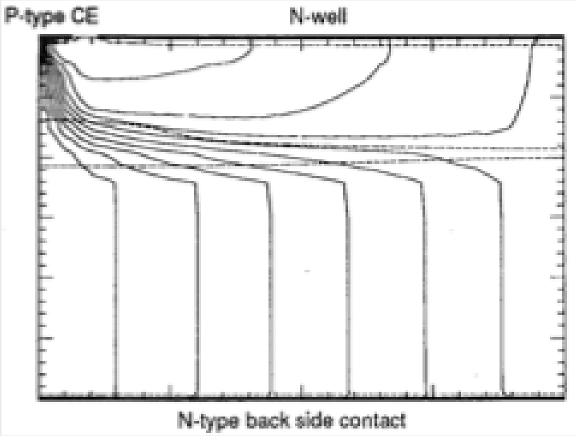
At lower back bias not fully depleted (left). Need a few V (4V) on the Nwell for full depletion (right)





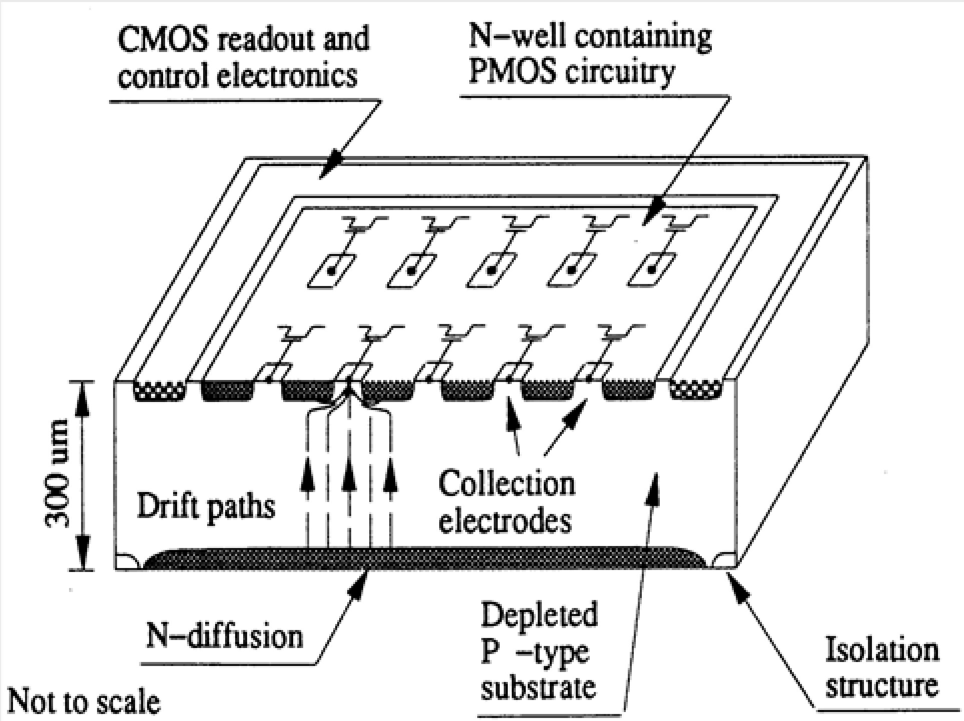
At high well biases (20 V left) undepletion occurs progressing over the full width when increasing the bias further (30 V right).

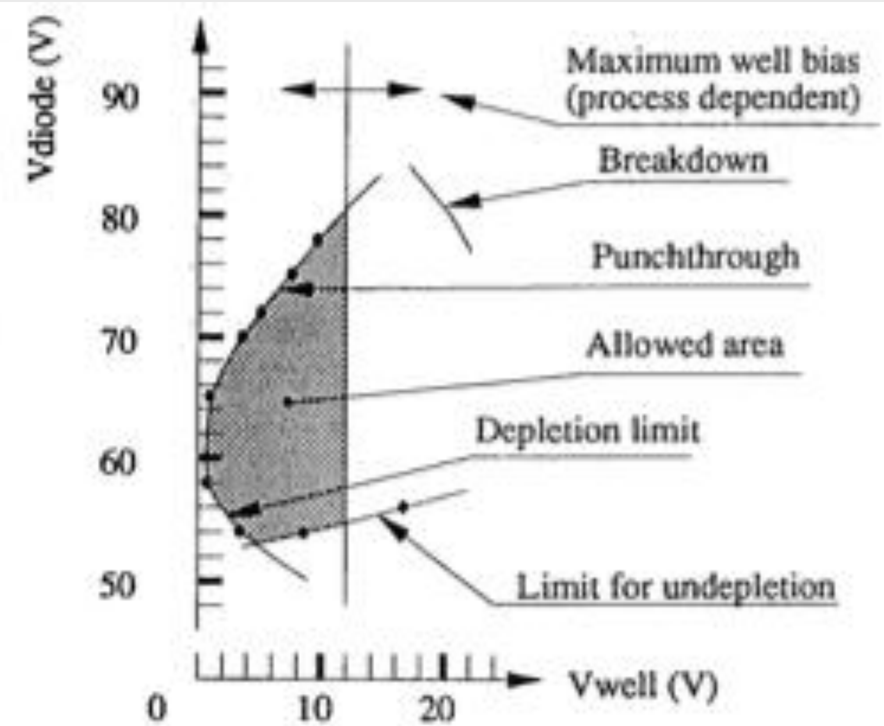




FINAL DEVICE & OPERATION LIMITS

Importance of device simulations



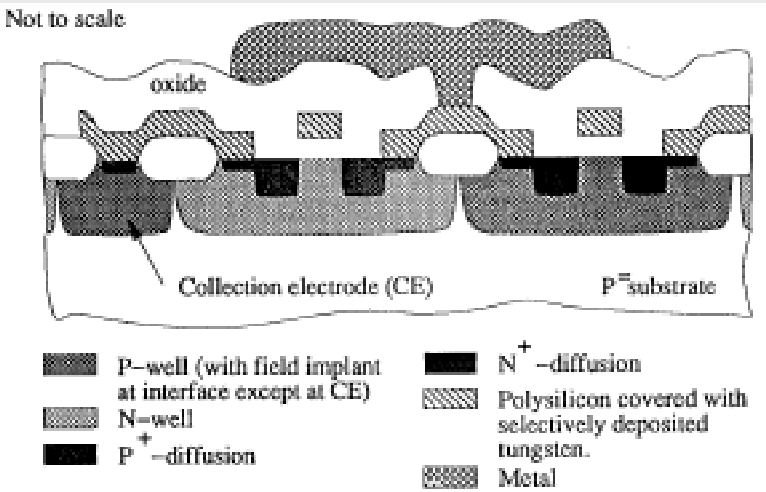


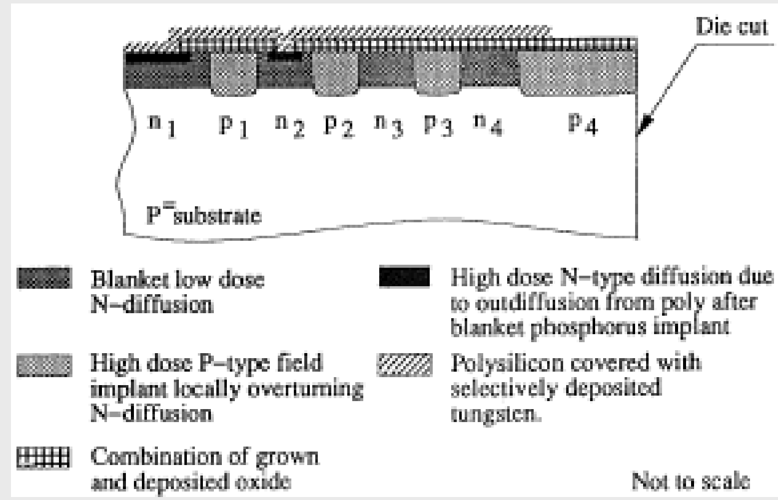
- Need full depletion (N=10^{12} cm^3)
- Back side processing (3 masks)

Operational limits
Importance of device simulations:
2D (PISCES)
3D (DA VINCI, available in 1992 only)

PROCESSING

Gettering on the back side using polysilicon & phosphorus implant

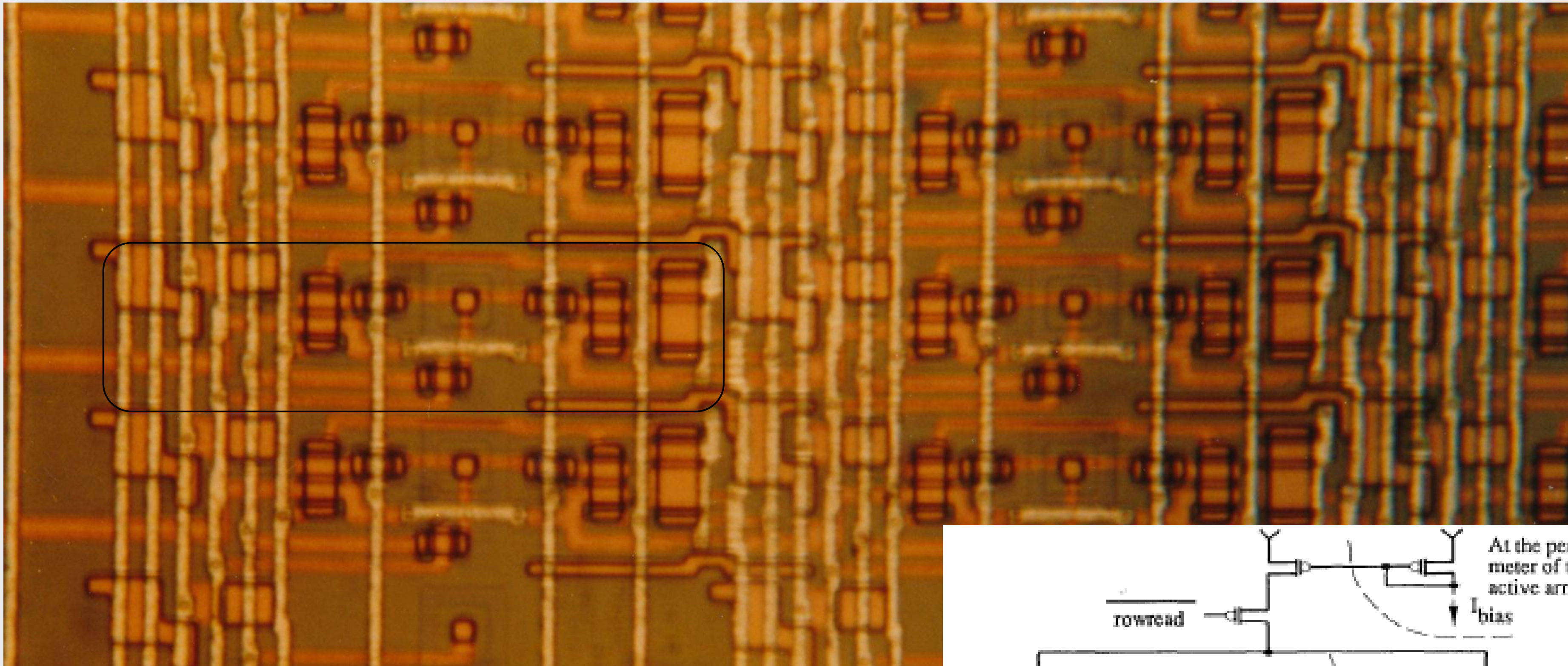


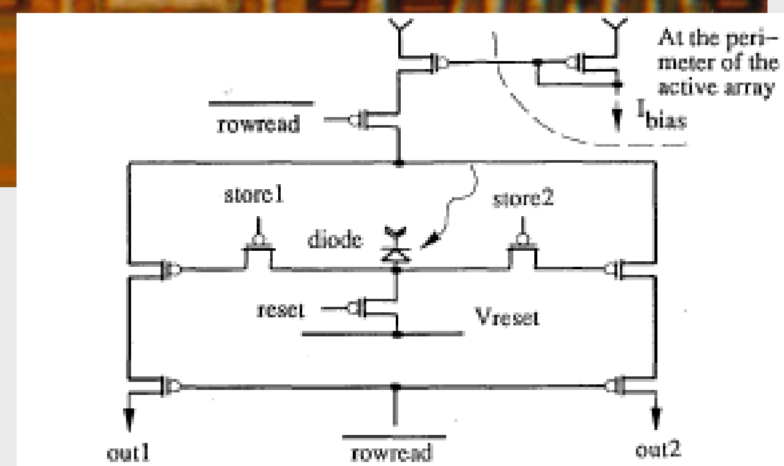


- Thirteen masks on the front side

- Three masks on the back side, Difficult in standard foundry
- Improved afterwards by trench etching (Julie Segal)

PIXEL CIRCUIT
125x34 micron pixel

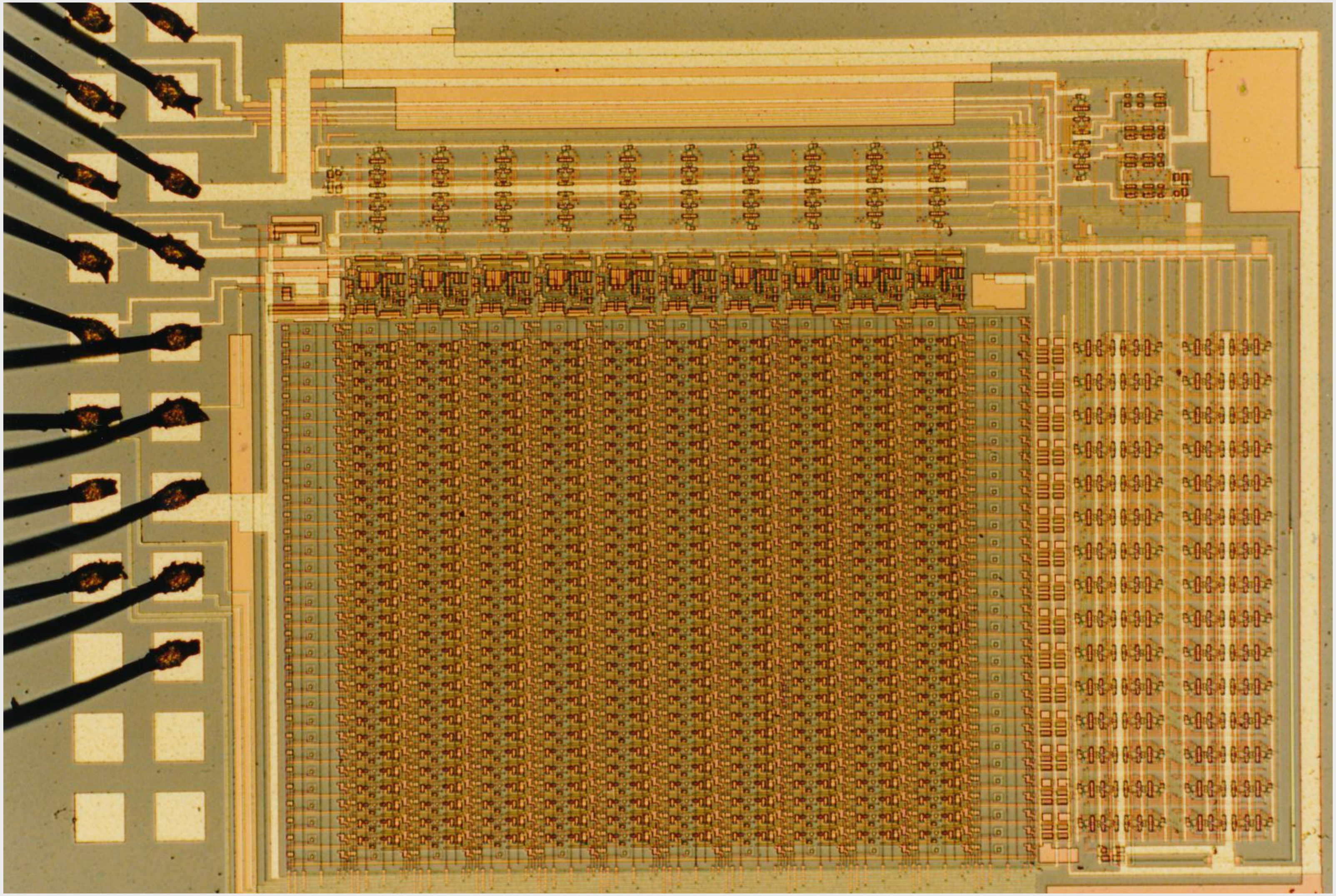




Ccollection electrode=26fF

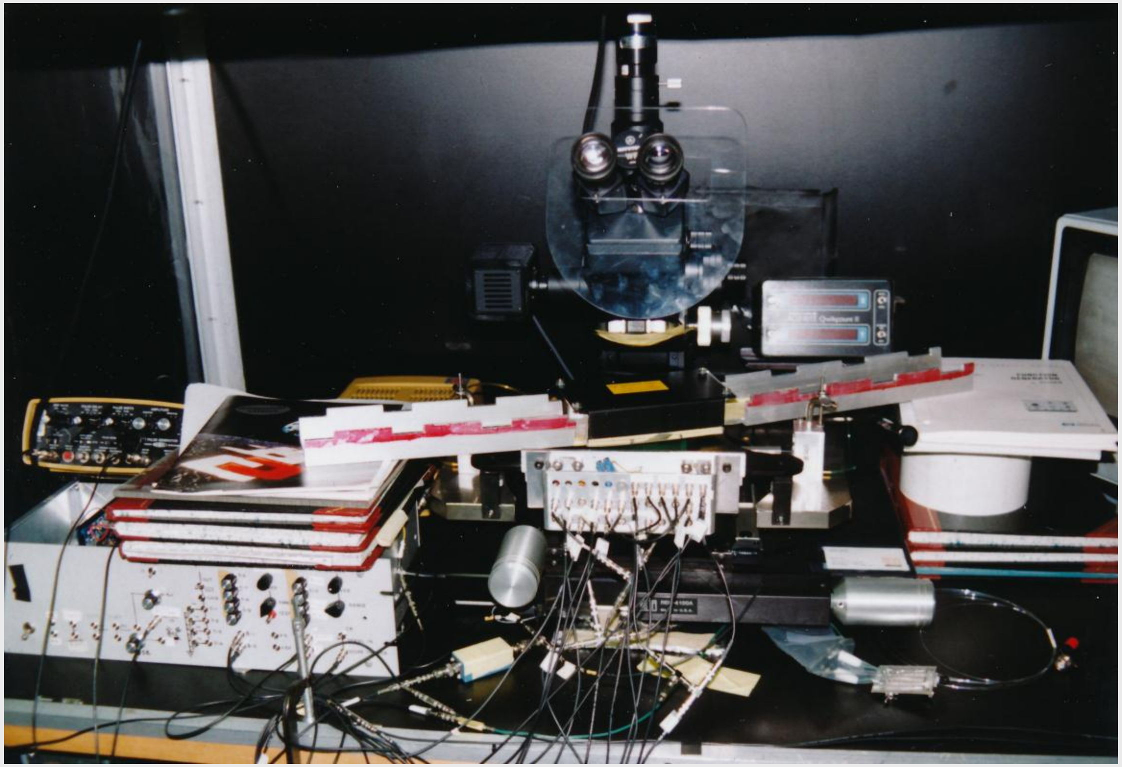
THE FULL CIRCUIT

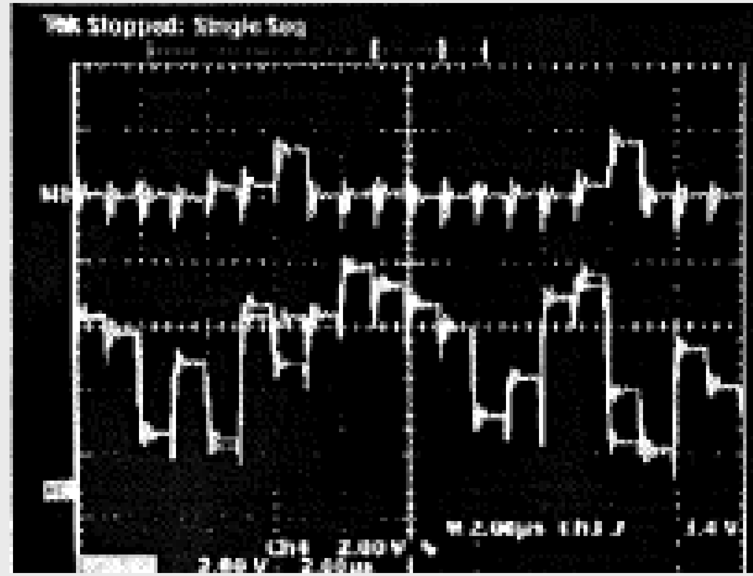
“yield structure”

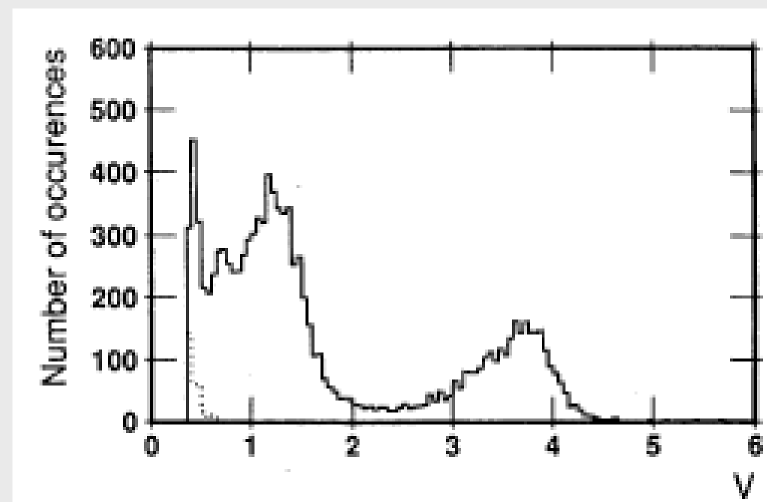


Measurements

Am^{241} Source

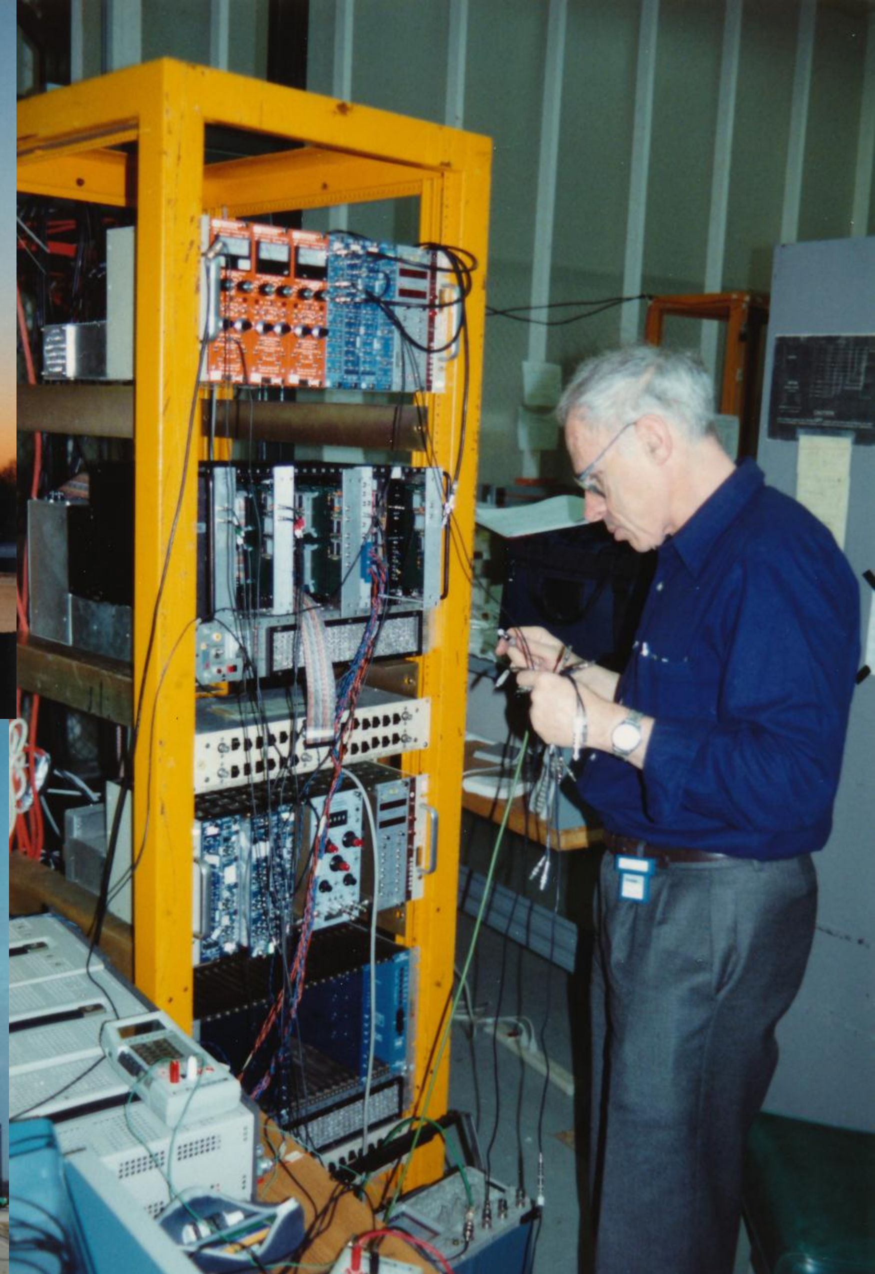




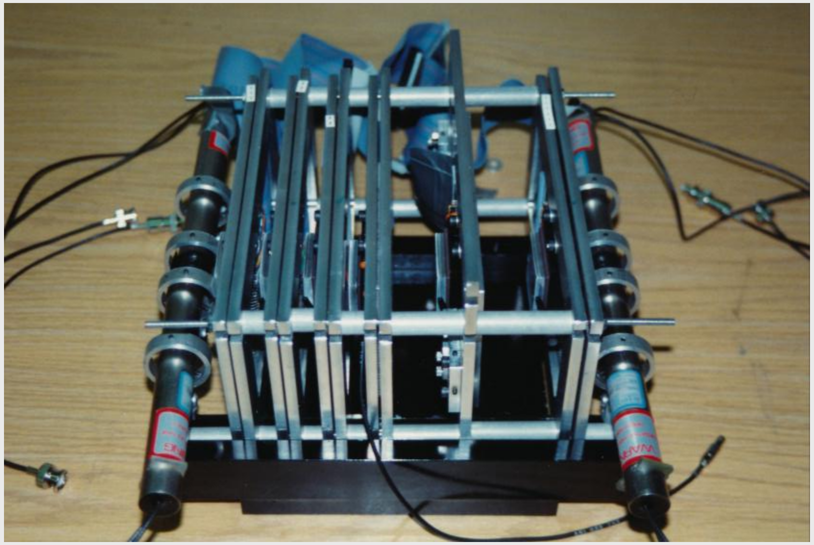


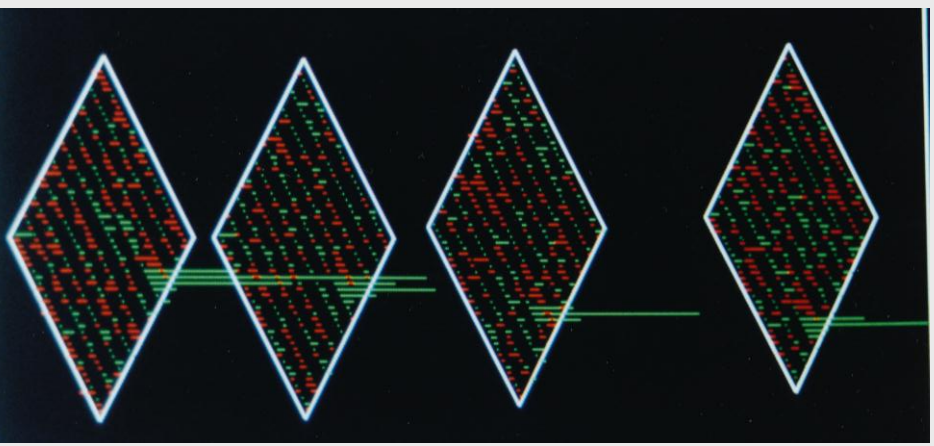
C=26fF P-type 1E12 cm^3

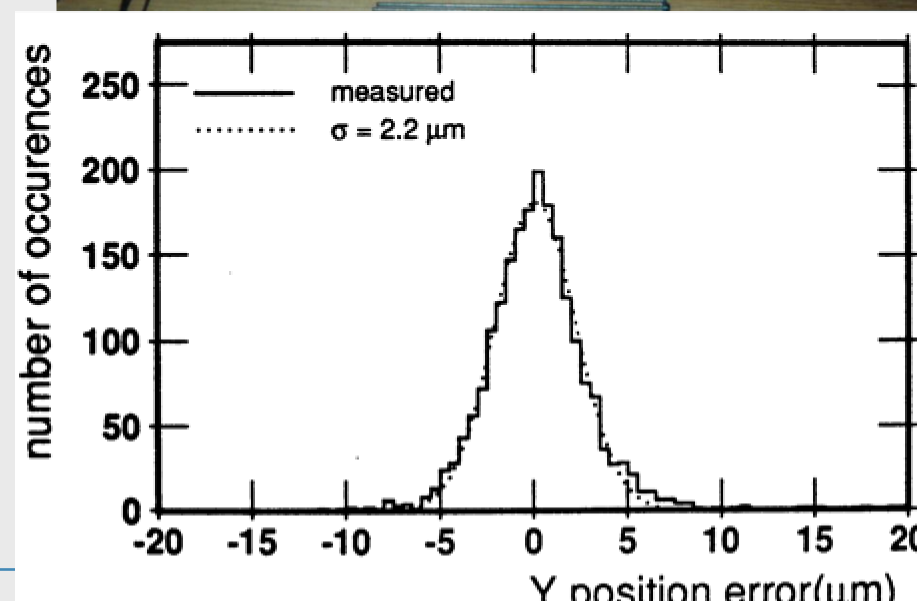




Beam test at Fermilab
(dec 1991-jan 1992)






number of occurences
measured
σ = 2.2 µm
250
200
150
100
50
0
-20
-15
-10
-5
0
5
10
15
20
Y position error(µm)


SONY
P6-120MP
Video 8
4910 -
4919

ACKNOWLEDGEMENTS

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- Lots of work behind the scenes to make things possible (funding, administration, getting beam time at end of run, getting in touch with FIB company, etc…)
- Patience, always making time to understand and explain, and come back with key suggestions (Use of a well, keeping wafers behind, etc…)
- Monolithic remains a hot topic today

- Tour guide in Chicago, Beatles, evening discussions…
- Hawaii

Thank You !